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Texas Instruments
CSD16325Q5

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N-Channel NexFET™ Power MOSFETs

Check for Samples: CSD16325Q5

FEATURES

- **Optimized for 5V Gate Drive**
- **Ultralow Q_g and Q_{gd}**
- **Low Thermal Resistance**
- **Avalanche Rated**
- **Pb Free Terminal Plating**
- **RoHS Compliant**
- **Halogen Free**
- **SON 5-mm × 6-mm Plastic Package**

APPLICATIONS

- **Point-of-Load Synchronous Buck in Networking, Telecom and Computing Systems**
- **Optimized for Synchronous FET Applications**

DESCRIPTION

The NexFET™ power MOSFET has been designed to minimize losses in power conversion applications and optimized for 5V gate drive applications.

PRODUCT SUMMARY

V_{DS}	Drain to Source Voltage	25		V
Q_g	Gate Charge Total (4.5V)	18		nC
Q_{gd}	Gate Charge Gate to Drain	3.5		nC
$R_{DS(on)}$	Drain to Source On Resistance	V_{GS} = 3V	2.1	mΩ
		V_{GS} = 4.5V	1.7	mΩ
		V_{GS} = 8V	1.5	mΩ
$V_{GS(th)}$	Threshold Voltage	1.1		V

ORDERING INFORMATION

Device	Package	Media	Qty	Ship
CSD16325Q5	SON 5-mm × 6-mm Plastic Package	13-Inch Reel	2500	Tape and Reel

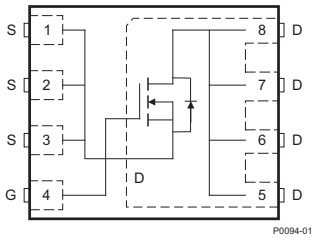
ABSOLUTE MAXIMUM RATINGS

T_A = 25°C unless otherwise stated		VALUE	UNIT
V_{DS}	Drain to Source Voltage	25	V
V_{GS}	Gate to Source Voltage	+10 / –8	V
I_D	Continuous Drain Current, T_C = 25°C	100	A
	Continuous Drain Current(1)	33	A
I_{DM}	Pulsed Drain Current, T_A = 25°C(2)	200	A
P_D	Power Dissipation(1)	3.1	W
T_J, T_{STG}	Operating Junction and Storage Temperature Range	–55 to 150	°C
E_{AS}	Avalanche Energy, single pulse I_D = 100A, L = 0.1mH, R_G = 25Ω	500	mJ

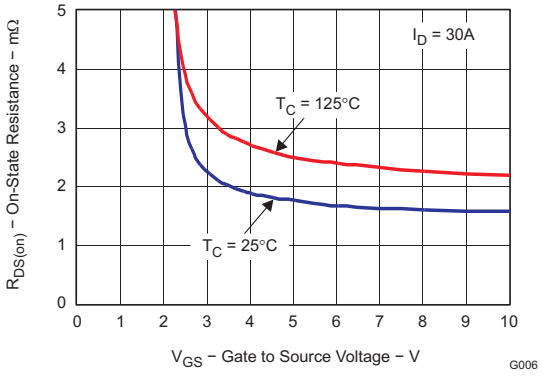
(1) Typical $R_{\theta JA}$ = 38°C/W on 1-inch^2 (6.45-cm^2), 2-oz. (0.071-mm thick) Cu pad on a 0.06-inch (1.52-mm) thick FR4 PCB.

(2) Pulse duration ≤300μs, duty cycle ≤2%

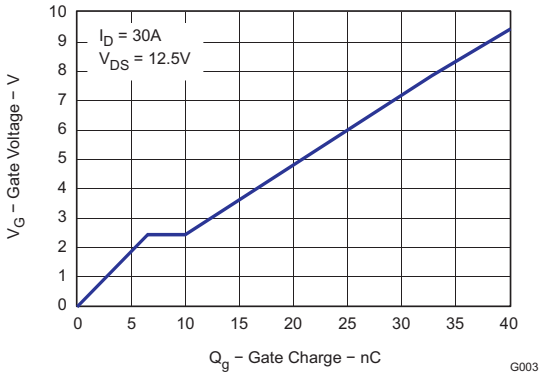
Top View



$R_{DS(on)}$ vs V_{GS}



Gate Charge



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

NexFET is a trademark of Texas Instruments.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ELECTRICAL CHARACTERISTICS

(T_A = 25°C unless otherwise stated)

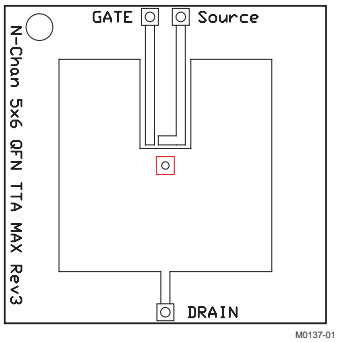
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Static Characteristics						
BV_{DSS}	Drain to Source Voltage	V_{GS} = 0V, I_D = 250µA	25			V
I_{DSS}	Drain to Source Leakage Current	V_{GS} = 0V, V_{DS} = 20V			1	µA
I_{GSS}	Gate to Source Leakage Current	V_{DS} = 0V, V_{GS} = +10/–8V			100	nA
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{DS} = V_{GS}, I_D = 250µA	0.9	1.1	1.4	V
$R_{DS(on)}$	Drain to Source On Resistance	V_{GS} = 3V, I_D = 30A		2.1	2.9	mΩ
		V_{GS} = 4.5V, I_D = 30A		1.7	2.2	mΩ
		V_{GS} = 8V, I_D = 30A		1.5	2	mΩ
g_{fs}	Transconductance	V_{DS} = 15V, I_D = 30A		159		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{GS} = 0V, V_{DS} = 12.5V, f = 1MHz		3070	4000	pF
C_{oss}	Output Capacitance			2190	2850	pF
C_{rss}	Reverse Transfer Capacitance			120	150	pF
R_G	Series Gate Resistance			1.6	3.2	Ω
Q_g	Gate Charge Total (4.5V)	V_{DS} = 12.5V, I_{DS} = 30A		18	25	nC
Q_{gd}	Gate Charge – Gate to Drain			3.5		nC
Q_{gs}	Gate Charge – Gate to Source			6.6		nC
$Q_{g(th)}$	Gate Charge at Vth			3.3		nC
Q_{oss}	Output Charge	V_{DS} = 13V, V_{GS} = 0V		43		nC
$t_{d(on)}$	Turn On Delay Time	V_{DS} = 12.5V, V_{GS} = 4.5V, I_{DS} = 30A, R_G =2Ω		10.5		ns
t_r	Rise Time			16		ns
$t_{d(off)}$	Turn Off Delay Time			32		ns
t_f	Fall Time			12		ns
Diode Characteristics						
V_{SD}	Diode Forward Voltage	I_{DS} = 30A, V_{GS} = 0V		0.8	1	V
Q_{rr}	Reverse Recovery Charge	V_{DD} = 10V, I_F = 30A, di/dt = 300A/µs		63		nC
t_{rr}	Reverse Recovery Time	V_{DD} = 10V, I_F = 30A, di/dt = 300A/µs		47		ns

THERMAL CHARACTERISTICS

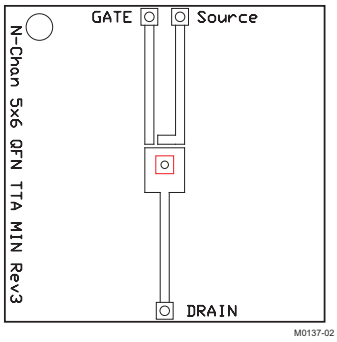
(T_A = 25°C unless otherwise stated)

PARAMETER		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Thermal Resistance Junction to Case(1)			1	°C/W
$R_{\theta JA}$	Thermal Resistance Junction to Ambient(1) (2)			50	°C/W

(1) $R_{\theta JC}$ is determined with the device mounted on a 1-inch^2 (6.45-cm^2), 2-oz. (0.071-mm thick) Cu pad on a 1.5-inch × 1.5-inch (3.81-cm × 3.81-cm), 0.06-inch (1.52-mm) thick FR4 PCB. $R_{\theta JC}$ is specified by design, whereas $R_{\theta JA}$ is determined by the user's board design.
(2) Device mounted on FR4 material with 1-inch^2 (6.45-cm^2), 2-oz. (0.071-mm thick) Cu.



Max $R_{\theta JA}$ = 50°C/W when mounted on 1 inch^2 (6.45 cm^2) of 2-oz. (0.071-mm thick) Cu.



Max $R_{\theta JA}$ = 126°C/W when mounted on minimum pad area of 2-oz. (0.071-mm thick) Cu.

TYPICAL MOSFET CHARACTERISTICS

(T_A = 25°C unless otherwise stated)

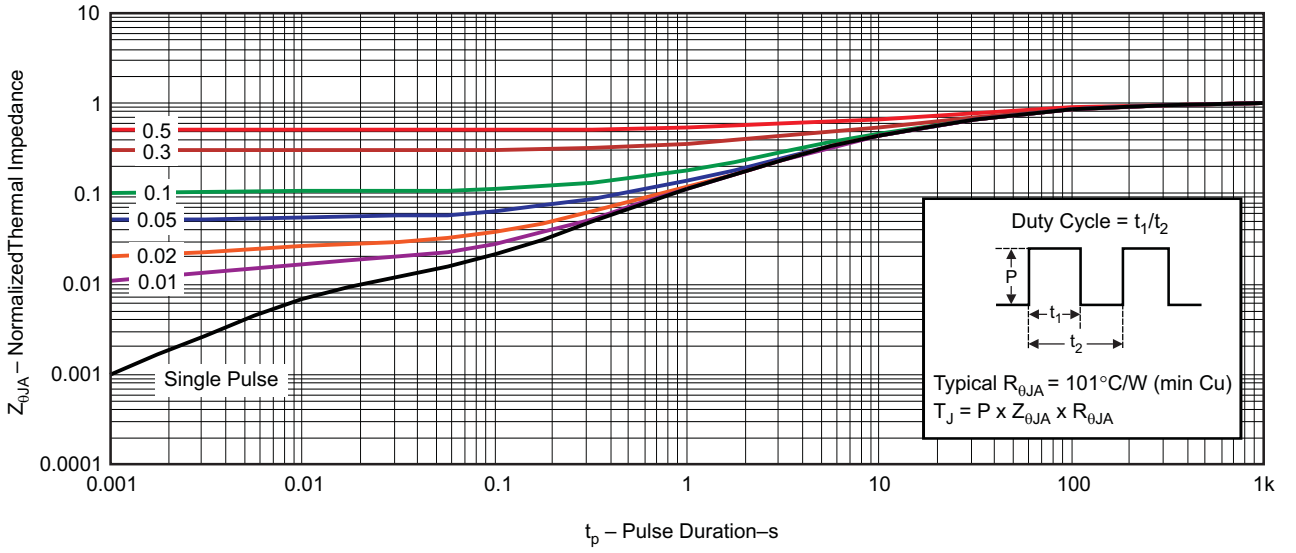


Figure 1. Transient Thermal Impedance

TYPICAL MOSFET CHARACTERISTICS (continued)

(T_A = 25°C unless otherwise stated)

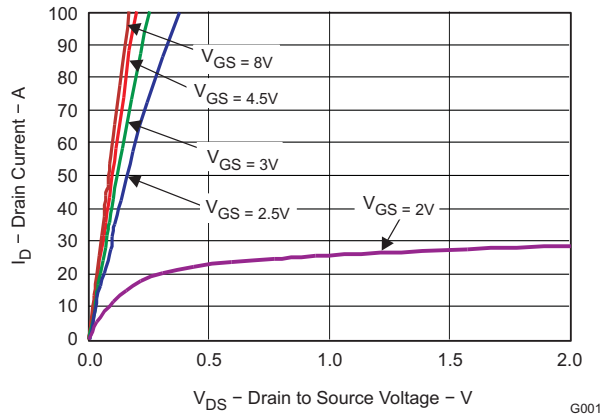


Figure 2. Saturation Characteristics

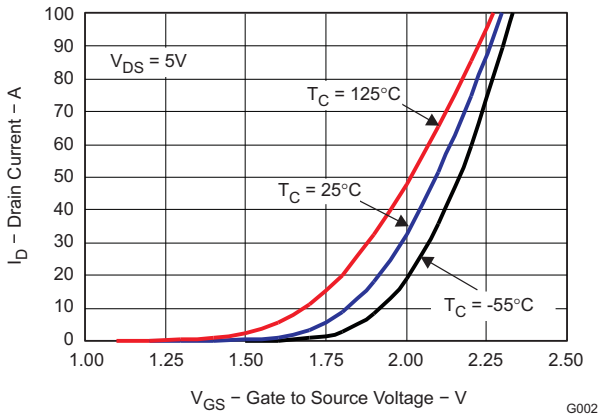


Figure 3. Transfer Characteristics

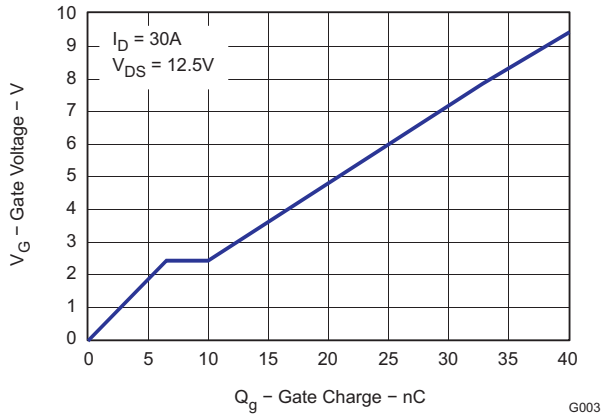


Figure 4. Gate Charge

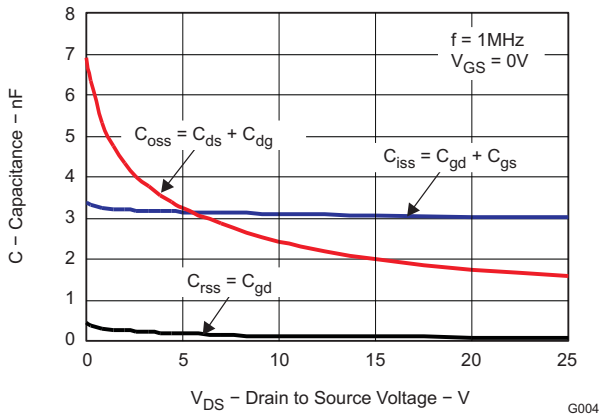


Figure 5. Capacitance

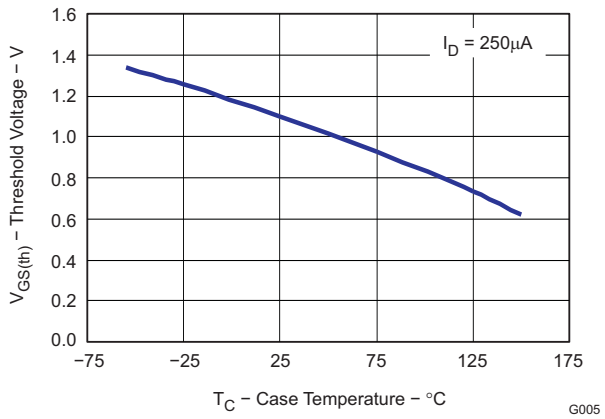


Figure 6. Threshold Voltage vs. Temperature

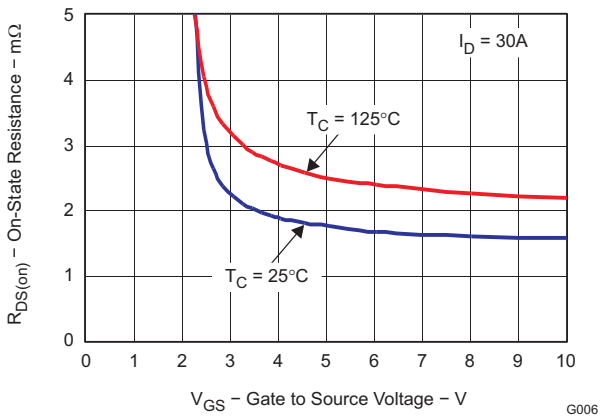


Figure 7. On-State Resistance vs. Gate to Source Voltage

TYPICAL MOSFET CHARACTERISTICS (continued)

(T_A = 25°C unless otherwise stated)

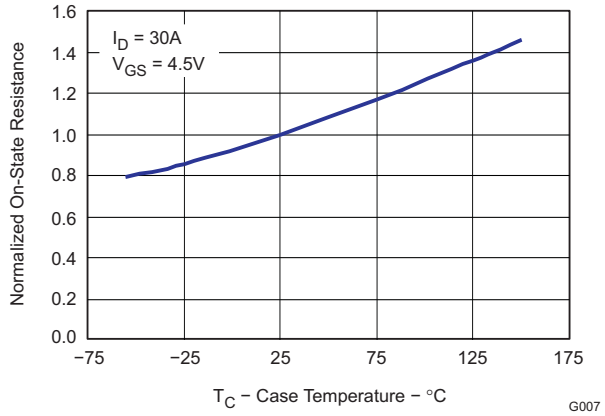


Figure 8. Normalized On-State Resistance vs. Temperature

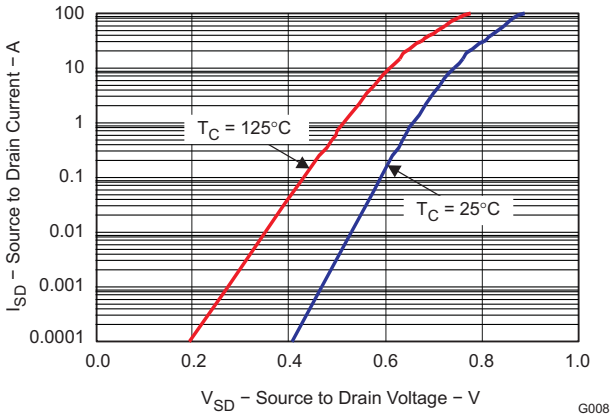


Figure 9. Typical Diode Forward Voltage

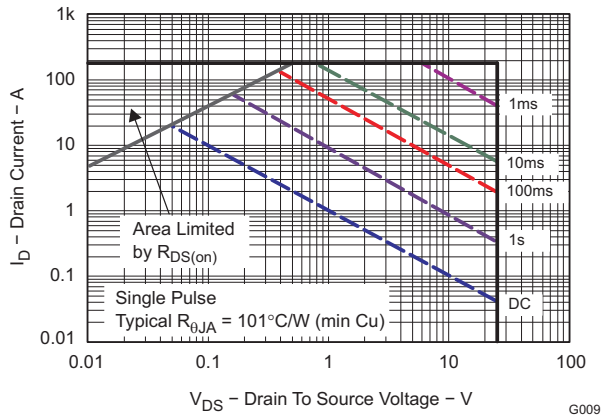


Figure 10. Maximum Safe Operating Area

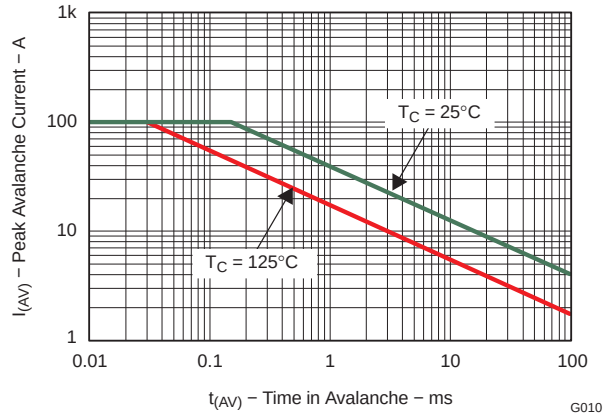


Figure 11. Single Pulse Unclamped Inductive Switching

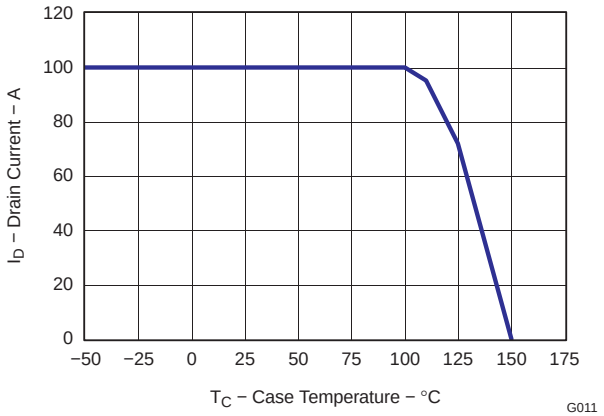
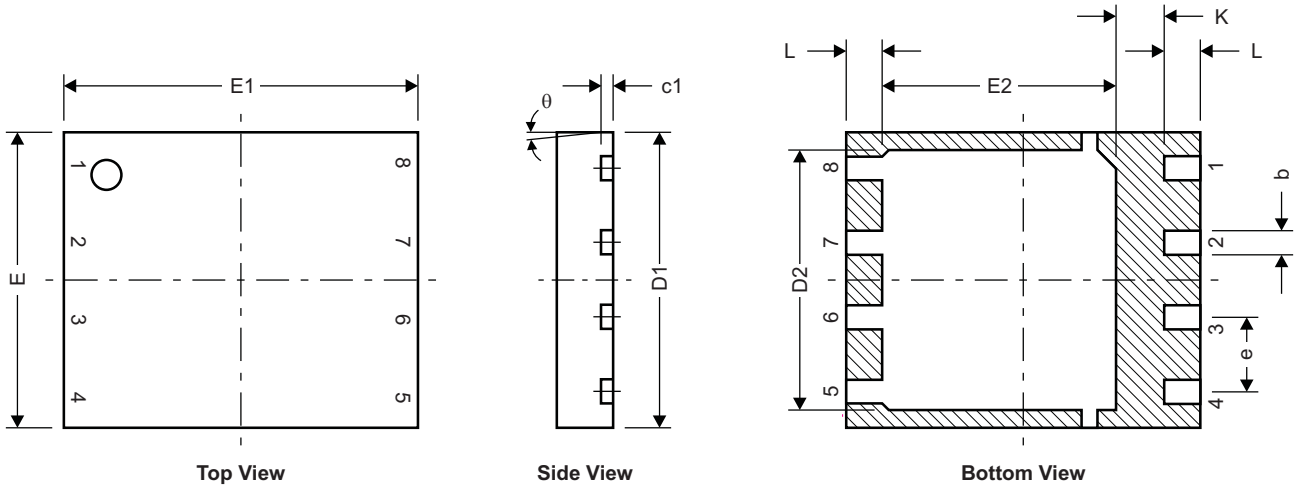
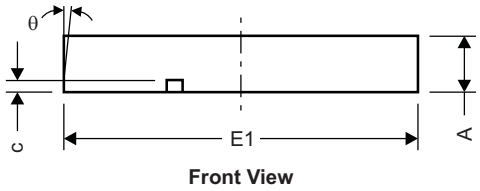


Figure 12. Maximum Drain Current vs. Temperature

MECHANICAL DATA

Q5 Package Dimensions

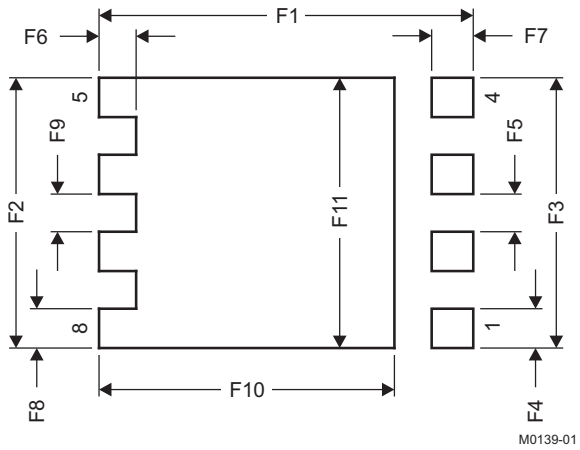




M0140-01

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.950	1.050	0.037	0.039
b	0.360	0.460	0.014	0.018
c	0.150	0.250	0.006	0.010
c1	0.150	0.250	0.006	0.010
D1	4.900	5.100	0.193	0.201
D2	4.320	4.520	0.170	0.178
E	4.900	5.100	0.193	0.201
E1	5.900	6.100	0.232	0.240
E2	3.920	4.12	0.154	0.162
e	1.27 TYP		0.050	
L	0.510	0.710	0.020	0.028
θ	0.00			

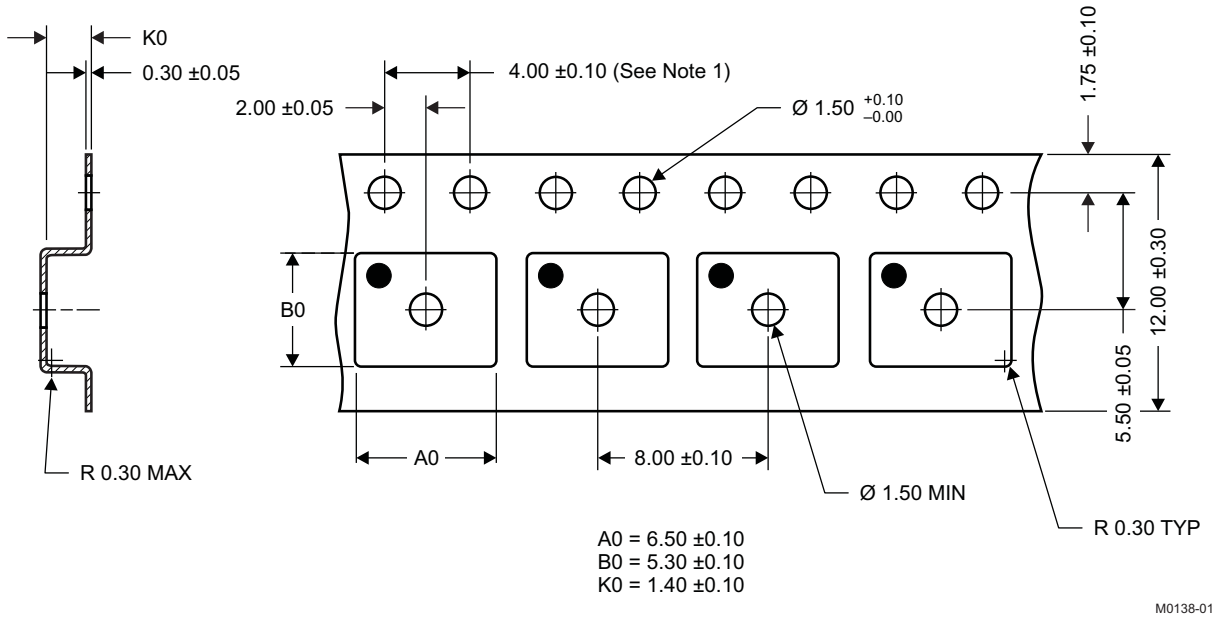
Recommended PCB Pattern



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
F1	6.205	6.305	0.244	0.248
F2	4.46	4.56	0.176	0.18
F3	4.46	4.56	0.176	0.18
F4	0.65	0.7	0.026	0.028
F5	0.62	0.67	0.024	0.026
F6	0.63	0.68	0.025	0.027
F7	0.7	0.8	0.028	0.031
F8	0.65	0.7	0.026	0.028
F9	0.62	0.67	0.024	0.026
F10	4.9	5	0.193	0.197
F11	4.46	4.56	0.176	0.18

For recommended circuit layout for PCB designs, see application note SLPA005 – *Reducing Ringing Through PCB Layout Techniques*.

Q5 Tape and Reel Information



Notes:

1. 10-sprocket hole-pitch cumulative tolerance ±0.2
2. Camber not to exceed 1mm in 100mm, noncumulative over 250mm
3. Material: black static-dissipative polystyrene
4. All dimensions are in mm, unless otherwise specified.
5. A0 and B0 measured on a plane 0.3mm above the bottom of the pocket
6. MSL1 260°C (IR and convection) PbF reflow compatible

REVISION HISTORY

Changes from Original (August 2009) to Revision A **Page**

- Changed Q_{rr} Reverse Recovery Charge typical value From: 102nC To: 63nC 2

Changes from Revision A (September 2009) to Revision B **Page**

- Changed Note 1 of the ABSOLUTE MAXIMUM RATINGS From: $R_{\theta JA}$ = 38°C/W To: Typical $R_{\theta JA}$ = 38°C/W 1
- Changed I_{DM} Pulsed Drain Current in the ABSOLUTE MAXIMUM RATINGS From: 210A To: 200A 1
- Changed From: Max $R_{\theta JA}$ = 48°C/W To: Max $R_{\theta JA}$ = 50°C/W 3
- Changed From: Max $R_{\theta JA}$ = 113°C/W To: Max $R_{\theta JA}$ = 126°C/W 3
- Changed Figure 1 text - From: $R_{\theta JA}$ = 101°C/W To: Typical $R_{\theta JA}$ = 101°C/W 3
- Changed Figure 10 text - From: $R_{\theta JA}$ = 101°C/W To: Typical $R_{\theta JA}$ = 101°C/W 5

Changes from Revision B (April 2010) to Revision C **Page**

- Changed $R_{DS(on)}$ - V_{GS} = 3V in the Electrical Characteristics table From: 2.7 to 2.9 in the max column 2
- Deleted the Package Marking Information section 7

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD16325Q5	ACTIVE	VSON-CLIP	DQH	8	2500	Pb-Free (RoHS Exempt)	CU SN	Level-1-260C-UNLIM	-55 to 150	CSD16325	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

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