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Texas Instruments CSD25302Q2

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Datasheet of CSD25302Q2 - MOSFET P-CH 20V 5A 6SON Contact us: sales@integrated-circuit.com Website: www.integrated-circuit.com





CSD25302Q2

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SLPS234B – NOVEMBER 2009 – REVISED JANUARY 2012

P-Channel NexFET[™] Power MOSFET

FEATURES

- Ultralow Q_g and Q_{gd}
- Low Thermal Resistance
- Avalanche Rated
- Pb Free Terminal Plating
- RoHS Compliant
- Halogen Free
- SON 2-mm × 2-mm Plastic Package

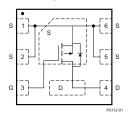
APPLICATIONS

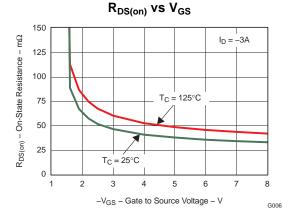
- Battery Management
- Load Management
- Battery Protection

DESCRIPTION

The device has been designed to deliver the lowest on resistance and gate charge in the smallest outline possible with excellent thermal characteristics in an ultra low profile. Low on resistance coupled with the extremely small footprint and low profile make the device ideal for battery operated space constrained applications.

Top View







Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

PRODUCT SUMMARY

V _{DS}	Drain to Source Voltage	-20		V
Qg	Gate Charge Total (-4.5V)	2.6		nC
Q _{gd}	Gate Charge Gate to Drain	0.5		nC
		$V_{GS} = -1.8V$	71	mΩ
R _{DS(on)}	Drain to Source On Resistance	$V_{GS} = -2.5V$	56	mΩ
		$V_{GS} = -4.5V$	39	mΩ
V _{GS(th)}	Threshold Voltage	-0.65		V

ORDERING INFORMATION

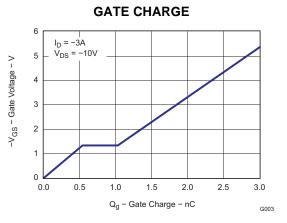
Device Package		Media	Qty	Ship	
CSD25302Q2	SON 2-mm × 2-mm Plastic Package	13-Inch Reel	3000	Tape and Reel	

ABSOLUTE MAXIMUM RATINGS

T _A = 25	°C unless otherwise stated	VALUE	UNIT
V _{DS}	Drain to Source Voltage	-20	V
V_{GS}	Gate to Source Voltage	±8	V
	Continuous Drain Current, $T_C = 25^{\circ}C$	-5	Α
ID	Continuous Drain Current ⁽¹⁾	-5	Α
I _{DM}	Pulsed Drain Current, $T_A = 25^{\circ}C^{(2)}$	-20	А
PD	Power Dissipation	2.4	W
T _J , T _{STG}	Operating Junction and Storage Temperature Range	-55 to 150	°C

(1) Package Limited

(2) Pulse duration 10 μ s, duty cycle ≤2%







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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ELECTRICAL CHARACTERISTICS

PARAMETER		TEST CONDITIONS		TYP	MAX	UNIT
Static Cl	haracteristics					
BV _{DSS}	Drain to Source Voltage	$V_{GS} = 0V, I_{DS} = -250\mu A$	-20			V
I _{DSS}	Drain to Source Leakage	$V_{GS} = 0V, V_{DS} = -16V$			-1	μA
I _{GSS}	Gate to Source Leakage	$V_{DS} = 0V, V_{GS} = \pm 8V$			-100	nA
V _{GS(th)}	Gate to Source Threshold Voltage	$V_{DS} = V_{GS}, I_{DS} = -250 \mu A$	-0.5	-0.65	-0.9	V
		$V_{GS} = -1.8V, I_{DS} = -3.0A$		71	92	mΩ
R _{DS(on)}	Drain to Source On Resistance	$V_{GS} = -2.5V, I_{DS} = -3.0A$		56	70	mΩ
		$V_{GS} = -4.5V, I_{DS} = -3.0A$		39	49	mΩ
9 _{fs}	Transconductance	$V_{DS} = -10V, I_{DS} = -3.0A$		12.3		S
Dynamic	Characteristics					
C _{ISS}	Input Capacitance			270	350	pF
C _{OSS}	Output Capacitance	$V_{GS} = 0V, V_{DS} = -10V, f = 1MHz$		120	150	pF
C _{RSS}	Reverse Transfer Capacitance			40	55	pF
Qg	Gate Charge Total (-4.5V)			2.6	3.4	nC
Q _{gd}	Gate Charge – Gate to Drain			0.5		nC
Q _{gs}	Gate Charge Gate to Source	$V_{\rm DS} = -10V, I_{\rm DS} = -3.0A$		0.54		nC
Qg(th)	Gate Charge at Vth			0.2		nC
Q _{OSS}	Output Charge	$V_{DS} = -13V, V_{GS} = 0V$		2.3		nC
t _{d(on)}	Turn On Delay Time			3.2		ns
t _r	Rise Time			13.2		ns
t _{d(off)}	Turn Off Delay Time	$-V_{DS} = -10V, V_{GS} = -4.5V, I_{DS} = -3.0A, R_{G} = 2\Omega$		8.6		ns
t _f	Fall Time			1.3		ns
Diode C	haracteristics		!			
V _{SD}	Diode Forward Voltage	$I_{DS} = -3.0A, V_{GS} = 0V$		-0.8	-1.0	V
Q _{rr}	Reverse Recovery Charge			2.5		nC
t _{rr}	Reverse Recovery Time	V_{dd} = -13V, I _F = -3.0A, di/dt = 300A/µs		8.8		ns

THERMAL CHARACTERISTICS

 $T_A = 25^{\circ}C$, unless otherwise specified

	PARAMETER		TYP	MAX	UNIT
R_{\thetaJC}	Thermal Resistance Junction to Case ⁽¹⁾			8.6	°C/W
R_{\thetaJA}	Thermal Resistance Junction to Ambient ⁽¹⁾⁽²⁾			66	°C/W

R_{0JC} is determined with the device mounted on a 1-inch² (6.45-cm²), 2-oz. (0.071-mm thick) Cu pad on a 1.5-inch × 1.5-inch (3.81-cm × (1) 3.81-cm), 0.06-inch (1.52-mm) thick FR4 PCB. $R_{\theta JC}$ is specified by design, whereas $R_{\theta JA}$ is determined by the user's board design. Device mounted on FR4 material with 1-inch² (6.45-cm²), 2-oz. (0.071-mm thick) Cu. (2)

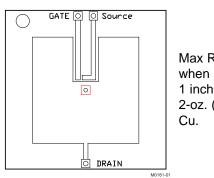


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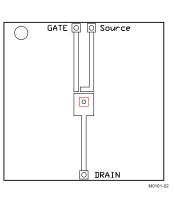
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Max $R_{\theta JA} = 66^{\circ}C/W$ when mounted on 1 inch² (6.45 cm²) of 2-oz. (0.071-mm thick)



Max $R_{\theta JA} = 207^{\circ}C/W$ when mounted on minimum pad area of 2-oz. (0.071-mm thick) Cu.



 $T_A = 25^{\circ}C$, unless otherwise specified

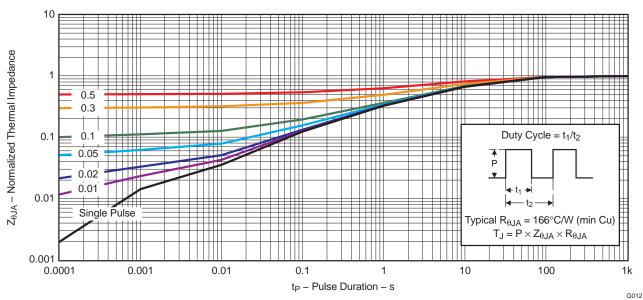


Figure 1. Transient Thermal Impedance



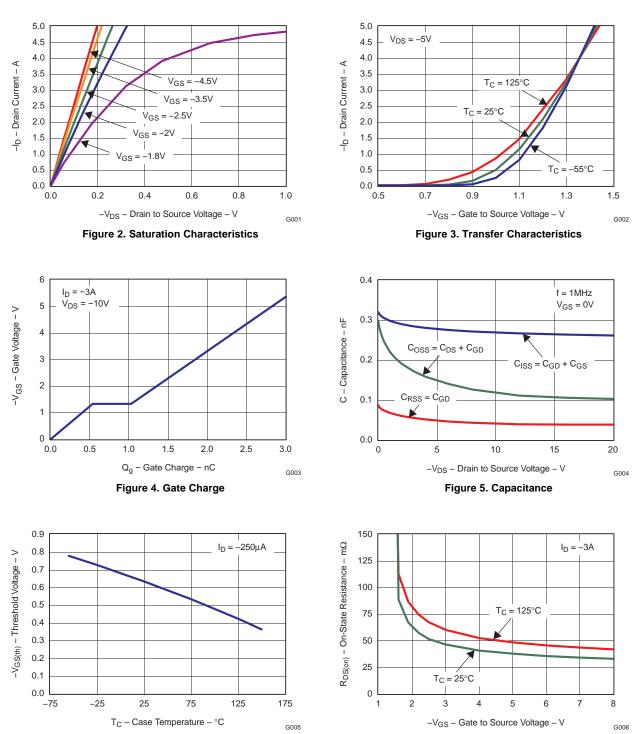


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TYPICAL MOSFET CHARACTERISTICS (continued)



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Figure 6. Threshold Voltage vs. Temperature



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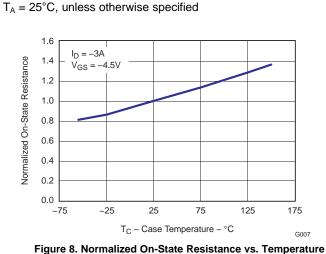
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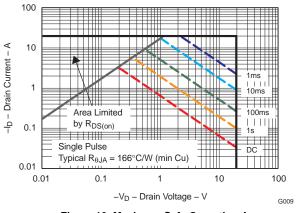
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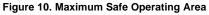
TYPICAL MOSFET CHARACTERISTICS (continued)

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 $\mathbf{Figure 9. Typical Diode Forward Voltage}^{\mathsf{v}}$





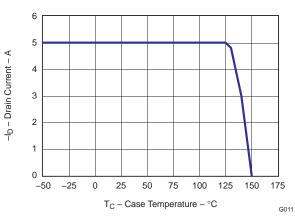


Figure 11. Maximum Drain Current vs. Temperature



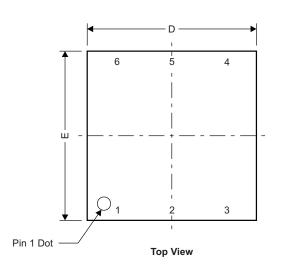
TEXAS INSTRUMENTS

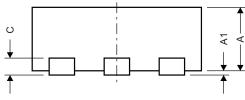
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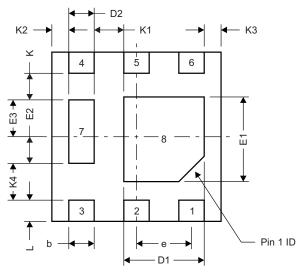
MECHANICAL DATA

Q2 Package Dimensions





Front	View
FIOII	view



Bottom View

Pinout				
Source	1, 2, 5, 6, 8			
Gate	3			
Drain	4, 7			

M0175-01

DIM		MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX	
A	0.700	0.750	0.800	0.028	0.030	0.032	
A1	0.000		0.050	0.000		0.002	
b	0.250	0.300	0.350	0.010	0.012	0.014	
С		0.203 TYP			0.008 TYP		
D		2.000 TYP			0.080 TYP		
D1	0.900	0.950	1.000	0.036	0.038	0.040	
D2		0.300 TYP			0.012 TYP		
E		2.000 TYP			0.080 TYP		
E1	0.900	1.000	1.100	0.036	0.040	0.044	
E2		0.280 TYP			0.0112 TYP		
E3		0.470 TYP			0.0188 TYP		
е		0.650 BSC			0.026 TYP		
К		0.280 TYP			0.0112 TYP		
K1		0.350 TYP			0.014 TYP		
K2		0.200 TYP			0.008 TYP		
K3		0.200 TYP			0.008 TYP		
K4		0.470 TYP			0.0188 TYP		
L	0.200	0.25	0.300	0.008	0.010	0.0121	



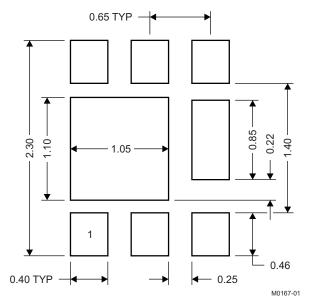
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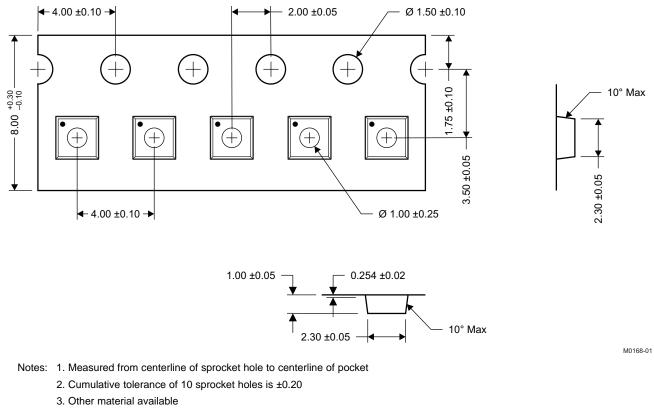
Recommended PCB Pattern



Note: All dimensions are in mm, unless otherwise specified.

For recommended circuit layout for PCB designs, see application note SLPA005 – *Reducing Ringing through PCB Layout Techniques*.

Q2 Tape and Reel Information



- 4. Typical SR of form tape Max 10⁸ OHM/SQ
- 5. All dimensions are in mm, unless otherwise specified.

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REVISION HISTORY

Changes from Original (November 2009) to Revision A	Page
Deleted the Package Marking Information section	
Changes from Revision A (October 2010) to Revision B	Page
Added ESDS statement	



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