1 Orderable parts

The 33910G5 data sheet is within MC33910G5 product specifications - page 3 to page 49
The 33910BAC data sheet is within MC33911BAC product specifications - page 50 to page 95

Table 1. Orderable part variations [(1)]

Device	Temperature	Package	Changes
MC33910G5AC/R2	-40 °C to 125 °C	32 LQFP	• Increase ESD GUN IEC61000-4-2 (gun test contact with 150 pF, 330 Ω test conditions) performance to achieve ±6.0 kV min on the LIN pin. • Immunity against ISO7637 pulse 3b • Reduce EMC emission level on LIN • Improve EMC immunity against RF – target new specification including 3x68 pF • Comply with J2602 conformance test
MC34910G5AC/R2	-40 °C to 85 °C		
MC33910BAC/R2	-40 °C to 125 °C		Initial release
MC34910BAC/R2	-40 °C to 85 °C		

Notes
1. To order parts in Tape & Reel, add the R2 suffix to the part number.

1 MC33910G5 product specifications - page 3 to page 49

2 Internal block diagram

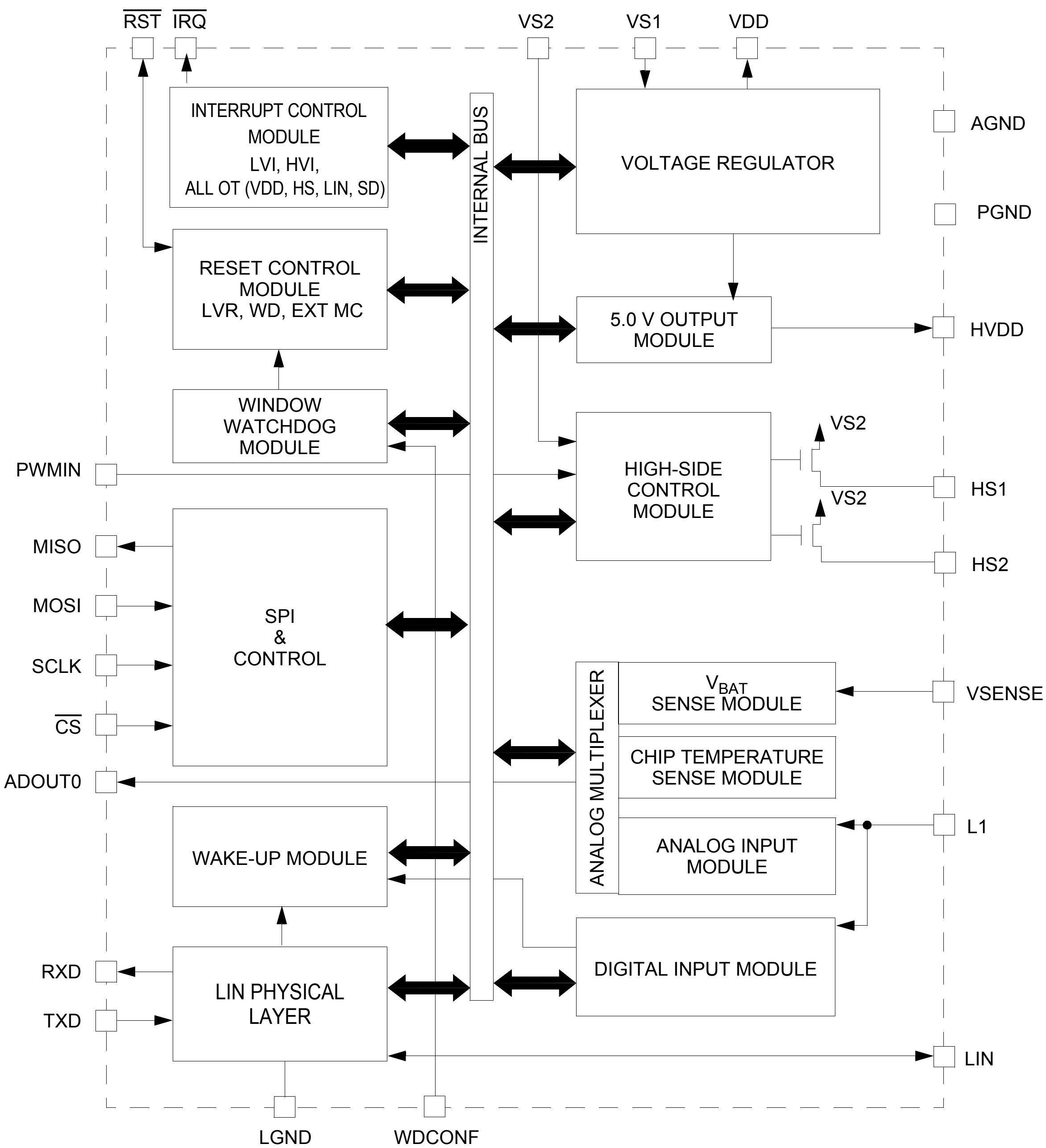


Figure 2. 33910 simplified internal block diagram

3 Pin connections

3.1 Pinout diagram

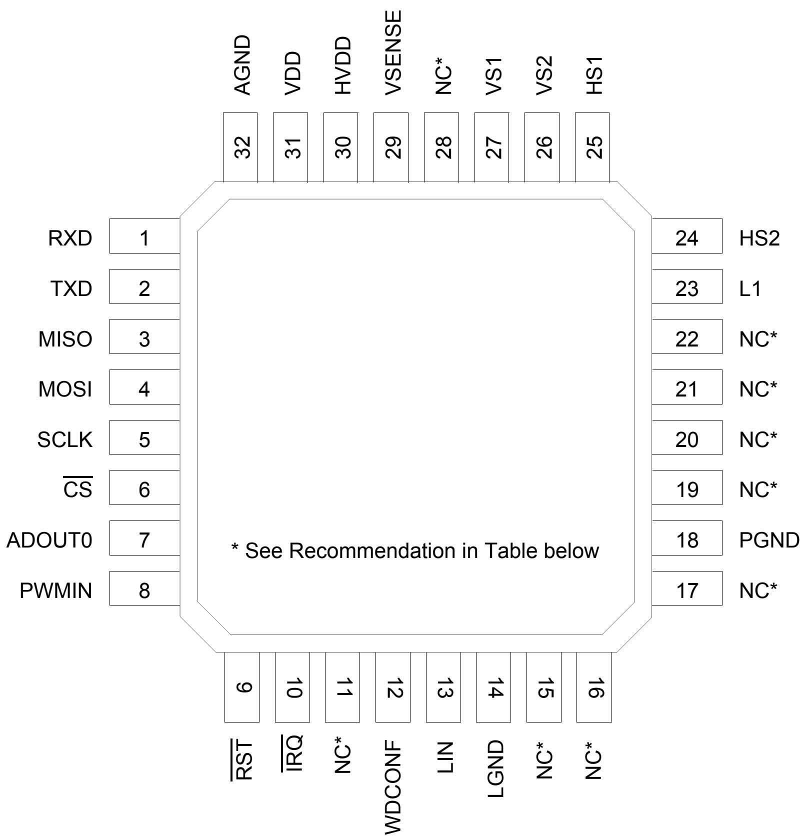


Figure 3. 33910 pin connections

3.2 Pin definitions

A functional description of each pin can be found in the Functional pin description.

Table 2. 33910 pin definitions

Pin	Pin name	Formal name	Definition
1	RXD	Receiver Output	This pin is the receiver output of the LIN interface which reports the state of the bus voltage to the MCU interface.
2	TXD	Transmitter Input	This pin is the transmitter input of the LIN interface which controls the state of the bus output.
3	MISO	SPI Output	SPI (Serial Peripheral Interface) data output. When CS is high, pin is in the high-impedance state.
4	MOSI	SPI Input	SPI (Serial Peripheral Interface) data input.
5	SCLK	SPI Clock	SPI (Serial Peripheral Interface) clock Input.
6	CS	SPI Chip Select	SPI (Serial Peripheral Interface) chip select input pin. CS is active low.
7	ADOUT0	Analog Output Pin 0	Analog Multiplexer Output.
8	PWMIN	PWM Input	High-side Pulse Width Modulation Input.

Table 2. 33910 pin definitions (continued)

Pin	Pin name	Formal name	Definition
9	RST	Internal Reset I/O	Bidirectional Reset I/O pin - driven low when any internal reset source is asserted. $\overline{RST}$ is active low.
10	IRQ	Internal Interrupt Output	Interrupt output pin, indicating wake-up events from Stop modemode or events from Normal and Normal request modes. $\overline{IRQ}$ is active low.
11	NC	Not Connected	This pin must not be connected.
12	WDCONF	Watchdog Configuration Pin	This input pin is for configuration of the watchdog period and allows the disabling of the watchdog.
13	LIN	LIN Bus	This pin represents the single-wire bus transmitter and receiver.
14	LGND	LIN Ground Pin	This pin is the device LIN ground connection. It is internally connected to the PGND pin.
15, 16, 17, 19, 20, 21 & 22	NC	Not Connected	This pin must not be connected or connected to ground.
18	PGND	Power Ground Pin	This pin is the device low-side ground connection. It is internally connected to the LGND pin.
23	L1	Wake-up Input	This pin is the wake-up capable digital input(2). In addition, L1 input can be sensed analog via the analog multiplexer.
24 25	HS2 HS1	High-side Outputs	High-side switch outputs.
26 27	VS2 VS1	Power Supply Pin	These pins are device battery level power supply pins. VS2 is supplying the HSx drivers while VS1 supplies the remaining blocks.(3)
28	NC	Not Connected	This pin can be left opening or connected to any potential ground or power supply
29	VSENSE	Voltage Sense Pin	Battery voltage sense input.(4)
30	HVDD	Hall Sensor Supply Output	+5.0 V switchable supply output pin.(5)
31	VDD	Voltage Regulator Output	+5.0 V main voltage regulator output pin.(6)
32	AGND	Analog Ground Pin	This pin is the device analog ground connection.

Notes

2. When used as digital input, a series 33 kΩ resistor must be used to protect against automotive transients.
3. Reverse battery protection series diodes must be used externally to protect the internal circuitry.
4. This pin can be connected directly to the battery line for voltage measurements. The pin is self protected against reverse battery connections. It is strongly recommended to connect a 10 kΩ resistor in series with this pin for protection purposes.
5. External capacitor (1.0 µF < C < 10 µF; 0.1 Ω < ESR < 5.0 Ω) required.
6. External capacitor (2.0 µF < C < 100 µF; 0.1 Ω < ESR < 10 Ω) required.

4 Electrical characteristics

4.1 Maximum ratings

Table 3. Maximum ratings

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Symbol	Ratings	Value	Unit	Notes
Electrical ratings				
$V_{SUP(SS)}$ $V_{SUP(PK)}$	Supply Voltage at VS1 and VS2 • Normal Operation (DC) • Transient Conditions (load dump)	-0.3 to 27 -0.3 to 40	V	
V_{DD}	Supply Voltage at VDD	-0.3 to 5.5	V	
V_{IN} $V_{IN(IRQ)}$	Input/Output Pins Voltage • $\overline{CS}$, $\overline{RST}$, SCLK, PWMIN, ADOUT0, MOSI, MISO, TXD, RXD, HVDD • Interrupt Pin ($\overline{IRQ}$)	-0.3 to V_{DD} +0.3 -0.3 to 11	V	(7) (8)
V_{HS}	HS1 and HS2 Pin Voltage (DC)	-0.3 to V_{SUP} +0.3	V	
V_{L1DC} V_{L1TR}	L1 Pin Voltage • Normal Operation with a series 33 k resistor (DC) • Transient input voltage with external component (according to ISO7637-2) (See Figure 5)	-18 to 40 ±100	V	
V_{VSENSE}	VSENSE Pin Voltage (DC)	-27 to 40	V	
V_{BUSDC} V_{BUSTR}	LIN Pin Voltage • Normal Operation (DC) • Transient input voltage with external component (according to ISO7637-2) (See Figure 5)	-18 to 40 -150 to 100	V	
I_{VDD}	VDD Output Current	Internally Limited	A	
V_{ESD1-1} V_{ESD1-2} V_{ESD1-3} V_{ESD2-1} V_{ESD2-2} V_{ESD3-1} V_{ESD3-2} V_{ESD3-3} V_{ESD3-4} V_{ESD4-1} V_{ESD4-2} V_{ESD4-3}	ESD Capability • AECQ100 • Human Body Model - JESD22/A114 (C_{ZAP} = 100 pF, R_{ZAP} = 1500 Ω) • LIN Pin • L1 • all other Pins • Charge Device Model - JESD22/C101 (C_{ZAP} = 4.0 pF) • Corner Pins (Pins 1, 8, 9, 16, 17, 24, 25 and 32) • All other Pins (Pins 2-7, 10-15, 18-23, 26-31) • According to LIN Conformance Test Specification / LIN EMC Test Specification, August 2004 (C_{ZAP} = 150 pF, R_{ZAP} = 330 Ω) • Contact Discharge, Unpowered • LIN pin with 220 pF • LIN pin without capacitor • VS1/VS2 (100 nF to ground) • L1 input (33 kΩ serial resistor) • According to IEC 61000-4-2 (C_{ZAP} = 150 pF, R_{ZAP} = 330 Ω) • Unpowered • LIN pin with 220 pF and without capacitor • VS1/VS2 (100 nF to ground) • L1 input (33 kΩ serial resistor)	±8.0 k ±6.0 k ±2000 ±750 ±500 ±20 k ±11 k >±12 k ±6000 ±8000 ±8000 ±8000	V	

Notes
7. Exceeding voltage limits on specified pins may cause a malfunction or permanent damage to the device.
8. Extended voltage range for programming purpose only.

Table 3. Maximum ratings (continued)

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Symbol	Ratings	Value	Unit	Notes
Thermal ratings				
T_A	Operating Ambient Temperature • 33910 • 34910	 -40 to 125 -40 to 85	°C	(9)
T_J	Operating Junction Temperature	-40 to 150	°C	
T_{STG}	Storage Temperature	-55 to 150	°C	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient Natural Convection, Single Layer board (1s) Natural Convection, Four Layer board (2s2p)	 85 56	°C/W	(9), (10) (9), (11)
$R_{\theta JC}$	Thermal Resistance, Junction to Case	23	°C/W	(12)
T_{PPRT}	Peak Package Reflow Temperature During Reflow	Note 14	°C	(13), (14)

Notes

9. Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
10. Per JEDEC JESD51-2 with the single layer board (JESD51-3) horizontal.
11. Per JEDEC JESD51-6 with the board (JESD51-7) horizontal.
12. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
13. Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
14. NXP's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL), go to www.NXP.com, search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts. (i.e. MC33xxxD enter 33xxx), and review parametrics.

4.2 Static electrical characteristics

Table 4. Static electrical characteristics

Characteristics noted under conditions 5.5 V ≤ V_{SUP} ≤ 18 V, -40 °C ≤ T_A ≤ 125 °C for the 33910 and -40 °C ≤ T_A ≤ 85 °C for the 34910, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
Supply voltage range (VS1, VS2)						
V_{SUP}	Nominal Operating Voltage	5.5	–	18	V	
V_{SUPOP}	Functional Operating Voltage	–	–	27	V	(15)
V_{SUPLD}	Load Dump	–	–	40	V	
Supply current range (V_{SUP} = 13.5 V)						
I_{RUN}	Normal Mode (I_{OUT} at V_{DD} = 10 mA), LIN Recessive State	–	4.5	10	mA	(16)
I_{STOP}	Stop Mode, VDD ON with I_{OUT} = 100 µA, LIN Recessive State • 5.5 V < V_{SUP} < 12 V • V_{SUP} = 13.5 V • 13.5 V < V_{SUP} < 18 V	 – – –	 47 62 180	 80 90 400	µA	(16), (17), (18), (19)
I_{SLEEP}	Sleep Mode, VDD OFF, LIN Recessive State • 5.5 V < V_{SUP} < 12 V • V_{SUP} = 13.5 V • 13.5 V ≤ V_{SUP} < 18 V	 – – –	 27 33 160	 35 48 300	µA	(16), (18)
I_{CYCLIC}	Cyclic Sense Supply Current Adder	–	10	–	µA	(20)
Supply under/overvoltage detections						
$V_{BATFAIL}$ $V_{BATFAIL\_HYS}$	Power-On Reset (BATFAIL) • Threshold (measured on VS1) • Hysteresis (measured on VS1)	 1.5 –	 3.0 0.9	 3.9 –	V	(21), (20)
V_{SUV} V_{SUV_HYS}	V_{SUP} Undervoltage Detection (VSUV Flag) (Normal and Normal Request Modes, Interrupt Generated) • Threshold (measured on VS1) • Hysteresis (measured on VS1)	 5.55 –	 6.0 0.2	 6.6 –	V	
V_{SOV} V_{SOV_HYS}	V_{SUP} Overvoltage Detection (VSOV Flag) (Normal and Normal Request Modes, Interrupt Generated) • Threshold (measured on VS1) • Hysteresis (measured on VS1)	 18 –	 19.25 1.0	 20.5 –	V	

Notes

15. Device is fully functional. All features are operating.
16. Total current (I_{VS1} + I_{VS2}) measured at GND pins excluding all loads, cyclic sense disabled.
17. Total I_{DD} current (including loads) below 100 µA.
18. Stop and Sleep modes current increases if V_{SUP} exceeds13.5 V.
19. This parameter is guaranteed after 90 ms.
20. This parameter is guaranteed by process monitoring but not production tested.
21. The Flag is set during power up sequence. To clear the flag, a SPI read must be performed.

Table 4. Static electrical characteristics (continued)

Characteristics noted under conditions 5.5 V ≤ V_{SUP} ≤ 18 V, -40 °C ≤ T_A ≤ 125 °C for the 33910 and -40 °C ≤ T_A ≤ 85 °C for the 34910, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
Voltage regulator (22) (VDD)						
V_{DDRUN}	Normal Mode Output Voltage • 1.0 mA < I_{VDD} < 50 mA; 5.5 V < V_{SUP} < 27 V	4.75	5.00	5.25	V	
I_{VDDRUN}	Normal Mode Output Current Limitation	60	110	200	mA	
V_{DDDROP}	Dropout Voltage • I_{VDD} = 50 mA	–	0.1	0.25	V	(23)
V_{DDSTOP}	Stop Mode Output Voltage • I_{VDD} < 5.0 mA	4.75	5.0	5.25	V	
$I_{VDDSTOP}$	Stop Mode Output Current Limitation	6.0	13	36	mA	
LR_{RUN} LR_{STOP}	Line Regulation • Normal mode, 5.5 V < V_{SUP} < 18 V; I_{VDD} = 10 mA • Stop mode, 5.5 V < V_{SUP} < 18 V; I_{VDD} = 1.0 mA	– –	– –	25 25	mV	
LD_{RUN} LD_{STOP}	Load Regulation • Normal mode, 1.0 mA < I_{VDD} < 50 mA • Stop mode, 0.1 mA < I_{VDD} < 5.0 mA	– –	– –	80 50	mV	
T_{PRE}	Overtemperature Prewarning (Junction) • Interrupt generated, VDDOT Bit Set	90	115	140	°C	(24)
T_{PRE_HYS}	Overtemperature Prewarning Hysteresis	–	13	–	°C	(24)
T_{SD}	Overtemperature Shutdown Temperature (Junction)	150	170	190	°C	(24)
T_{SD_HYS}	Overtemperature Shutdown Hysteresis	–	13	–	°C	(24)
Hall sensor supply output (25) (HVDD)						
H_{VDDACC}	V_{DD} Voltage matching H_{VDDACC} = (HVDD-VDD) / VDD * 100% • I_{HVDD} = 15 mA	-2.0	–	2.0	%	
I_{HVDD}	Current Limitation	20	35	50	mA	
$H_{VDDDROP}$	Dropout Voltage • I_{HVDD} = 15 mA; I_{VDD} = 5.0 mA	–	160	300	mV	
LR_{HVDD}	Line Regulation • I_{HVDD} = 5.0 mA; I_{VDD} = 5.0 mA	–	–	40	mV	
LD_{HVDD}	Load Regulation • 1.0 mA > I_{HVDD} > 15 mA; I_{VDD} = 5.0 mA	–	–	20	mV	

Notes
22. Specification with external capacitor 2.0 μF < C < 100 μF and 100 mΩ ≤ ESR ≤ 10 Ω.
23. Measured when voltage has dropped 250 mV below its nominal Value (5.0 V).
24. This parameter is guaranteed by process monitoring but not production tested.
25. Specification with external capacitor 1.0 μF < C < 10 μF and 100 mΩ ≤ ESR ≤ 10 Ω.

Table 4. Static electrical characteristics (continued)

Characteristics noted under conditions 5.5 V ≤ V_{SUP} ≤ 18 V, -40 °C ≤ T_A ≤ 125 °C for the 33910 and -40 °C ≤ T_A ≤ 85 °C for the 34910, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
$\overline{RST}$ input/output pin ($\overline{RST}$)						
$V_{\overline{RST}TH}$	VDD Low Voltage Reset Threshold	4.3	4.5	4.7	V	
V_{OL}	Low-state Output Voltage • I_{OUT} = 1.5 mA; 3.5 V ≤ V_{SUP} ≤ 27 V	0.0	–	0.9	V	
I_{OH}	High-state Output Current (0 V < V_{OUT} < 3.5 V)	-150	-250	-350	µA	
I_{PD_MAX}	Pull-down Current Limitation (internally limited) V_{OUT} = V_{DD}	1.5	–	8.0	mA	
V_{IL}	Low-state Input Voltage	-0.3	–	0.3 x V_{DD}	V	
V_{IH}	High-state Input Voltage	0.7 x V_{DD}	–	V_{DD} +0.3	V	
MISO SPI output pin (MISO)						
V_{OL}	Low-state Output Voltage • I_{OUT} = 1.5 mA	0.0	–	1.0	V	
V_{OH}	High-state Output Voltage • I_{OUT} = -250 µA	V_{DD} -0.9	–	V_{DD}	V	
$I_{TRIMISO}$	Tri-state Leakage Current • 0 V ≤ V_{MISO} ≤ V_{DD}	-10	–	10	µA	
SPI input pins (MOSI, SCLK, $\overline{CS}$)						
V_{IL}	Low-state Input Voltage	-0.3	–	0.3 x V_{DD}	V	
V_{IH}	High-state Input Voltage	0.7 x V_{DD}	–	V_{DD} +0.3	V	
I_{IN}	MOSI, SCLK Input Current • 0 V ≤ V_{IN} ≤ V_{DD}	-10	–	10	µA	
$I_{PU\overline{CS}}$	$\overline{CS}$ Pull-up Current • 0 V < V_{IN} < 3.5 V	10	20	30	µA	
Interrupt output pin ($\overline{IRQ}$)						
V_{OL}	Low-state Output Voltage • I_{OUT} = 1.5 mA	0.0	–	0.8	V	
V_{OH}	High-state Output Voltage • I_{OUT} = -250 µA	V_{DD} -0.8	–	V_{DD}	V	
I_{OUT}	Leakage Current • V_{DD} ≤ V_{OUT} ≤ 10 V	–	–	2.0	mA	
Pulse width modulation input pin (PWMIN)						
V_{IL}	Low-state Input Voltage	-0.3	–	0.3 x V_{DD}	V	
V_{IH}	High-state Input Voltage	0.7 x V_{DD}	–	V_{DD} +0.3	V	
$I_{PUPWMIN}$	Pull-up current • 0 V < V_{IN} < 3.5 V	10	20	30	µA	

Table 4. Static electrical characteristics (continued)

Characteristics noted under conditions 5.5 V ≤ V_{SUP} ≤ 18 V, -40 °C ≤ T_A ≤ 125 °C for the 33910 and -40 °C ≤ T_A ≤ 85 °C for the 34910, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
High-side outputs HS1 and HS2 pins (HS1, HS2)						
$R_{DS(on)}$	Output Drain-to-Source On Resistance • T_J = 25 °C, I_{LOAD} = 50 mA; V_{SUP} > 9.0 V • T_J = 150 °C, I_{LOAD} = 50 mA; V_{SUP} > 9.0 V • T_J = 150 °C, I_{LOAD} = 30 mA; 5.5 V < V_{SUP} < 9.0 V	– – –	– – –	7.0 10 14	Ω	 (26) (26)
I_{LIMHSX}	Output Current Limitation • 0 V < V_{OUT} < V_{SUP} - 2.0 V	60	90	250	mA	(27)
I_{OLHSX}	Open Load Current Detection	–	5.0	7.5	mA	(28)
I_{LEAK}	Leakage Current • -0.2 V < V_{HSX} < V_{S2} + 0.2 V	–	–	10	µA	
V_{THSC}	Short-circuit Detection Threshold • 5.5 V < V_{SUP} < 27 V	V_{SUP} -2.0	–	–	V	(29)
T_{HSSD}	Overtemperature Shutdown	140	160	180	°C	(30), (31)
T_{HSSD_HYS}	Overtemperature Shutdown Hysteresis	–	10	–	°C	(31)
L1 input pin (L1)						
V_{THL}	Low Detection Threshold • 5.5 V < V_{SUP} < 27 V	2.0	2.5	3.0	V	(32)
V_{THH}	High Detection Threshold • 5.5 V < V_{SUP} < 27 V	3.0	3.5	4.0	V	(32)
V_{HYS}	Hysteresis • 5.5 V < V_{SUP} < 27 V	0.4	0.8	1.4	V	(32)
I_{IN}	Input Current • -0.2 V < V_{IN} < VS1	-10	–	10	µA	(33)
R_{L1IN}	Analog Input Impedance	800	1300	2000	kΩ	(34)
$RATIO_{L1}$	Analog Input Divider Ratio ($RATIO_{L1}$ = V_{L1} / V_{ADOUT0}) • L1DS (L1 Divider Select) = 0 • L1DS (L1 Divider Select) = 1	0.95 3.42	1.0 3.6	1.05 3.78		
$V_{RATIOL1-OFFSET}$	Analog Output Offset Ratio • L1DS (L1 Divider Select) = 0 • L1DS (L1 Divider Select) = 1	-80 -22	6.0 2.0	80 22	mV	
$L1_{MATCHING}$	Analog Inputs Matching • L1DS (L1 Divider Select) = 0 • L1DS (L1 Divider Select) = 1	96 96	100 100	104 104	%	

Notes

26. This parameter is production tested up to T_A = 125 °C, and guaranteed by process monitoring up to T_J = 150 °C.
27. When overcurrent occurs, the corresponding high-side stays ON with limited current capability and the HSxCL flag is set in the HSSR.
28. When open load occurs, the flag (HSxOP) is set in the HSSR.
29. HS automatically shutdown if HSOT occurs or if the HVSE flag is enabled and an overvoltage occurs.
30. When overtemperature shutdown occurs, both high-sides are turned off. All flags in HSSR are set.
31. Guaranteed by characterization but not production tested
32. If L1 pin is unused it must be connected to ground.
33. Analog multiplexer input disconnected from L1 input pin.
34. Analog multiplexer input connected to L1 input pin.

Table 4. Static electrical characteristics (continued)

Characteristics noted under conditions 5.5 V ≤ V_{SUP} ≤ 18 V, -40 °C ≤ T_A ≤ 125 °C for the 33910 and -40 °C ≤ T_A ≤ 85 °C for the 34910, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
Window watchdog configuration pin (WDCONF) [35]						
R_{EXT}	External Resistor Range	20	–	200	kΩ	
WD_{ACC}	Watchdog Period Accuracy with External Resistor (Excluding Resistor Accuracy)	-15	–	15	%	[36]
Analog multiplexer						
V_{ADOUT0_TEMP}	Temperature Sense Analog Output Voltage • T_A = -40 °C • T_A = 25 °C • T_A = 125 °C	 2.0 2.8 3.6	 - 3.0 -	 2.8 3.6 4.6	V	
V_{ADOUT0_25}	Temperature Sense Analog Output Voltage per characterization • T_A = 25 °C	3.1	3.15	3.2	V	[37]
S_{TTOV}	Internal Chip Temperature Sense Gain	9.0	10.5	12	mV/K	
S_{TTOV_3T}	Internal Chip Temperature Sense Gain per characterization at three temperatures. See Figure 16, Temperature sense gain	9.9	10.2	10.5	mV/K	[37]
$RATIO_{VSENSE}$	VSENSE Input Divider Ratio ($RATIO_{VSENSE} = V_{VSENSE} / V_{ADOUT0}$) • 5.5 V < V_{SUP} < 27 V	5.0	5.25	5.5		
$RATIO_{VSENSECZ}$	VSENSE Input Divider Ratio (RATIOVSENSE=Vsense/Vadout0) per characterization • 5.5 <Vsup< 27 V	5.15	5.25	5.35		[37]
$OFFSET_{VSENSE}$	VSENSE Output Related Offset	-30	-10	30	mV	
$OFFSET_{VSENSE\_CZ}$	VSENSE Output Related Offset per characterization	-30	-12.6	0	mV	[37]
Analog output (ADOUT0)						
V_{OUT_MAX}	Maximum Output Voltage • -5.0 mA < I_O < 5.0 mA	V_{DD} -0.35	–	V_{DD}	V	
V_{OUT_MIN}	Minimum Output Voltage • -5.0 mA < I_O < 5.0 mA	0.0	–	0.35	V	
RxD output pin (LIN physical layer) (RxD)						
V_{OL}	Low-state Output Voltage • I_{OUT} = 1.5 mA	0.0	–	0.8	V	
V_{OH}	High-state Output Voltage • I_{OUT} = -250 µA	V_{DD} -0.8	–	V_{DD}	V	

Notes

35. For V_{SUP} 4.7 V to 18 V
36. Watchdog timing period calculation formula: t_{PWD} [ms] = [0.466 * (R_{EXT} - 20)] + 10 with (R_{EXT} in kΩ)
37. These limits have been defined after laboratory characterization on 3 lots and 30 samples. These tighten limits could not be guaranteed by production test.

Table 4. Static electrical characteristics (continued)

Characteristics noted under conditions 5.5 V ≤ V_{SUP} ≤ 18 V, -40 °C ≤ T_A ≤ 125 °C for the 33910 and -40 °C ≤ T_A ≤ 85 °C for the 34910, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
TXD input pin (LIN physical layer) (TXD)						
V_{IL}	Low-state Input Voltage	-0.3	–	0.3 x V_{DD}	V	
V_{IH}	High-state Input Voltage	0.7 x V_{DD}	–	V_{DD} +0.3	V	
I_{PUIN}	Pin Pull-up Current, 0 V < V_{IN} < 3.5 V	10	20	30	µA	
LIN physical layer with J2602 feature enabled (bit DIS_J2602 = 0)						
$V_{TH\_UNDER\_VOLTAGE}$	LIN Undervoltage threshold • Positive and Negative threshold (V_{THP}, V_{THN})	5.0		6.0	V	
V_{J2602_DEG}	Hysteresis (V_{THP} - V_{THN})		400		mV	
LIN physical layer, transceiver (LIN)(38)						
V_{BAT}	Operating Voltage Range	8.0		18	V	
V_{SUP}	Supply Voltage Range	7.0		18	V	
$V_{SUP\_NON\_OP}$	Voltage Range within which the device is not destroyed	-0.3		40	V	
I_{BUS_LIM}	Current Limitation for Driver Dominant State • Driver ON, V_{BUS} = 18 V	40	90	200	mA	
$I_{BUS\_PAS\_DOM}$	Input Leakage Current at the receiver • Driver off; V_{BUS} = 0 V; V_{BAT} = 12 V	-1.0	–	–	mA	
$I_{BUS\_PAS\_REC}$	Leakage Output Current to GND • Driver Off; 8.0 V < V_{BAT} < 18 V; 8.0 V < V_{BUS} < 18 V; V_{BUS} ≥ V_{BAT}	–	–	20	µA	
$I_{BUS\_NO\_GND}$	Control Unit Disconnected from Ground • GND_{DEVICE} = V_{SUP}; V_{BAT} = 12 V; 0 < V_{BUS} < 18 V	-1.0	–	1.0	mA	(39)
I_{BUSNO_BAT}	V_{BAT} Disconnected; V_{SUP_DEVICE} = GND; 0 V < V_{BUS} < 18 V	–	–	100	µA	(40)
V_{BUSDOM}	Receiver Dominant State	–	–	0.4	V_{SUP}	
V_{BUSREC}	Receiver Recessive State	0.6	–	–	V_{SUP}	
V_{BUS_CNT}	Receiver Threshold Center • (V_{TH_DOM} + V_{TH_REC})/2	0.475	0.5	0.525	V_{SUP}	
V_{HYS}	Receiver Threshold Hysteresis • (V_{TH_REC} - V_{TH_DOM})	–	–	0.175	V_{SUP}	
$V_{SERDIODE}$	Voltage Drop at the Serial Diode in Pull-up Path	0.4		1.0	V	
V_{SHIFT_BAT}	VBAT_SHIFT	0		11.5%	V_{BAT}	
V_{SHIFT_GND}	GND_SHIFT	0		11.5%	V_{BAT}	

Notes

38. Parameters guaranteed for 7.0 V ≤ V_{SUP} ≤ 18 V.
39. Loss of local ground must not affect communication in the residual network.
40. Node has to sustain the current which can flow under this condition. Bus must remain operational under this condition.

Table 4. Static electrical characteristics (continued)

Characteristics noted under conditions 5.5 V ≤ V_{SUP} ≤ 18 V, -40 °C ≤ T_A ≤ 125 °C for the 33910 and -40 °C ≤ T_A ≤ 85 °C for the 34910, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
LIN physical layer, transceiver (LIN) (continued)[38]						
V_{BUSWU}	LIN Wake-up threshold from Stop or Sleep Mode		5.3	5.8	V	(41)
R_{SLAVE}	LIN Pull-up Resistor to V_{SUP}	20	30	60	kΩ	
T_{LINSD}	Overtemperature Shutdown	140	160	180	°C	(42)
T_{LINSD_HYS}	Overtemperature Shutdown Hysteresis	–	10	–	°C	

Notes

41. This parameter is 100% tested on an Automatic Tester. However, since it has not been monitored during reliability stresses, NXP does not guarantee this parameter during the product's life time.
42. When overtemperature shutdown occurs, the LIN bus goes in recessive state and the flag LINOT in LINSR is set.

4.3 Dynamic electrical characteristics

Table 5. Dynamic electrical characteristics

Characteristics noted under conditions 5.5 V ≤ V_{SUP} ≤ 18 V, -40 °C ≤ T_A ≤ 125 °C for the 33910 and -40 °C ≤ T_A ≤ 85 °C for the 34910, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
SPI interface timing (see Figure 13)						
f_{SPIOP}	SPI Operating Frequency	–	–	4.0	MHz	
t_{PSCLK}	SCLK Clock Period	250	–	N/A	ns	
t_{WSCLKH}	SCLK Clock High Time	110	–	N/A	ns	(43)
t_{WSCLKL}	SCLK Clock Low Time	110	–	N/A	ns	(43)
t_{LEAD}	Falling Edge of $\overline{CS}$ to Rising Edge of SCLK	100	–	N/A	ns	(43)
t_{LAG}	Falling Edge of SCLK to $\overline{CS}$ Rising Edge	100	–	N/A	ns	(43)
t_{SISU}	MOSI to Falling Edge of SCLK	40	–	N/A	ns	(43)
t_{SIH}	Falling Edge of SCLK to MOSI	40	–	N/A	ns	(43)
t_{RSO}	MISO Rise Time • C_L = 220 pF	–	40	–	ns	(43)
t_{FSO}	MISO Fall Time • C_L = 220 pF	–	40	–	ns	(43)
t_{SOEN} t_{SODIS}	Time from Falling or Rising Edges of $\overline{CS}$ to: • MISO Low-impedance • MISO High-impedance	0.0 0.0	– –	50 50	ns	(43)
t_{VALID}	Time from Rising Edge of SCLK to MISO Data Valid • 0.2 x V_{DD} ≤ MISO ≥ 0.8 x V_{DD}, C_L = 100 pF	0.0	–	75	ns	(43)
$\overline{RST}$ output pin						
$t_{\overline{RST}}$	Reset Low-level Duration After V_{DD} High (see Figure 12)	0.65	1.0	1.35	ms	
$t_{\overline{RSTDF}}$	Reset Deglitch Filter Time	350	480	900	ns	
Window watchdog configuration pin (WDCONF)						
t_{PWD}	Watchdog Time Period • External Resistor R_{EXT} = 20 kΩ (1%) • External Resistor R_{EXT} = 200 kΩ (1%) • Without External Resistor R_{EXT} (WDCONF Pin Open)	8.5 79 110	10 94 150	11.5 108 205	ms	(44)

Notes

43. This parameter is guaranteed by process monitoring but not production tested.
44. Watchdog timing period calculation formula: t_{PWD} [ms] = [0.466 * (R_{EXT} - 20)] + 10 with (R_{EXT} in kΩ)

Table 5. Dynamic electrical characteristics (continued)

Characteristics noted under conditions 5.5 V ≤ V_{SUP} ≤ 18 V, -40 °C ≤ T_A ≤ 125 °C for the 33910 and -40 °C ≤ T_A ≤ 85 °C for the 34910, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
L1 input						
t_{WUF}	L1 Filter Time Deglitcher	8.0	20	38	µs	(45)
State machine timing						
t_{STOP}	Delay Between $\overline{CS}$ LOW-to-HIGH Transition (at End of SPI Stop Command) and Stop Mode Activation	–	–	5.0	µs	(45)
t_{NRTOUT}	Normal Request Mode Timeout (see Figure 12)	110	150	205	ms	
T_{ON}	Cyclic Sense ON Time from Stop and Sleep Mode	130	200	270	µs	(46)
	Cyclic Sense Accuracy	-35		+35	%	(45)
t_{S-ON}	Delay Between SPI Command and HS Turn On • 9.0 V < V_{SUP} < 27 V	–	–	10	µs	(47)
t_{S-OFF}	Delay Between SPI Command and HS Turn Off • 9.0 V < V_{SUP} < 27 V	–	–	10	µs	(47)
t_{SNR2N}	Delay Between Normal Request and Normal Mode After a Watchdog Trigger Command (Normal Request Mode)	–	–	10	µs	(45)
$t_{WU\overline{CS}}$ t_{WUSPI}	Delay Between $\overline{CS}$ Wake-up ($\overline{CS}$ LOW to HIGH) in Stop Mode and: • Normal Request mode, VDD ON and $\overline{RST}$ HIGH • First Accepted SPI Command	9.0 90	15 —	80 N/A	µs	
$t_{2\overline{CS}}$	Minimum Time Between Rising and Falling Edge on the $\overline{CS}$	4.0	—	—	µs	
J2602 deglitcher						
t_{J2602_DEG}	V_{SUP} Deglitcher • (DIS_J2602 = 0)	35	50	70	µs	(48)
LIN physical layer: driver characteristics for normal slew rate - 20.0 kBit/sec according to LIN physical layer specification(49), (50)						
D1	Duty Cycle 1: • $TH_{REC(MAX)}$ = 0.744 * V_{SUP} • $TH_{DOM(MAX)}$ = 0.581 * V_{SUP} • D1 = $t_{BUS\_REC(MIN)}/(2 \times t_{BIT})$, t_{BIT} = 50 µs, 7.0 V ≤ V_{SUP} ≤ 18 V	0.396	—	—		
D2	Duty Cycle 2: • $TH_{REC(MIN)}$ = 0.422 * V_{SUP} • $TH_{DOM(MIN)}$ = 0.284 * V_{SUP} • D2 = $t_{BUS\_REC(MAX)}/(2 \times t_{BIT})$, t_{BIT} = 50 µs, 7.6 V ≤ V_{SUP} ≤ 18 V	—	—	0.581		

Notes

45. This parameter is guaranteed by process monitoring but not production tested.
46. This parameter is 100% tested on an Automatic Tester. However, since it has not been monitored during reliability stresses, NXP does not guarantee this parameter during the product's life time.
47. Delay between turn on or off command (rising edge on $\overline{CS}$) and HS ON or OFF, excluding rise or fall time due to external load.
48. This parameter has not been monitoring during operating life test.
49. Bus load R_{BUS} and C_{BUS} 1.0 nF / 1.0 kΩ, 6.8 nF / 660 Ω, 10 nF / 500 Ω. Measurement thresholds: 50% of TXD signal to LIN signal threshold defined at each parameter. See Figure 6.
50. See Figure 7.

Table 5. Dynamic electrical characteristics (continued)

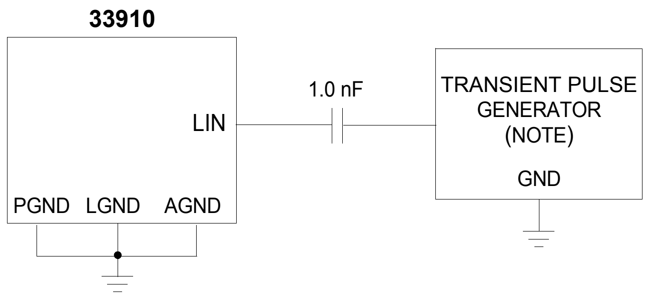
Characteristics noted under conditions 5.5 V ≤ V_{SUP} ≤ 18 V, -40 °C ≤ T_A ≤ 125 °C for the 33910 and -40 °C ≤ T_A ≤ 85 °C for the 34910, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
LIN physical layer: driver characteristics for slow slew rate - 10.4 kBit/sec according to LIN physical layer specification (51), (52)						
D3	Duty Cycle 3: • $TH_{REC(MAX)}$ = 0.778 * V_{SUP} • $TH_{DOM(MAX)}$ = 0.616 * V_{SUP} • D3 = $t_{BUS\_REC(MIN)}$/(2 x t_{BIT}), t_{BIT} = 96 µs, 7.0 V ≤ V_{SUP} ≤ 18 V	0.417	—	—		
D4	Duty Cycle 4: • $TH_{REC(MIN)}$ = 0.389 * V_{SUP} • $TH_{DOM(MIN)}$ = 0.251 * V_{SUP} • D4 = $t_{BUS\_REC(MAX)}$/(2 x t_{BIT}), t_{BIT} = 96 µs, 7.6 V ≤ V_{SUP} ≤ 18 V	—	—	0.590		
LIN physical layer: driver characteristics for fast slew rate						
SR_{FAST}	LIN Fast Slew Rate (Programming Mode)	—	20	—	V/µs	
LIN physical layer: characteristics and wake-up timings (53)						
t_{REC_PD} t_{REC_SYM}	Propagation Delay and Symmetry • Propagation Delay of Receiver, t_{REC_PD}=MAX (t_{REC_PDR}, t_{REC_PDF}) • Symmetry of Receiver Propagation Delay, t_{REC_PDF} - t_{REC_PDR}	— -2.0	4.2 —	6.0 2.0	µs	(54)
t_{PROPWL}	Bus Wake-Up Deglitcher (Sleep and Stop modes)	42	70	95	µs	(55), (59), (56)
t_{WAKE_SLEEP} t_{WAKE_STOP}	Bus Wake-Up Event Reported • From Sleep mode • From Stop mode	— 9.0	— 27	1500 35	µs	(57) (58)
t_{TXDDOM}	TXD Permanent Dominant State Delay	0.65	1.0	1.35	s	
Pulse width modulation input pin (PWMIN)						
f_{PWMIN}	PWMIN pin • Max. frequency to drive HS output pins	—	10	—	kHz	(59)

Notes

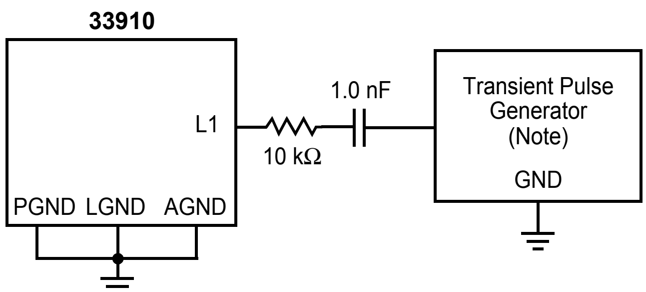
51. Bus load R_{BUS} and C_{BUS} 1.0 nF / 1.0 kΩ, 6.8 nF / 660 Ω, 10 nF / 500 Ω. Measurement thresholds: 50% of TXD signal to LIN signal threshold defined at each parameter. See Figure 6.
52. See Figure 8.
53. V_{SUP} from 7.0 to 18 V, bus load R_{BUS} and C_{BUS} 1.0 nF / 1.0 kΩ, 6.8 nF / 660 Ω, 10 nF / 500 Ω. Measurement thresholds: 50% of TXD signal to LIN signal threshold defined at each parameter. See Figure 6.
54. See Figure 9.
55. See Figure 10, for Sleep and Figure 11, for Stop mode.
56. This parameter is tested on automatic tester but has not been monitoring during operating life test.
57. The measurement is done with 1.0 µF capacitor and 0 mA current load on V_{DD}. The value takes into account the delay to charge the capacitor. The delay is measured between the bus wake-up threshold (V_{BUSWU}) rising edge of the LIN bus and when V_{DD} reaches 3.0 V. See Figure 10. The delay depends of the load and capacitor on V_{DD}.
58. In Stop mode, the delay is measured between the bus wake-up threshold (V_{BUSWU}) and the falling edge of the $\overline{IRQ}$ pin. See Figure 11.
59. This parameter is guaranteed by process monitoring but not production tested.

4.4 Timing diagrams



Note Waveform per ISO 7637-2. Test Pulses 1, 2, 3a, 3b.

Figure 4. Test circuit for transient test pulses (LIN)



Note Waveform per ISO 7637-2. Test Pulses 1, 2, 3a, 3b,.

Figure 5. Test circuit for transient test pulses (L1)

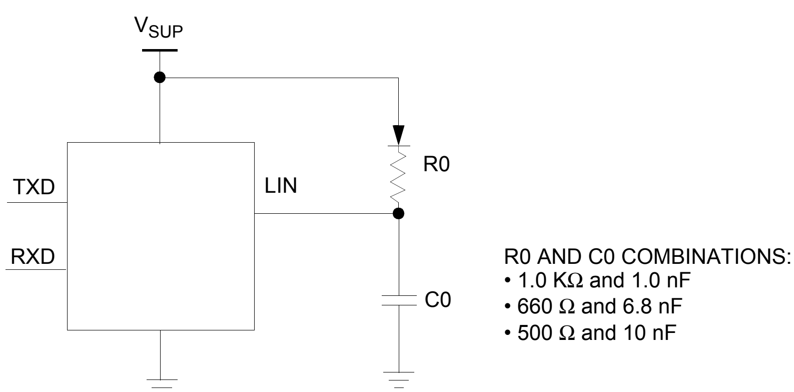


Figure 6. Test circuit for LIN timing measurements

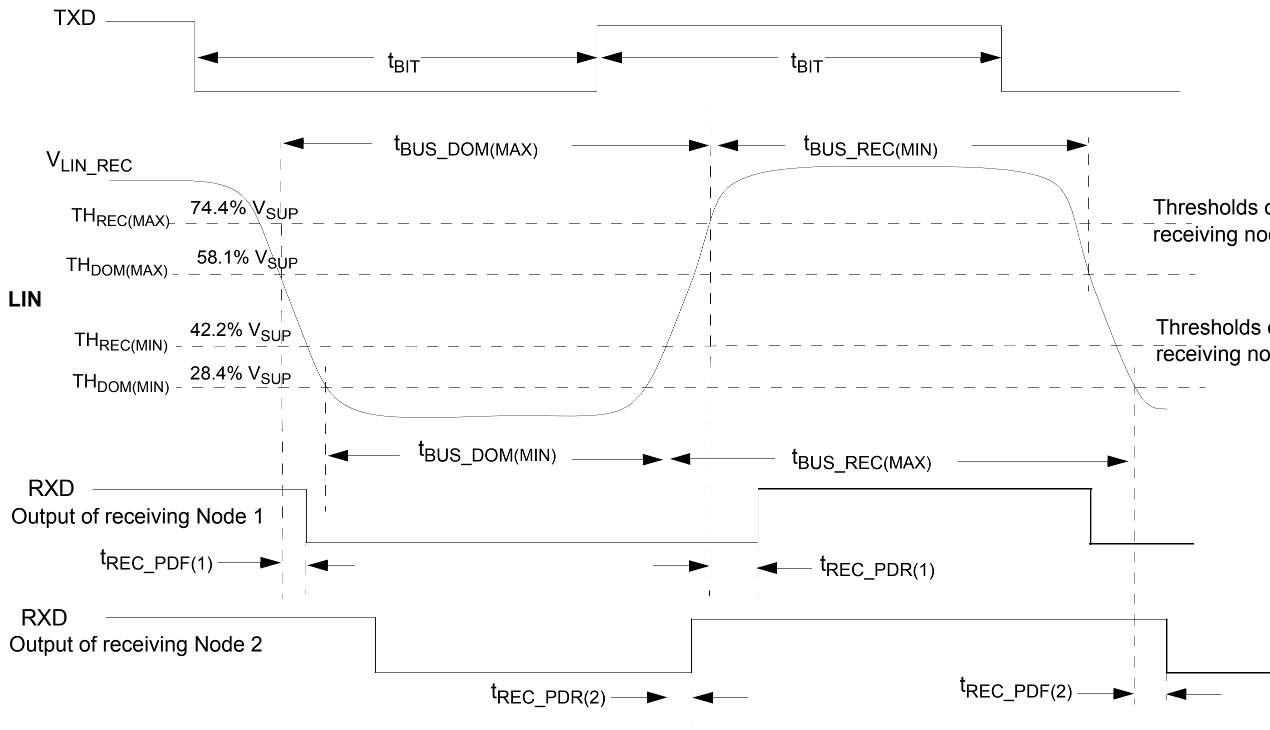


Figure 7. LIN timing measurements for normal slew rate

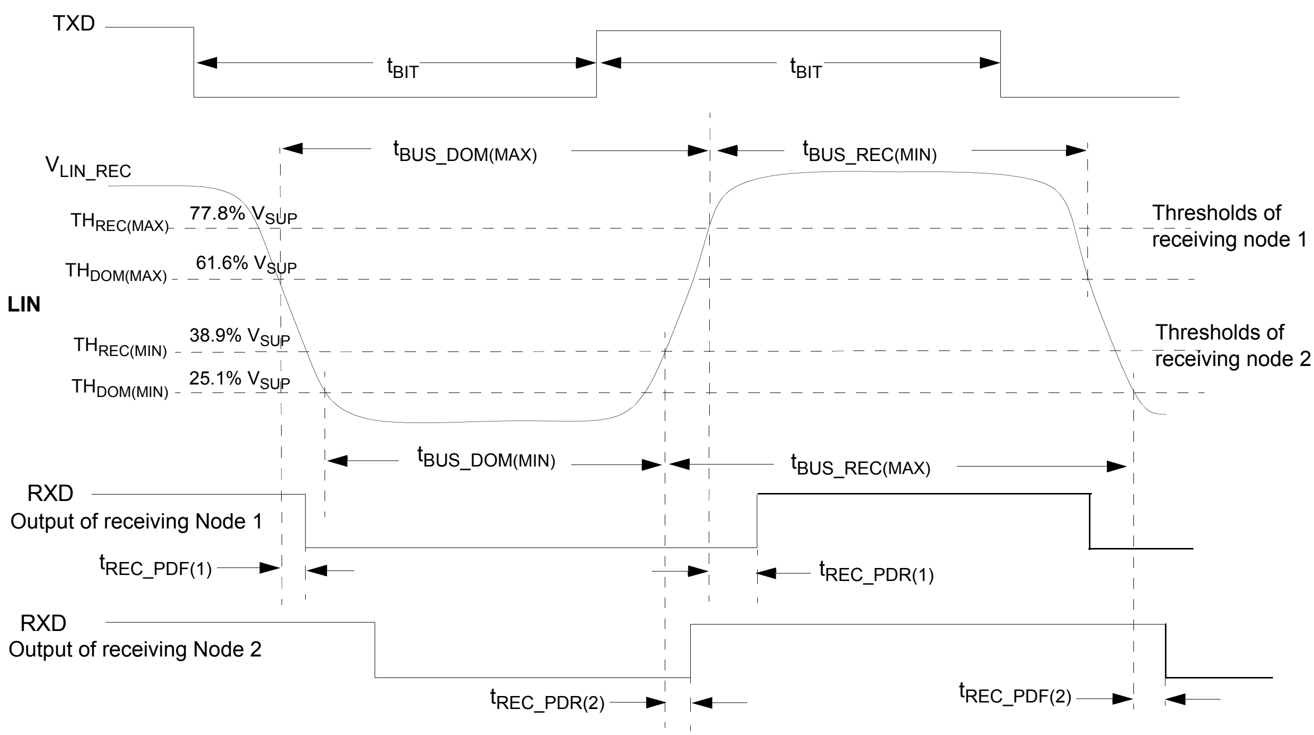


Figure 8. LIN timing measurements for slow slew rate

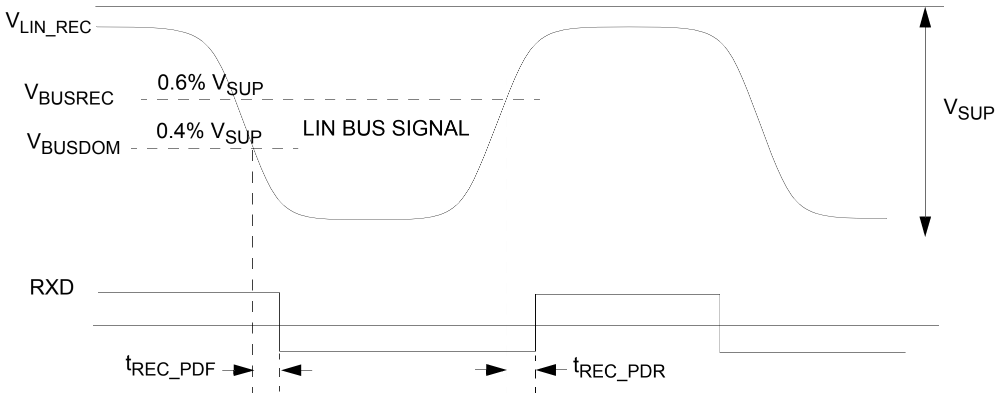


Figure 9. LIN receiver timing

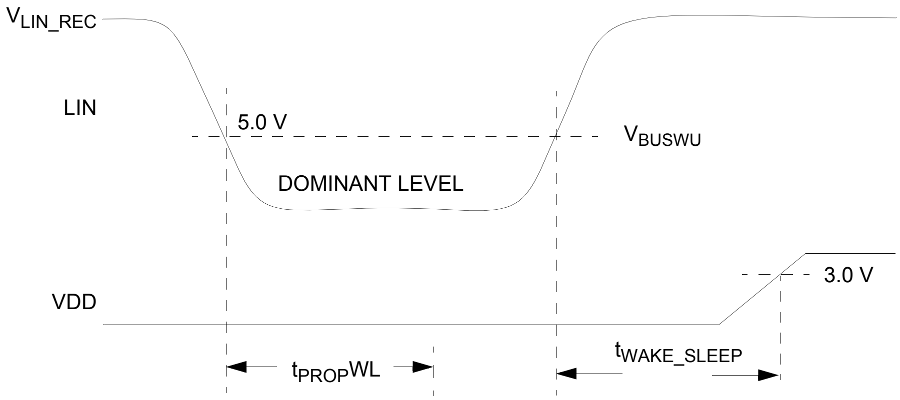


Figure 10. LIN wake-up sleep mode timing

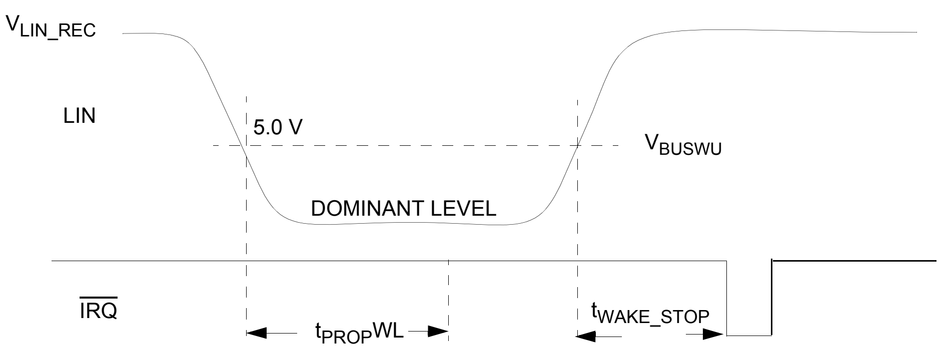


Figure 11. LIN wake-up stop mode timing

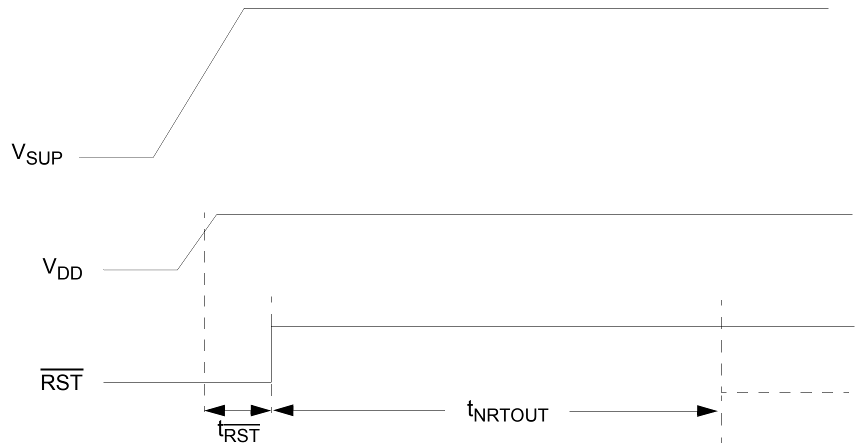


Figure 12. Power on reset and normal request timeout timing

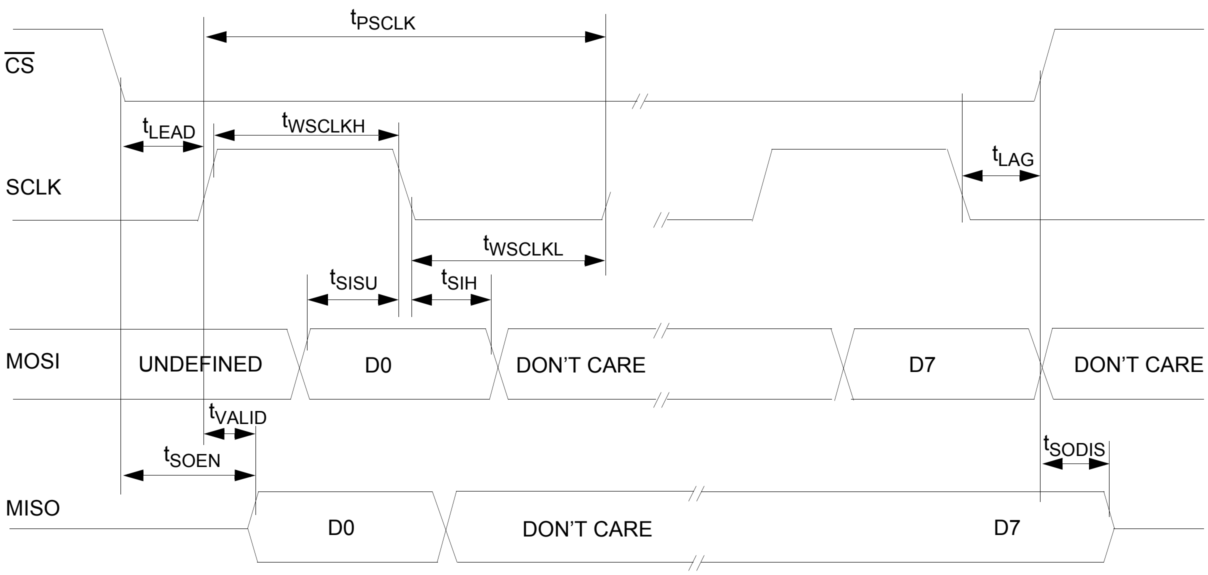


Figure 13. SPI timing characteristics

5 Functional description

5.1 Introduction

The 33910 was designed and developed as a highly integrated and cost-effective solution for automotive and industrial applications. For automotive body electronics, the 33910 is well suited to perform keypad applications via the LIN bus. Power switches are provided on the device configured as high-side outputs. Other ports are also provided, which include a Hall Sensor port supply, and one wake-up capable pin. An internal voltage regulator provides power to a MCU device. Also included in this device is a LIN physical layer, which communicates using a single wire. This enables this device to be compatible with 3-wire bus systems, where one wire is used for communication, one for battery, and one for ground.

5.2 Functional pin description

See Figure 1, 33910 simplified application diagram, for a graphic representation of the various pins referred to in the following paragraphs. Also, see Pin connections for a description of the pin locations in the package.

5.2.1 Receiver output pin (RXD)

The RXD pin is a digital output. It is the receiver output of the LIN interface and reports the state of the bus voltage: RXD Low when LIN bus is dominant, RXD High when LIN bus is recessive.

5.2.2 Transmitter input pin (TXD)

The TXD pin is a digital input. It is the transmitter input of the LIN interface and controls the state of the bus output (dominant when TXD is Low, recessive when TXD is High). This pin has an internal pull-up to force recessive state in case the input is left floating.

5.2.3 LIN bus pin (LIN)

The LIN pin represents the single-wire bus transmitter and receiver. It is suited for automotive bus systems and is compliant to the LIN bus specification 2.0, 2.1, and SAE J2602-2. The LIN interface is only active during Normal mode. See Table 6, Operating modes overview.

5.2.4 Serial data clock pin (SCLK)

The SCLK pin is the SPI clock input. MISO data changes on the positive transition of the SCLK. MOSI is sampled on the negative edge of the SCLK.

5.2.5 Master out slave in pin (MOSI)

The MOSI digital pin receives SPI data from the MCU. This data input is sampled on the negative edge of SCLK.

5.2.6 Master in slave out pin (MISO)

The MISO pin sends data to an SPI-enabled MCU. It is a digital tri-state output used to shift serial data to the microcontroller. Data on this output pin changes on the positive edge of the SCLK. When $\overline{CS}$ is High, this pin remains in the high-impedance state.

5.2.7 Chip select pin ($\overline{CS}$)

$\overline{CS}$ is an active low digital input. It must remain low during a valid SPI communication and allow for several devices to be connected in the same SPI bus without contention. A rising edge on $\overline{CS}$ signals the end of the transmission and the moment the data shifted in is latched. A valid transmission must consist of 8 bits only. While in STOP mode, a low-to-high level transition on this pin generates a wake-up condition for the 33910.

5.2.8 Analog multiplexer pin (ADOUT0)

The ADOUT0 pin can be configured via the SPI to allow the MCU A/D converter to read the several inputs of the Analog Multiplexer, including the VSENSE and L1 input voltages, and the internal junction temperature.

5.2.9 PWM input control pin (PWMIN)

This digital input can control the high-sides drivers in Normal Request and Normal mode. To enable PWM control, the MCU must perform a write operation to the High-side Control Register (HSCR). This pin has an internal 20 µA current pull-up.

5.2.10 Reset pin ($\overline{RST}$)

This bidirectional pin is used to reset the MCU in case the 33910 detects a reset condition, or to inform the 33910 the MCU has just been reset. After release of the $\overline{RST}$ pin, Normal Request mode is entered. The $\overline{RST}$ pin is an active low filtered input and output formed by a weak pull-up and a switchable pull-down structure which allows this pin to be shorted either to V_{DD} or to GND during software development, without the risk of destroying the driver.

5.2.11 Interrupt pin ($\overline{IRQ}$)

The $\overline{IRQ}$ pin is a digital output used to signal events or faults to the MCU while in Normal and Normal Request mode or to signal a wake-up from Stop mode. This active low output transitions to high only after the interrupt is acknowledged by a SPI read of the respective status bits.

5.2.12 Watchdog configuration pin (WDCONF)

The WDCONF pin is the configuration pin for the internal watchdog. A resistor can be connected to this pin to configure the window watchdog period. When connected directly to ground, the watchdog is disabled. When this pin is left open, the watchdog period is fixed to its lower precision internal default value (150 ms typical).

5.2.13 Ground connection pins (AGND, PGND, LGND)

The AGND, PGND, and LGND pins are the Analog and Power ground pins. The AGND pin is the ground reference of the voltage regulator module. The PGND and LGND pins are used for high current load return as in the LIN interface pin.

Note: PGND, AGND and LGND pins must be connected together.

5.2.14 Digital/analog pin (L1)

The L1 pin is multi purpose input. It can be used as a digital input, which can be sampled by reading the SPI and used for wake-up when 33910 is in low power mode or used as analog input for the analog multiplexer. When used to sense voltage outside the module, a 33 kohm series resistor must be used on the input.

When used as wake-up input L1 can be configured to operate in cyclic-sense mode. In this mode one or both of the high-side switches are configured to be periodically turned on and sample the wake-up input. If a state change is detected between two cycles a wake-up is initiated. The 33910 can also wake-up from Stop or Sleep by a simple state change on L1. When used as analog input, the voltage present on the L1 pin is scaled down by an selectable internal voltage divider and can be routed to the ADOUT0 output through the analog multiplexer.

Note: If L1 input is selected in the analog multiplexer, it is disabled as the digital input and remains disabled in low power mode. No wake-up feature is available in this condition. When the L1 input is not selected in the analog multiplexer, the voltage divider is disconnected from this input.

5.2.15 High-side output pins (HS1 and HS2)

These two high-side switches are able to drive loads such as relays or lamps. Their structures are connected to the VS2 supply pin. The pins are short-circuit protected and both outputs are also protected against overheating. HS1 and HS2 are controlled by SPI and can respond to a signal applied to the PWMIN input pin. HS1 and HS2 outputs can also be used during low-power mode for the cyclic-sense of the wake inputs.

5.2.16 Power supply pins (VS1 and VS2)

Those are the battery level voltage supply pins. In an application, VS1 and VS2 pins must be protected against reverse battery connection and negative transient voltages with external components. These pins sustain standard automotive voltage conditions such as a load dump at 40 V. The high-side switches (HS1 and HS2) are supplied by the VS2 pin. All other internal blocks are supplied by the VS1 pin.

5.2.17 Voltage sense pin (VSENSE)

This input can be connected directly to the battery line. It is protected against battery reverse connection. The voltage present in this input is scaled down by an internal voltage divider, and can be routed to the ADOUT0 output pin and used by the MCU to read the battery voltage. The ESD structure on this pin allows for excursion up to +40 V and down to -27 V, allowing this pin to be connected directly to the battery line. It is strongly recommended to connect a 10 kΩ resistor in series with this pin for protection purposes.

5.2.18 Hall sensor switchable supply pin (HVDD)

This pin provides a switchable supply for external hall sensors. While in Normal mode, this current limited output can be controlled through the SPI. The HVDD pin needs to be connected to an external capacitor to stabilize the regulated output voltage.

5.2.19 +5.0 V main regulator output pin (VDD)

An external capacitor has to be placed on the VDD pin to stabilize the regulated output voltage. The VDD pin is intended to supply a microcontroller. The pin is current limited against shorts to GND and overtemperature protected. During Stop mode, the voltage regulator does not operate with its full drive capabilities and the output current is limited. During Sleep mode, the regulator output is completely shut down.

6 Functional device operations

6.1 Operational modes

6.1.1 Introduction

The 33910 offers three main operating modes: Normal (Run), Stop, and Sleep (Low Power). In Normal mode, the device is active and is operating under normal application conditions. The Stop and Sleep modes are low power modes with wake-up capabilities. In Stop mode, the voltage regulator still supplies the MCU with V_{DD} (limited current capability), while in Sleep mode the voltage regulator is turned off (V_{DD} = 0 V).

Wake-up from Stop mode is initiated by a wake-up interrupt. Wake-up from Sleep mode is done by a reset and the voltage regulator is turned back on. The selection of the different modes is controlled by the MOD1:2 bits in the Mode Control Register (MCR). Figure 14 describes how transitions are done between the different operating modes. Table 6 gives an overview of the operating modes.

6.1.2 Reset mode

The 33910 enters the Reset mode after a power up. In this mode, the $\overline{RST}$ pin is low for 1.0 ms (typical value). After this delay, it enters the Normal Request mode and the $\overline{RST}$ pin is driven high. The Reset mode is entered if a reset condition occurs (V_{DD} low, watchdog trigger fail, after wake-up from Sleep mode, Normal Request mode timeout occurs).

6.1.3 Normal request mode

This is a temporary mode automatically accessed by the device after the Reset mode, or after a wake-up from Stop mode. In Normal Request mode, the VDD regulator is ON, the RESET pin is High, and the LIN is operating in RX Only mode. As soon as the device enters in the Normal Request mode an internal timer is started for 150 ms (typical value). During these 150 ms, the MCU must configure the Timing Control Register (TIMCR) and the Mode Control Register (MCR) with MOD2 and MOD1 bits set = 0, to enter the Normal mode. If within the 150 ms timeout, the MCU does not command the 33910 to Normal mode, it enters in Reset mode. If the WDCONF pin is grounded in order to disable the watchdog function, it goes directly in Normal mode after the Reset mode.

6.1.4 Normal mode

In Normal mode, all 33910 functions are active and can be controlled by the SPI interface and the PWMIN pin. The VDD regulator is ON and delivers its full current capability. If an external resistor is connected between the WDCONF pin and the Ground, the window watchdog function is enabled. The wake-up input (L1) can be read as digital input or have its voltage routed through the analog-multiplexer.

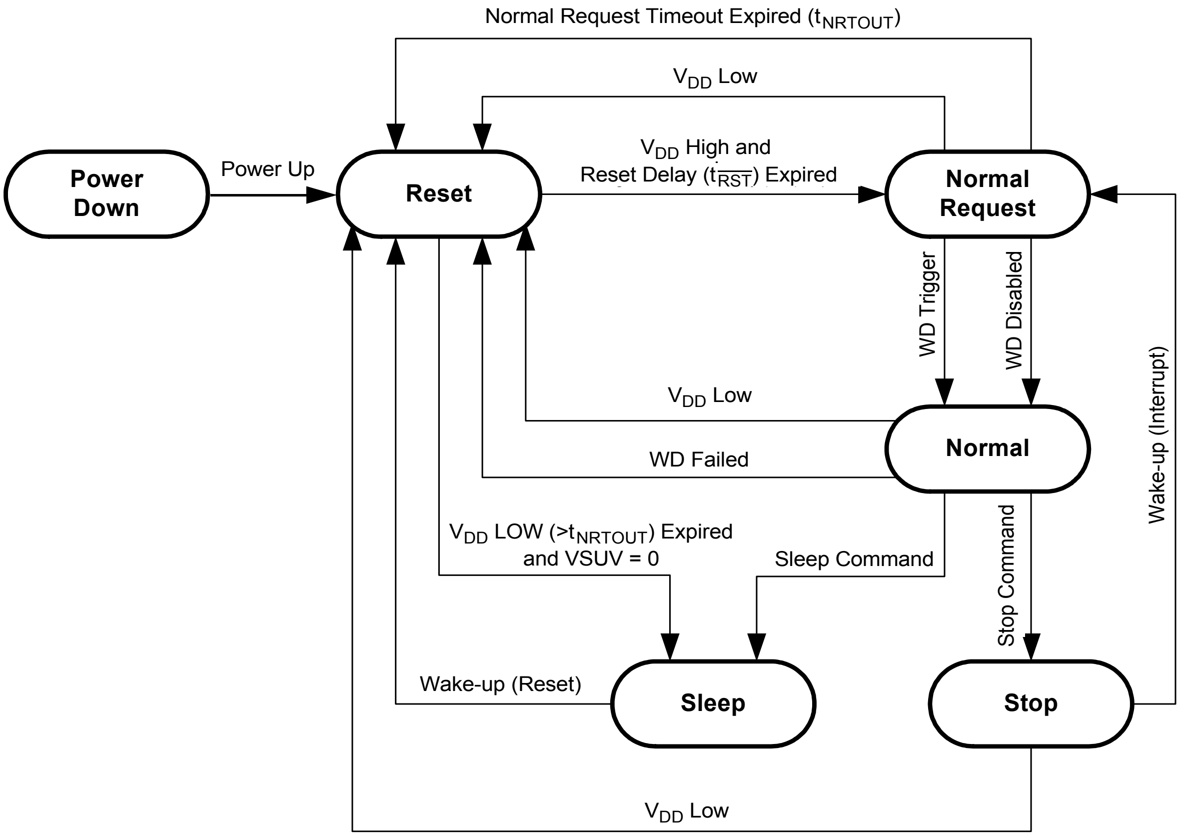
The LIN interface has slew rate and timing compatible with the LIN protocol specification 2.0, 2.1 and SAEJ2602. The LIN bus can transmit and receive information. The high-side switches are active and have PWM capability according to the SPI configuration. The interrupts are generated to report failures for V_{SUP} over/undervoltage, thermal shutdown, or thermal shutdown prewarning on the main regulator.

6.1.5 Sleep mode

The Sleep mode is a low power mode. From Normal mode, the device enters into Sleep mode by sending one SPI command through the Mode Control Register (MCR), or (V_{DD} low > 150 ms) with V_{SUV} = 0. When in Reset mode, a V_{DD} undervoltage condition with no V_{SUP} undervoltage (V_{SUV} = 0) sends the device to Sleep mode. All blocks are in their lowest power consumption condition. Only some wake-up sources (wake-up input with or without cyclic sense, forced wake-up and LIN receiver) are active. The 5.0 V regulator is OFF. The internal low-power oscillator may be active if the IC is configured for cyclic-sense. In this condition, one of the high-side switches is turned on periodically and the wake-up input is sampled. Wake-up from Sleep mode is similar to a power-up. The device goes in Reset mode except the SPI reports the wake-up source and the BATFAIL flag is not set.

6.1.6 Stop mode

The Stop mode is the second low power mode, but in this case the 5.0 V regulator is ON with limited current drive capability. The application MCU is always supplied while the 33910 is operating in Stop mode. The device can enter into Stop mode only by sending the SPI command. When the application is in this mode, it can wake-up from the 33910 side (for example: cyclic sense, force wake-up, LIN bus, wake inputs) or the MCU side ($\overline{CS}$, $\overline{RST}$ pins). Wake-up from Stop mode transitions the 33910 to Normal Request mode and generates an interrupt except if the wake-up event is a low to high transition on the $\overline{CS}$ pin or comes from the $\overline{RST}$ pin.



Legend
WD: Watchdog
WD Disabled: Watchdog disabled (WDCONF pin connected to GND)
WD Trigger: Watchdog is triggered by SPI command
WD Failed: No watchdog trigger or trigger occurs in closed window
Stop Command: Stop command sent via SPI
Sleep Command: Sleep command sent via SPI
Wake-up from Stop mode: L1 state change, LIN bus wake-up, Periodic wake-up, $\overline{CS}$ rising edge wake-up or $\overline{RST}$ wake-up.
Wake-up from Sleep mode: L1 state change, LIN bus wake-up, Periodic wake-up.

Figure 14. Operating modes and transitions

Table 6. Operating modes overview

Function	Reset mode	Normal request mode	Normal mode	Stop mode	Sleep mode
VDD	Full	Full	Full	Stop	-
HVDD	-	SPI (60)	SPI	-	-
HSx	-	SPI/PWM (61)	SPI/PWM	Note (62)	Note (63)
Analog Mux	-	SPI	SPI	-	-
L1	-	Input	Input	Wake-up	Wake-up
LIN	-	Rx-Only	Full/Rx-Only	Rx-Only/Wake-up	Wake-up
Watchdog	-	150 ms (typ.) timeout	On (64)/Off	-	-
Voltage Monitoring	V_{SUP}/V_{DD}	V_{SUP}/V_{DD}	V_{SUP}/V_{DD}	V_{DD}	-

Notes

60. Operation can be enabled/controlled by the SPI.
61. Operation can be controlled by the PWMIN input.
62. HSx switches can be configured for cyclic sense operation in Stop mode.
63. HSx switches can be configured for cyclic sense operation in Sleep mode.
64. Windowing operation when enabled by an external resistor.

6.1.7 Interrupts

Interrupts are used to signal a microcontroller a peripheral needs to be serviced. The interrupts which can be generated, change according to the operating mode. While in Normal and Normal Request modes, the 33910 signals through interrupts special conditions which may require a MCU software action. Interrupts are not generated until all pending wake-up sources are read in the Interrupt Source Register (ISR).

While in Stop mode, interrupts are used to signal wake-up events. Sleep mode does not use interrupts. Wake-up is performed by powering-up the MCU. In Normal and Normal Request mode the wake-up source can be read by SPI. The interrupts are signaled to the MCU by a low logic level of the IRQ pin, which remains low until the interrupt is acknowledged by a SPI read command of the ISR register. The IRQ pin is then driven high. Interrupts are only asserted while in Normal, Normal Request and Stop mode. Interrupts are not generated while the RST pin is low. The following is a list of the interrupt sources in Normal and Normal Request modes. Some of these can be masked by writing to the SPI - Interrupt Mask Register (IMR).

6.1.7.1 Low-voltage interrupt

Signals when the supply line (VS1) voltage drops below the VSUV threshold (V_{SUV}).

6.1.7.2 High-voltage interrupt

Signals when the supply line (VS1) voltage increases above the VSOV threshold (V_{SOV}).

6.1.7.3 Overtemperature prewarning

Signals when the 33910 temperature has reached the pre-shutdown warning threshold. It is used to warn the MCU an overtemperature shutdown in the main 5.0 V regulator is imminent.

6.1.7.4 LIN overtemperature shutdown/TXD stuck at dominant/RXD short-circuit

These signal fault conditions within the LIN interface causes the LIN driver to be disabled. In order to restart the operation, the fault must be removed and TXD must go recessive.

6.1.7.5 High-side overtemperature shutdown

Signals a shutdown in the high-side outputs.

6.1.8 Reset

To reset a MCU the 33910 drives the $\overline{RST}$ pin low for the time the reset condition lasts. After the reset source is removed, the state machine drives the $\overline{RST}$ output low for at least 1.0 ms (typical value) before driving it high. In the 33910, four main reset sources exist:

6.1.8.1 5.0 V regulator low-voltage-reset ($V_{\overline{RST}TH}$)

The 5.0 V regulator output V_{DD} is continuously monitored against brown outs. If the supply monitor detects the voltage at the VDD pin has dropped below the reset threshold $V_{\overline{RST}TH}$ the 33910 issues a reset. In case of overtemperature, the voltage regulator is disabled and the voltage monitoring issues a VDDOT Flag independently of the V_{DD} voltage.

6.1.8.2 Window watchdog overflow

If the watchdog counter is not properly serviced while its window is open, the 33910 detects an MCU software run-away and resets the microcontroller.

6.1.8.3 Wake-up from sleep mode

During Sleep mode, the 5.0 V regulator is not active, hence all wake-up requests from Sleep mode require a power-up/reset sequence.

6.1.8.4 External reset

The 33910 has a bidirectional reset pin which drives the device to a safe state (same as Reset mode) for as long as this pin is held low. The $\overline{RST}$ pin must be held low long enough to pass the internal glitch filter and get recognized by the internal reset circuit. This functionality is also active in Stop mode. After the $\overline{RST}$ pin is released, there is no extra $t_{\overline{RST}}$ to be considered.

6.1.9 Wake-up capabilities

Once entered into one of the low-power modes (Sleep or Stop) only wake-up sources can bring the device into Normal mode operation. In Stop mode, a wake-up is signaled to the MCU as an interrupt, while in Sleep mode the wake-up is performed by activating the 5.0 V regulator and resetting the MCU. In both cases the MCU can detect the wake-up source by accessing the SPI registers and reading the Interrupt Source Register. There is no specific SPI register bit to signal a $\overline{CS}$ wake-up or external reset. If necessary this condition is detected by excluding all other possible wake-up sources.

6.1.9.1 Wake-up from wake-up input (L1) with cyclic sense disabled

The wake-up line is dedicated to sense state changes of external switch and wake-up the MCU (in Sleep or Stop mode). In order to select and activate direct wake-up from L1 input, the Wake-up Control Register (WUCR) must be configured with appropriate L1WE input enabled or disabled. The wake-up input's state is read through the Wake-up Status Register (WUSR). L1 input is also used to perform cyclic-sense wake-up.

Note: Selecting an L1 input in the analog multiplexer before entering low power mode disables the wake-up capability of the L1 input

6.1.9.2 Wake-up from wake-up input (L1) with cyclic sense timer enabled

The SBCLIN can wake-up at the end of a cyclic sense period if on the wake-up input line (L1) a state change occurs. One or both HSx switch can be activated in Sleep or Stop modes from an internal timer. Cyclic sense and force wake-up are exclusive. If cyclic sense is enabled, the force wake-up can not be enabled. In order to select and activate the cyclic sense wake-up from the L1 input, before entering in low power modes (Stop or Sleep modes), the following SPI set-up has to be performed:

In WUCR: select the L1 input to WU-enable.

In HSCR: enable the desired HSx.

- In TIMCR: select the CS/$\overline{WD}$ bit and determine the cyclic sense period with CYSTx bits.
- Perform Goto Sleep/Stop command.

6.1.9.3 Forced wake-up

The 33910 can wake-up automatically after a predetermined time spent in Sleep or Stop mode. Cyclic sense and Forced wake-up are exclusive. If Forced wake-up is enabled, the Cyclic Sense can not be enabled. To determine the wake-up period, the following SPI set-up has to be sent before entering in low power modes:

- In TIMCR: select the CS/$\overline{\text{WD}}$ bit and determine the low power mode period with CYSTx bits.
- In HSCR: all HSx bits must be disabled.

6.1.9.4 $\overline{\text{CS}}$ wake-up

While in Stop mode, a rising edge on the $\overline{\text{CS}}$ causes a wake-up. The $\overline{\text{CS}}$ wake-up does not generate an interrupt, and is not reported on SPI.

6.1.9.5 LIN wake-up

While in the low-power mode, the 33910 monitors the activity on the LIN bus. A dominant pulse larger than t_{PROPWL} followed by a dominant to recessive transition causes a LIN wake-up. This behavior protects the system from a short to ground bus condition. The bit RXONLY = 1 from LINCR Register disables the LIN wake-up from Stop mode.

6.1.9.6 $\overline{\text{RST}}$ wake-up

While in Stop mode, the 33910 can wake-up when the $\overline{\text{RST}}$ pin is held low long enough to pass the internal glitch filter. Then, the 33910 changes to Normal Request or Normal modes depending on the WDCONF pin configuration. The $\overline{\text{RST}}$ wake-up does not generate an interrupt and is not reported via SPI.

From Stop mode, the following wake-up events can be configured:

- Wake-up from L1 input without cyclic sense
- Cyclic sense wake-up inputs
- Force wake-up
- $\overline{\text{CS}}$ wake-up
- LIN wake-up
- $\overline{\text{RST}}$ wake-up

From Sleep mode, the following wake-up events can be configured:

- Wake-up from L1 input without cyclic sense
- Cyclic sense wake-up inputs
- Force wake-up
- LIN wake-up

6.1.10 Window watchdog

The 33910 includes a configurable window watchdog which is active in Normal mode. The watchdog can be configured by an external resistor connected to the WDCONF pin. The resistor is used to achieve higher precision in the timebase used for the watchdog. SPI clears are performed by writing through the SPI in the MOD bits of the Mode Control Register (MCR).

During the first half of the SPI timeout, watchdog clears are not allowed, but after the first half of the SPI timeout window, the clear operation opens. If a clear operation is performed outside the window, the 33910 resets the MCU, in the same way as when the watchdog overflows.

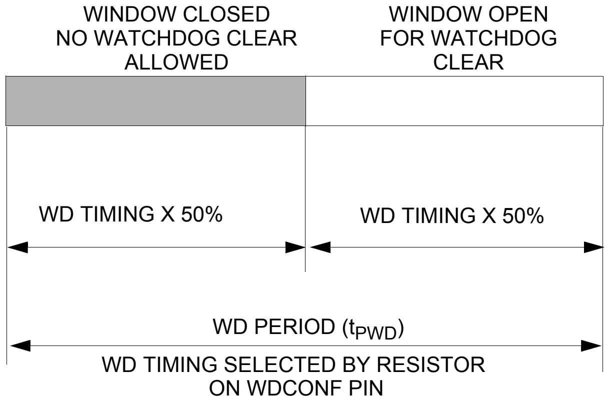


Figure 15. Window watchdog operation

To disable the watchdog function in Normal mode the user must connect the WDCONF pin to ground. This measure effectively disables Normal Request mode. The WDOFF bit in the Watchdog Status Register (WDSR) is set. This condition is only detected during Reset mode. If neither a resistor nor a connection to ground is detected, the watchdog falls back to the internal lower precision timebase of 150 ms (typ.) and signals the faulty condition through the Watchdog Status Register (WDSR).

The watchdog timebase can be further divided by a prescaler which can be configured by the Timing Control Register (TIMCR). During Normal Request mode, the window watchdog is not active but there is a 150 ms (typ.) timeout for leaving the Normal Request mode. In case of a timeout, the 33910 enters into Reset mode, resetting the microcontroller before entering again into Normal Request mode.

6.1.11 Faults detection management

The 33910 has the capability to detect faults like an overvoltage or undervoltage on VS1, TxD in permanent Dominant State, Overtemperature on HS, LIN. It is able to take corrective actions accordingly. Most of faults are monitoring through SPI and the Interrupt pin. The microcontroller can also take actions. The following table summarizes all fault sources the device is able to detect with associated conditions. The status for a device recovery and the SPI or pins monitoring are also described.

Table 7. Fault detection management conditions

Block	Fault	Mode	Condition	Fallout	Recovery	Monitoring [66]	
						Reg (flag, bit)	Interrupt
Power Supply	Battery Fail	All modes	V_{SUP}<3.0 V (typ) then power-up	-	Condition gone	VSR (BATFAIL, 0)	-
	Vsup Overvoltage	Normal, Normal Request	V_{SUP} > 19.25 V (typ)	In Normal mode, HS shutdown if bit HVSE=1 (reg MCR)	Condition gone, to re-enable HS write to HSCR registers	VSR (VSOV,3)	IRQ low + ISR (0101) [67]
	V_{SUP} Undervoltage		V_{SUP} < 6.0 V (typ)	-	Condition gone	VSR (VSUV,2)	IRQ low + ISR (0101)
	V_{DD} Undervoltage	All except Sleep	V_{DD} < 4.5 V (typ)	Reset [65]		-	-
	V_{DD} Overtemp Prewarning	All except Low Power modes	Temperature > 115 °C (typ)	-		VSR (VDDOT,1)	IRQ low + ISR (0101)
	V_{DD} Overtemperature		Temperature > 170 °C (typ)	VDD shutdown, Reset then Sleep		-	-
LIN	Rxd Pin Short Circuit	Normal, Normal Request	RXD pin shorted to GND or 5.0 V	LIN trans shutdown	LIN transmitter re-enabled once the condition is gone and TXD is high	LINSR, (RXSHORT,3)	IRQ low + ISR (0100) [67]
	Txd Pin Permanent Dominant		TXD pin low for more than 1.0 s (typ)	LIN transmitter shutdown		LINSR (TXDOM,2)	
	Lin Driver Overtemperature		Temperature > 160 °C (typ)			LINSR (LINOT,1)	

Table 7. Fault detection management conditions (continued)

<table>
<tr><th rowspan="2">Block</th><th rowspan="2">Fault</th><th rowspan="2">Mode</th><th rowspan="2">Condition</th><th rowspan="2">Fallout</th><th rowspan="2">Recovery</th><th colspan="2">Monitoring (66)</th></tr>
<tr><th>Reg (flag, bit)</th><th>Interrupt</th></tr>
<tr><td rowspan="5">High-side</td><td>High-side Drivers Overtemperature</td><td rowspan="5">Normal, Normal Request</td><td>Temperature > 160 °C (typ)</td><td>Both HS thermal shutdown</td><td>Condition gone, to re-enable HS write to HSCR reg</td><td>All flags in HSSR are set</td><td>IRQ low + ISR (0010) (67)</td></tr>
<tr><td>Hs1 Open Load Detection</td><td rowspan="2">Current through HSx < 5.0 mA (typ)</td><td rowspan="2">-</td><td rowspan="4">Condition gone</td><td>HSSR (HS1OP,1)</td><td rowspan="4">-</td></tr>
<tr><td>Hs2 Open-load Detection</td><td>HSSR (HS2OP,3)</td></tr>
<tr><td>Hs1 Overcurrent</td><td rowspan="2">Current through HSx tends to rise above the current limit 60 mA (min)</td><td rowspan="2">HSx on with limited current capability 60 mA (min)</td><td>HSSR (HS1CL,0)</td></tr>
<tr><td>Hs2 Overcurrent</td><td>HSSR (HS2CL,2)</td></tr>
<tr><td rowspan="3">Watchdog</td><td>Normal Request Time-out Expired</td><td>Normal Request</td><td>The MCU did not command the device to Normal mode within the 150 ms timeout after reset</td><td>Reset</td><td rowspan="2">-</td><td>-</td><td rowspan="3">-</td></tr>
<tr><td>Watchdog Timeout</td><td>Normal</td><td>WD timeout or WD clear within the window closed</td><td>Reset</td><td>WDSR (WDTO, 3)</td></tr>
<tr><td>Watchdog Error</td><td>Normal</td><td>WDCONF pin is floating</td><td>WD internal lower precision timebase 150 ms (typ)</td><td>Connect WDCONF to a resistor or to GND</td><td>WDSR (WDERR, 2)</td></tr>
</table>

Notes

65. When in Reset mode a VDD undervoltage condition combined with no V_{SUP} undervoltage (VSUV = 0) sends the device to Sleep mode.
66. Registers to be read when back in Normal Request or Normal mode depending on the fault. Interrupts only generated in Normal, Normal Request and Stop modes
67. Unless masked, If masked IRQ remains high and the ISR flags are not set.

6.1.12 Temperature sense gain

The analog multiplexer can be configured via SPI to allow the ADOUT0 pin to deliver the internal junction temperature of the device. Figure 16 illustrates the internal chip temp sense obtained per characterization at 3 temperatures with 3 different lots and 30 samples.

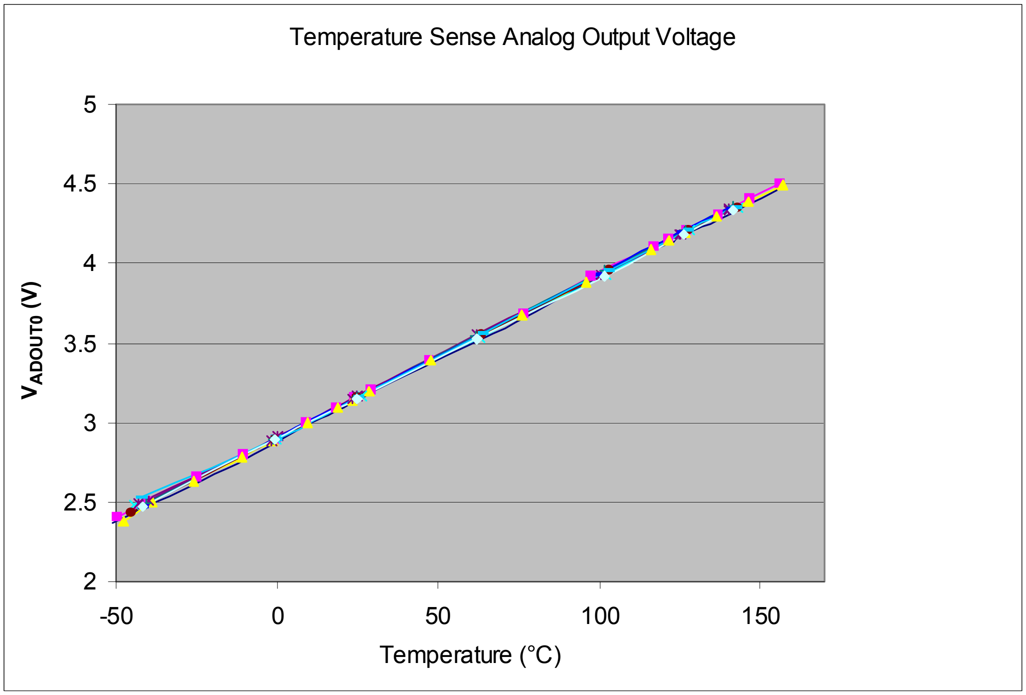


Figure 16. Temperature sense gain

6.1.13 High-side output pins HS1 and HS2

These outputs are two high-side drivers intended to drive small resistive loads or LEDs incorporating the following features:

- PWM capability (software maskable)
- Open load detection
- Current limitation
- Overtemperature shutdown (with maskable interrupt)
- High-voltage shutdown (software maskable)
- Cyclic sense

The high-side switches are controlled by the bits HS1:2 in the High-side Control Register (HSCR).

6.1.13.1 PWM capability (direct access)

Each high-side driver offers additional (to the SPI control) direct control via the PWMIN pin. If both the bits HS1 and PWMHS1 are set in the High-side Control Register (HSCR), then the HS1 driver is turned on if the PWMIN pin is high and turned of if the PWMIN pin is low. This applies to HS2 configuring HS2 and PWMHS2 bits.

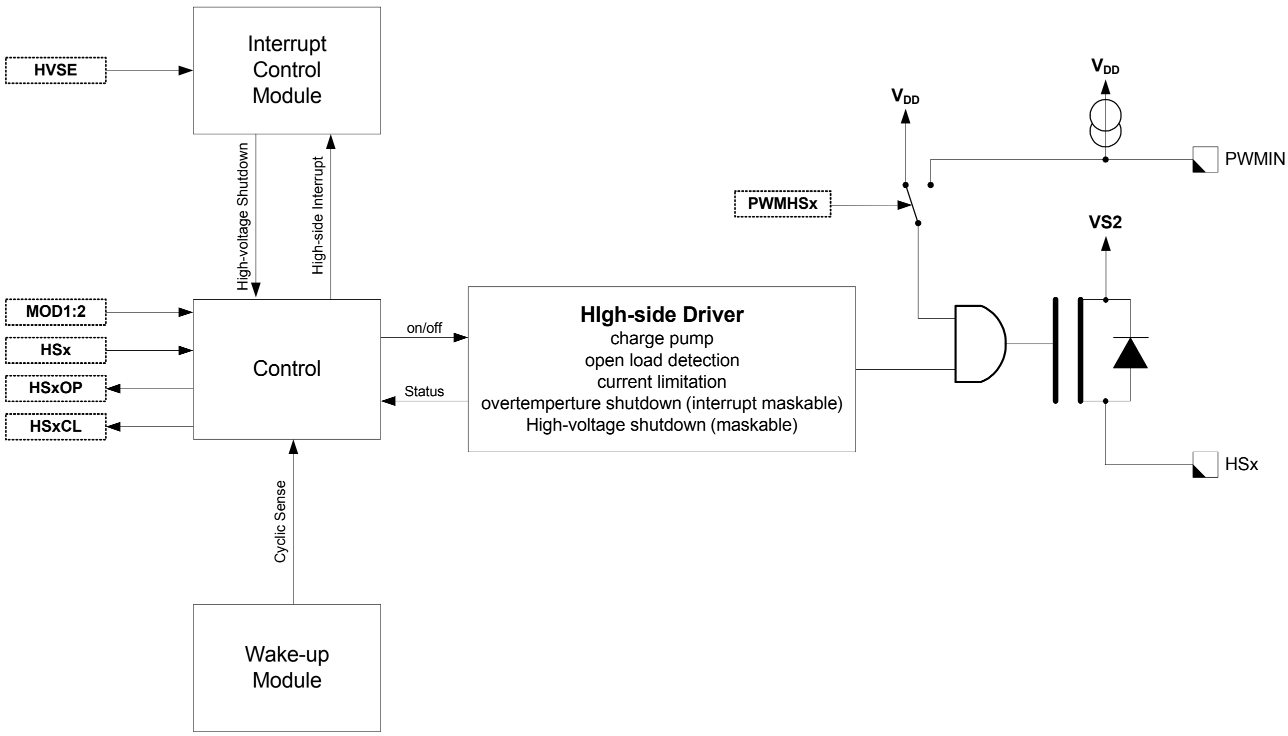


Figure 17. High-side drivers HS1 and HS2

6.1.13.2 Open load detection

Each high-side driver signals an open load condition if the current through the high-side is below the open load current threshold. The open load condition is indicated with the bits HS1OP and HS2OP in the High-side Status Register (HSSR).

6.1.13.3 Current limitation

Each high-side driver has an output current limitation. In combination with the overtemperature shutdown the high-side drivers are protected against overcurrent and short-circuit failures. When the driver operates in the current limitation area, it is indicated with the bits HS1CL and HS2CL in the HSSR.

Note: If the driver is operating in current limitation mode, excessive power might be dissipated.

6.1.13.4 Overtemperature protection (HS interrupt)

Both high-side drivers are protected against overtemperature. In case of an overtemperature condition both high-side drivers are shut down and the event is latched in the Interrupt Control Module. The shutdown is indicated as HS Interrupt in the Interrupt Source Register (ISR). A thermal shutdown of the high-side drivers is indicated by setting all HSxOP and HSxCL bits simultaneously. If the bit HSM is set in the Interrupt Mask Register (IMR), then an interrupt (IRQ) is generated. A write to the High-side Control Register (HSCR), when the overtemperature condition is gone, re-enables the high-side drivers.

6.1.13.5 High-voltage shutdown

In case of a high voltage condition and if the high voltage shutdown is enabled (bit HVSE in the Mode Control Register (MCR) is set both high-side drivers are shut down. A write to the High-side Control Register (HSCR), when the high voltage condition is gone, re-enables the high-side drivers.

6.1.13.6 Sleep and stop mode

The high-side drivers can be enabled to operate in Sleep and Stop mode for cyclic sensing. Also see Table 6, Operating modes overview.

6.1.14 Lin physical layer

The LIN bus pin provides a physical layer for single-wire communication in automotive applications. The LIN physical layer is designed to meet the LIN physical layer specification and has the following features:

- LIN physical layer 2.0, 2.1 and SAEJ2602 compliant
- Slew rate selection
- Overtemperature shutdown
- Advanced diagnostics

The LIN driver is a low-side MOSFET with thermal shutdown. An internal pull-up resistor with a serial diode structure is integrated, so no external pull-up components are required for the application in a slave node. The fall time from dominant to recessive and the rise time from recessive to dominant is controlled. The symmetry between both slopes is guaranteed.

6.1.14.1 LIN pin

The LIN pin offers a high susceptibility immunity level from external disturbance, guaranteeing communication during external disturbance.

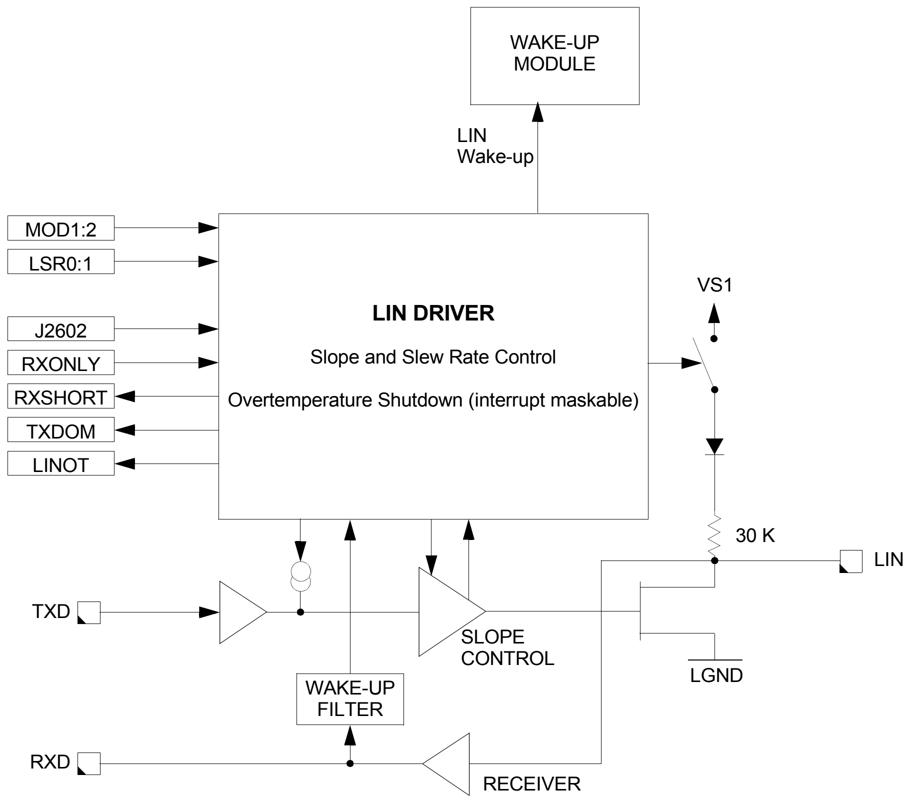


Figure 18. LIN interface

6.1.14.2 Slew rate selection

The slew rate can be selected for optimized operation at 10.4 and 20 kBit/s as well as a fast baud rate for test and programming. The slew rate can be adapted with the bits LSR1:0 in the LIN Control Register (LINCR). The initial slew rate is optimized for 20 kBit/s.

6.1.14.3 J2602 conformance

To be compliant with the SAE J2602-2 specification, the J2602 feature has to be enabled in the LINCR Register (bit DIS_J2602 sets to 0). The LIN transmitter is disabled in case of a V_{SUP} undervoltage condition occurs and TXD is in Recessive State: the LIN bus goes in Recessive State and RXD goes high. The LIN transmitter is not disabled if TXD is in Dominant State. A deglitcher on V_{SUP} (t_{J2602_DEG}) is implemented to avoid false switching.

If the (DIS_J2602) bit is set to 1, the J2602 feature is disabled and the communication TXD-LIN-RXD works for V_{SUP} down to 4.6 V (typical value) and then the communication is interrupted. The (DIS_J2602) bit is set per default to 0.

6.1.14.4 Overtemperature shutdown (LIN interrupt)

The output low-side FET is protected against overtemperature conditions. In case of an overtemperature condition, the transmitter is shut down and the LINOT bit in the LIN Status Register (LINSR) is set. If the LINM bit is set in the Interrupt Mask Register (IMR), an Interrupt $\overline{IRQ}$ is generated. The transmitter is automatically re-enabled once the condition is gone and TXD is high.

6.1.14.5 RXD short-circuit detection (LIN interrupt)

The LIN transceiver has a short-circuit detection for the RXD output pin. If the device transmits and in case of a short-circuit condition, either 5.0 V or Ground, the RXSHORT bit in the LIN Status Register (LINSR) is set and the transmitter is shutdown. If the LINM bit is set in the Interrupt Mask Register (IMR), an Interrupt $\overline{IRQ}$ is generated. The transmitter is automatically re-enabled once the condition is gone (transition on RXD) and TXD is high. A read of the LIN Status Register (LINSR) without the RXD pin short-circuit condition clears the bit RXSHORT.

6.1.14.6 TXD dominant detection (LIN interrupt)

The LIN transceiver monitors the TXD input pin to detect a stuck in dominant (0 V) condition. In case of a stuck condition (TXD pin 0 V for more than 1 second (typ.)), the transmitter is shut down and the TXDOM bit in the LIN Status Register (LINSR) is set. If the LINM bit is set in the IMR, an Interrupt $\overline{IRQ}$ is generated. The transmitter is automatically re-enabled once TXD is high. A read of the LIN Status Register (LINSR) with the TXD pin at 5.0 V clears the bit TXDOM.

6.1.14.7 LIN receiver operation only

While in Normal mode, the activation of the RXONLY bit disables the LIN TXD driver. In case of a LIN error condition, this bit is automatically set. If Stop mode is selected with this bit set, the LIN wake-up functionality is disabled and the RXD pin reflects the state of the LIN bus.

6.1.14.8 Stop mode and wake-up feature

During Stop mode operation, the transmitter of the physical layer is disabled. The receiver is still active and able to detect wake-up events on the LIN bus line. A dominant level longer than T_{PROPWL} followed by a rising edge generates a wake-up interrupt, and is reported in the Interrupt Source Register (ISR). Also see Figure 11.

6.1.14.9 Sleep mode and wake-up feature

During Sleep mode operation, the transmitter of the physical layer is disabled. The receiver must be active to detect wake-up events on the LIN bus line. A dominant level longer than T_{PROPWL} followed by a rising edge generates a system wake-up (Reset), and is reported in the Interrupt Source Register (ISR). Also see Figure 10.

6.2 Logic commands and registers

6.2.1 33910 SPI interface and configuration

The serial peripheral interface creates the communication link between a microcontroller (master) and the 33910. The interface consists of four pins (see Figure 19):

- $\overline{CS}$—Chip Select
- MOSI—Master-out Slave-in
- MISO—Master-in Slave-out
- SCLK—Serial Clock

A complete data transfer via the SPI consists of 1 byte. The master sends 4 bits of address (A3:A0) + 4 bits of control information (C3:C0) and the slave replies with four system status bits (VMS, LINS, HSS, n.d.) + 4 bits of status information (S3:S0).

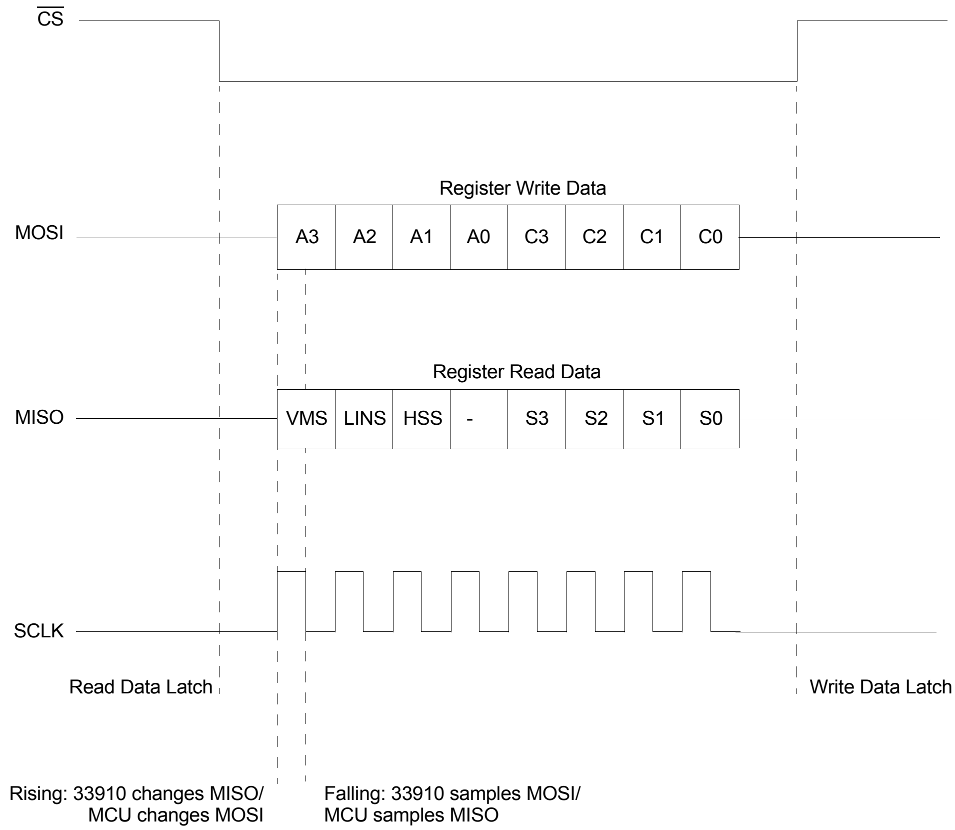


Figure 19. SPI protocol

During the inactive phase of the $\overline{CS}$ (HIGH), the new data transfer is prepared. The falling edge of the $\overline{CS}$ indicates the start of a new data transfer and puts the MISO in the low-impedance state and latches the analog status data (Register read data). With the rising edge of the SPI clock (SCLK), the data is moved to MISO/MOSI pins. With the falling edge of the SPI clock (SCLK), the data is sampled by the receiver.

The data transfer is only valid if exactly eight sample clock edges are present during the active (low) phase of $\overline{CS}$. The rising edge of the Chip Select $\overline{CS}$ indicates the end of the transfer and latches the write data (MOSI) into the register. The $\overline{CS}$ high forces MISO to the high-impedance state. Register reset values are described along with the reset condition. Reset condition is the condition causing the bit to be set to its reset value. The main reset conditions are:

- Power-On Reset (POR): the level at which the logic is reset and BATFAIL flag sets.
- Reset mode
- Reset done by the $\overline{RST}$ pin (ext_reset)

6.3 SPI register overview

Table 8. System status register

Adress(A3:A0)	Register Name / Read/Write Information		BIT			
			7	6	5	4
$0 - $F	SYSSR - System Status Register	R	VMS	LINS	HSS	-

Table 9 summarizes the SPI Register content for Control Information (C3:C0) = W and status information (S3:S0) = R.

Table 9. SPI register overview

Adress(A3:A0)	Register Name / Read/Write Information		BIT			
			3	2	1	0
$0	MCR - Mode Control Register	W	HVSE	0	MOD2	MOD1
	VSR - Voltage Status Register	R	VSOV	VSUV	VDDOT	BATFAIL
$1	VSR - Voltage Status Register	R	VSOV	VSUV	VDDOT	BATFAIL
$2	WUCR - Wake-up Control Register	W	0	0	0	L1WE
	WUSR - Wake-up Status Register	R	-	-	-	L1
$3	WUSR - Wake-up Status Register	R	-	-	-	L1
$4	LINCR - LIN Control Register	W	DIS_J2602	RXONLY	LSR1	LSR0
	LINSR - LIN Status Register	R	RXSHORT	TXDOM	LINOT	0
$5	LINSR - LIN Status Register	R	RXSHORT	TXDOM	LINOT	0
$6	HSCR - High-side Control Register	W	PWMHS2	PWMHS1	HS2	HS1
	HSSR - High-side Status Register	R	HS2OP	HS2CL	HS1OP	HS1CL
$7	HSSR - High-side Status Register	R	HS2OP	HS2CL	HS1OP	HS1CL
$A	TIMCR - Timing Control Register	W	CS/$\overline{WD}$	WD2	WD1	WD0
				CYST2	CYST1	CYST0
	WDSR - Watchdog Status Register	R	WDTO	WDERR	WDOFF	WDWO
$B	WDSR - Watchdog Status Register	R	WDTO	WDERR	WDOFF	WDWO
$C	AMUXCR - Analog Multiplexer Control Register	W	L1DS	MX2	MX1	MX0
$D	CFR - Configuration Register	W	HVDD	CYSX8	0	0
$E	IMR - Interrupt Mask Register	W	HSM	0	LINM	VMM
	ISR - Interrupt Source Register	R	ISR3	ISR2	ISR1	ISR0
$F	ISR - Interrupt Source Register	R	ISR3	ISR2	ISR1	ISR0

6.3.1 Register definitions

6.3.1.1 System status register - SYSSR

The System Status Register (SYSSR) is always transferred with every SPI transmission and gives a quick system status overview. It summarizes the status of the Voltage Monitor Status (VMS), LIN Status (LINS) and High-side Status (HSS).

Table 10. System status register

	S7	S6	S5	S4
Read	VMS	LINS	HSS	-

This read-only bit indicates one or more bits in the VSR are set.

1 = Voltage Monitor bit set

0 = None

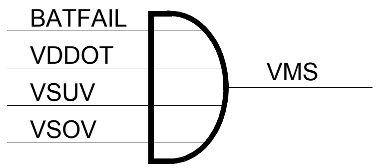


Figure 20. Voltage monitor status

This read-only bit indicates one or more bits in the LINSR are set.

1 = LIN Status bit set

0 = None

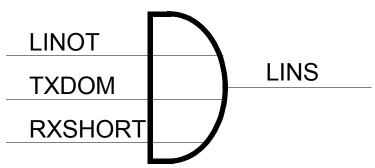


Figure 21. LIN status

This read-only bit indicates one or more bits in the HSSR are set.

1 = High-side Status bit set

0 = None

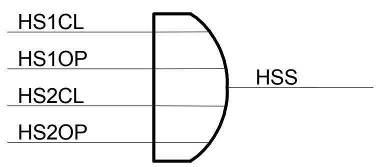


Figure 22. High-side status

6.3.1.2 Mode control register - MCR

The Mode Control Register (MCR) allows switching between the operation modes and to configure the 33910. Writing the MCR returns the VSR.

Table 11. Mode control register - $0

	C3	C2	C1	C0
Write	HVSE	0	MOD2	MOD1
Reset Value	1	0	-	-
Reset Condition	POR	POR	-	-

This write-only bit enables/disables automatic shutdown of the high-side drivers during a high-voltage VSOV condition.
1 = automatic shutdown enabled
0 = automatic shutdown disabled
These write-only bits select the operating mode and allow clearing the watchdog in accordance with Table 9, Mode Control Bits.

Table 12. Mode control bits

MOD2	MOD1	Description
0	0	Normal Mode
0	1	Stop Mode
1	0	Sleep Mode
1	1	Normal Mode + Watchdog Clear

6.3.1.3 Voltage status register - VSR

Returns the status of the several voltage monitors. This register is also returned when writing to the Mode Control Register (MCR).

Table 13. Voltage status register - $0/$1

	S3	S2	S1	S0
Read	VSOV	VSUV	VDDOT	BATFAIL

6.3.1.3.1 VSOV - V_{SUP} overvoltage

This read-only bit indicates an overvoltage condition on the VS1 pin.
1 = Overvoltage condition.
0 = Normal condition.

6.3.1.3.2 VSUV - V_{SUP} undervoltage

This read-only bit indicates an undervoltage condition on the VS1 pin.
1 = Undervoltage condition.
0 = Normal condition.

6.3.1.3.3 VDDOT - main voltage regulator overtemperature warning

This read-only bit indicates the main voltage regulator temperature reached the Overtemperature Prewarning Threshold.
1 = Overtemperature Prewarning
0 = Normal

6.3.1.3.4 BATFAIL - battery fail flag

This read-only bit is set during power-up and indicates the 33910 had a Power-On-Reset (POR). Any access to the MCR or VSR clears the BATFAIL flag.

1 = POR Reset has occurred

0 = POR Reset has not occurred

6.3.1.4 Wake-up control register - WUCR

This register is used to control the digital wake-up input. Writing the WUCR returns the Wake-Up Status Register (WUSR).

Table 14. Wake-up Control Register - $2

	C3	C2	C1	C0
Write	0	0	0	L1WE
Reset Value	1	1	1	1
Reset Condition	POR, Reset mode or ext_reset			

6.3.1.4.1 L1WE - wake-up input enable

This write-only bit enables/disables the L1 input. In Stop and Sleep mode the L1WE bit activates the L1 input for wake-up. If the L1 input is selected on the analog multiplexer, the L1WE is masked to 0.

1 = Wake-up Input enabled.

0 = Wake-up Input disabled.

6.3.1.5 Wake-up status register - WUSR

This register is used to monitor the digital wake-up input and is also returned when writing to the WUCR.

Table 15. Wake-up status register - $2/$3

	S3	S2	S1	S0
Read	-	-	-	L1

6.3.1.5.1 L1 - wake-up input 1

This read-only bit indicates the status of the L1 input. If the L1 input is not enabled, then the Wake-up status returns 0. After a wake-up from Stop or Sleep mode this bit also allows to verify the L1 input has caused the wake-up, by first reading the Interrupt Status Register (ISR) and then reading the WUSR. The source of the wake-up is only reported on the first WUCR or WUSR access.

1 = L1 pin high, or L1 is the source of the wake-up.

0 = L1 pin low, disabled or selected as an analog input.

6.3.1.6 LIN control register - LINCR

This register controls the LIN physical interface block. Writing the LIN Control Register (LINCR) returns the LIN Status Register (LINSR).

Table 16. LIN control register - $4

	C3	C2	C1	C0
Write	DIS_J2602	RXONLY	LSR1	LSR0
Reset Value	0	0	0	0
Reset Condition	POR	POR, Reset mode, ext_reset or LIN failure gone*	POR	

* LIN failure gone: if LIN failure (overtemp, TXD/RXD short) was set, the flag resets automatically when the failure is gone.

6.3.1.6.1 J2602 - LIN dominant voltage select

This write-only bit controls the J2602 circuitry. If the circuitry is enabled (bit sets to 0), the TXD-LIN-RXD communication works down to the battery undervoltage condition is detected. Below, the bus is in recessive state. If the circuitry is disabled (bit sets to 1), the communication TXD-LIN-RXD works down to 4.6 V (typical value).

0 = Enabled J2602 feature.

1 = Disabled J2602 feature.

6.3.1.6.2 RXONLY - LIN receiver operation only

This write-only bit controls the behavior of the LIN transmitter. In Normal mode, the activation of the RXONLY bit disables the LIN transmitter. In case of a LIN error condition, this bit is automatically set. In Stop mode this bit disables the LIN wake-up functionality, and the RXD pin reflects the state of the LIN bus.

1 = only LIN receiver active (Normal mode) or LIN wake-up disabled (Stop mode).

0 = LIN fully enabled.

6.3.1.6.3 LSRx - LIN slew rate

This write-only bit controls the LIN driver slew rate in accordance with Table 18.

Table 17. LIN slew rate control

LSR1	LSR0	Description
0	0	Normal Slew Rate (up to 20 kb/s)
0	1	Slow Slew Rate (up to 10 kb/s)
1	0	Fast Slew Rate (up to 100 kb/s)
1	1	Reserved

6.3.1.7 LIN status register - LINSR

This register returns the status of the LIN physical interface block and is also returned when writing to the LINCR.

Table 18. LIN status register - $4/$5

	S3	S2	S1	S0
Read	RXSHORT	TXDOM	LINOT	0

6.3.1.7.1 RXSHORT - RXD pin short-circuit

This read-only bit indicates a short-circuit condition on the RXD pin (shorted either to 5.0 V or to Ground). The short-circuit delay must be a worst case of 8.0 μs to be detected and to shut down the driver. To clear this bit, it must be read after the condition is gone (transition detected on RXD pin). The LIN driver is automatically re-enabled once the condition is gone and TXD is high.

1 = RXD short-circuit condition.

0 = None.

6.3.1.7.2 TXDOM - TXD permanent dominant

This read-only bit signals the detection of a TXD pin stuck at dominant (Ground) condition and the resultant shutdown in the LIN transmitter. This condition is detected after the TXD pin remains in dominant state for more than 1 second (typical value). To clear this bit, it must be read after TXD has gone high. The LIN driver is automatically re-enabled once TXD goes High.

1 = TXD stuck at dominant fault detected.

0 = None.

6.3.1.7.3 LINOT - LIN driver overtemperature

This read-only bit signals the LIN transceiver was shutdown due to overtemperature. The transmitter is automatically re-enabled after the overtemperature condition is gone and TXD is high. The LINOT bit is cleared after SPI read once the condition is gone.

1 = LIN overtemperature shutdown

0 = None

6.3.1.8 High-side control register - HSCR

This register controls the operation of the high-side drivers. Writing to this register returns the High-side Status Register (HSSR).

Table 19. High-side control register - $6

	C3	C2	C1	C0
Write	PWMHS2	PWMHS1	HS2	HS1
Reset Value	0	0	0	0
Reset Condition	POR		POR, Reset mode, ext_reset, HSx overtemp or (VSOV & HVSE)	

6.3.1.8.1 PWMHSx - PWM input control enable

This write-only bit enables/disables the PWMIN input pin to control the respective high-side switch. The corresponding high-side switch must be enabled (HSx bit).

1 = PWMIN input controls HSx output.

0 = HSx is controlled only by SPI.

6.3.1.8.2 HSx - HSx switch control

This write-only bit enables/disables the corresponding high-side switch.

1 = HSx switch on.

0 = HSx switch off.

6.3.1.9 High-side status register - HSSR

This register returns the status of the high-side switches and is also returned when writing to the HSCR.

Table 20. High-side Status Register - $6/$7

	S3	S2	S1	S0
Read	HS2OP	HS2CL	HS1OP	HS1CL

6.3.1.9.1 High-side thermal shutdown

A thermal shutdown of the high-side drivers is indicated by setting all HSxOP and HSxCL bits simultaneously.

6.3.1.9.2 HSxOP - high-side switch open load detection

This read-only bit signals the high-side switches are conducting current below a certain threshold indicating possible load disconnection.

1 = HSx Open Load detected (or thermal shutdown)

0 = Normal

6.3.1.9.3 HSxCL - high-side current limitation

This read-only bit indicates the respective high-side switch is operating in current limitation mode.

1 = HSx in current limitation (or thermal shutdown)

0 = Normal

6.3.1.10 Timing control register - TIMCR

This register allows to configure the watchdog, the cyclic sense and Forced Wake-up periods. Writing to the Timing Control Register (TIMCR) also returns the Watchdog Status Register (WDSR).

Table 21. Timing control register - $A

	C3	C2	C1	C0
Write	CS/$\overline{WD}$	WD2	WD1	WD0
		CYST2	CYST1	CYST0
Reset Value	-	0	0	0
Reset Condition	-	POR		

6.3.1.10.1 CS/$\overline{WD}$ - cyclic sense or watchdog prescaler select

This write-only bit selects which prescaler is being written to, the Cyclic Sense/Forced Wake-up prescaler or the Watchdog prescaler.

1 = Cyclic Sense/Forced Wake-up Prescaler selected

0 = Watchdog Prescaler select

6.3.1.10.2 WDx - watchdog prescaler

This write-only bits selects the divider for the watchdog prescaler and therefore selects the watchdog period in accordance with Table 22. This configuration is valid only if windowing watchdog is active.

Table 22. Watchdog prescaler

WD2	WD1	WD0	Prescaler divider
0	0	0	1
0	0	1	2
0	1	0	4
0	1	1	6
1	0	0	8
1	0	1	10
1	1	0	12
1	1	1	14

6.3.1.10.3 CYSTx - cyclic sense period prescaler select

This write-only bits selects the interval for the wake-up cyclic sensing together with the bit CYSX8 in the Configuration Register (CFR) (See Configuration register - CFR on page 47). This option is only active if one of the high-side switches is enabled when entering in Stop or Sleep mode. Otherwise, a timed wake-up is performed after the period shown in Table 23.

Table 23. Cyclic sense and force wake-up interval

CYSX8 [68]	CYST2	CYST1	CYST0	Interval
X	0	0	0	No cyclic sense [69]
0	0	0	1	20 ms
0	0	1	0	40 ms
0	0	1	1	60 ms
0	1	0	0	80 ms
0	1	0	1	100 ms
0	1	1	0	120 ms
0	1	1	1	140 ms
1	0	0	1	160 ms
1	0	1	0	320 ms
1	0	1	1	480 ms
1	1	0	0	640 ms
1	1	0	1	800 ms
1	1	1	0	960 ms
1	1	1	1	1120 ms

Notes

68. Bit CYSX8 is located in Configuration Register (CFR)
69. No Cyclic Sense and no Force Wake-up available.

6.3.1.11 Watchdog status register - WDSR

This register returns the Watchdog status information and is also returned when writing to the TIMCR.

Table 24. Watchdog status register - $A/$B

	S3	S2	S1	S0
Read	WDTO	WDERR	WDOFF	WDWO

6.3.1.11.1 WDTO - watchdog timeout

This read-only bit signals the last reset was caused by either a watchdog timeout or by an attempt to clear the Watchdog within the window closed. Any access to this register or the Timing Control Register (TIMCR) clears the WDTO bit.

1 = Last reset caused by watchdog timeout

0 = None

6.3.1.11.2 WDERR - watchdog error

This read-only bit signals the detection of a missing watchdog resistor. In this condition, the watchdog is using the internal, lower precision timebase. The Windowing function is disabled.

1 = WDCONF pin resistor missing

0 = WDCONF pin resistor not floating

6.3.1.11.3 WDOFF - watchdog off

This read-only bit signals the watchdog pin connected to Ground and therefore disabled. In this case watchdog timeouts are disabled and the device automatically enters Normal mode out of Reset. This might be necessary for software debugging and for programming the Flash memory.

1 = Watchdog is disabled

0 = Watchdog is enabled

6.3.1.11.4 WDWO - watchdog window open

This read-only bit signals when the watchdog window is open for clears. The purpose of this bit is for testing. Should be ignored in case WDERR is High.

1 = Watchdog window open

0 = Watchdog window closed

6.3.1.12 Analog multiplexer control register - MUXCR

This register controls the analog multiplexer and selects the divider ration for the L1 input divider.

Table 25. Analog Multiplexer Control Register -$C

	C3	C2	C1	C0
Write	L1DS	MX2	MX1	MX0
Reset Value	1	0	0	0
Reset Condition	POR	POR, Reset mode or ext_reset		

6.3.1.12.1 L1DS - L1 analog input divider select

This write-only bit selects the resistor divider for the L1 analog input. Voltage is internally clamped to VDD.

0 = L1 Analog divider: 1

1 = L1 Analog divider: 3.6 (typ.)

6.3.1.13 MXx - analog multiplexer input select

These write-only bits selects which analog input is multiplexed to the ADOUT0 pin according to Table 26. When disabled or when in Stop or Sleep mode, the output buffer is not powered and the ADOUT0 output is left floating to achieve lower current consumption.

Table 26. Analog multiplexer channel select

MX2	MX1	MX0	Meaning
0	0	0	Disabled
0	0	1	Reserved
0	1	0	Die Temperature Sensor (70)
0	1	1	VSENSE input
1	0	0	L1 input
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

Notes

70. Accessing the Die Temperature Sensor directly from the Disabled state is not recommended. If this transition must be performed and to avoid the intermediate state, wait at least 1.0 ms, then start the die temp measurement. Possible access is Disabled ⟶ Vsense input ⟶ Die Temperature Sensor.

6.3.1.14 Configuration register - CFR

This register controls the Hall Sensor Supply enable/disable and the cyclic sense timing multiplier.

Table 27. Configuration register - $D

	C3	C2	C1	C0
Write	HVDD	CYSX8	0	0
Reset Value	0	0	0	0
Reset Condition	POR, Reset mode or ext_reset	POR	POR	POR

6.3.1.14.1 HVDD - hall sensor supply enable

This write-only bit enables/disables the state of the hall sensor supply.

1 = HVDD on

0 = HVDD off

6.3.1.14.2 CYSX8 - cyclic sense timing x eight

This write-only bit influences the cyclic sense and Forced Wake-up period as shown in Table 23.

1 = Multiplier enabled

0 = None

6.3.1.15 Interrupt mask register - IMR

This register allows masking of some of the interrupt sources. No interrupt is generated to the MCU and no flag is set in the ISR register. The 5.0 V Regulator overtemperature prewarning interrupt and undervoltage (VSUV) interrupts can not be masked and always causes an interrupt. Writing to the IMR returns the ISR.

Table 28. Interrupt mask register - $E

	C3	C2	C1	C0
Write	HSM	0	LINM	VMM
Reset Value	1	1	1	1
Reset Condition	POR			

6.3.1.15.1 HSM - high-side interrupt mask

This write-only bit enables/disables interrupts generated in the high-side block.

1 = HS Interrupts Enabled

0 = HS Interrupts Disabled

6.3.1.15.2 LINM - LIN interrupts mask

This write-only bit enables/disables interrupts generated in the LIN block.

1 = LIN Interrupts Enabled

0 = LIN Interrupts Disabled

6.3.1.15.3 VMM - voltage monitor interrupt mask

This write-only bit enables/disables interrupts generated in the Voltage Monitor block. The only maskable interrupt in the Voltage Monitor Block is the V_{SUP} overvoltage interrupt.

1 = Interrupts Enabled

0 = Interrupts Disabled

6.3.1.16 Interrupt source register - ISR

This register allows the MCU to determine the source of the last interrupt or wake-up respectively. A read of the register acknowledges the interrupt and leads $\overline{IRQ}$ pin to high, if there are no other pending interrupts. If there are pending interrupts, $\overline{IRQ}$ is driven high for 10 µs and then be driven low again.

This register is also returned when writing to the Interrupt Mask Register (IMR).

Table 29. Interrupt source register - $E/$F

	S3	S2	S1	S0
Read	ISR3	ISR2	ISR1	ISR0

6.3.1.16.1 ISRx - interrupt source register

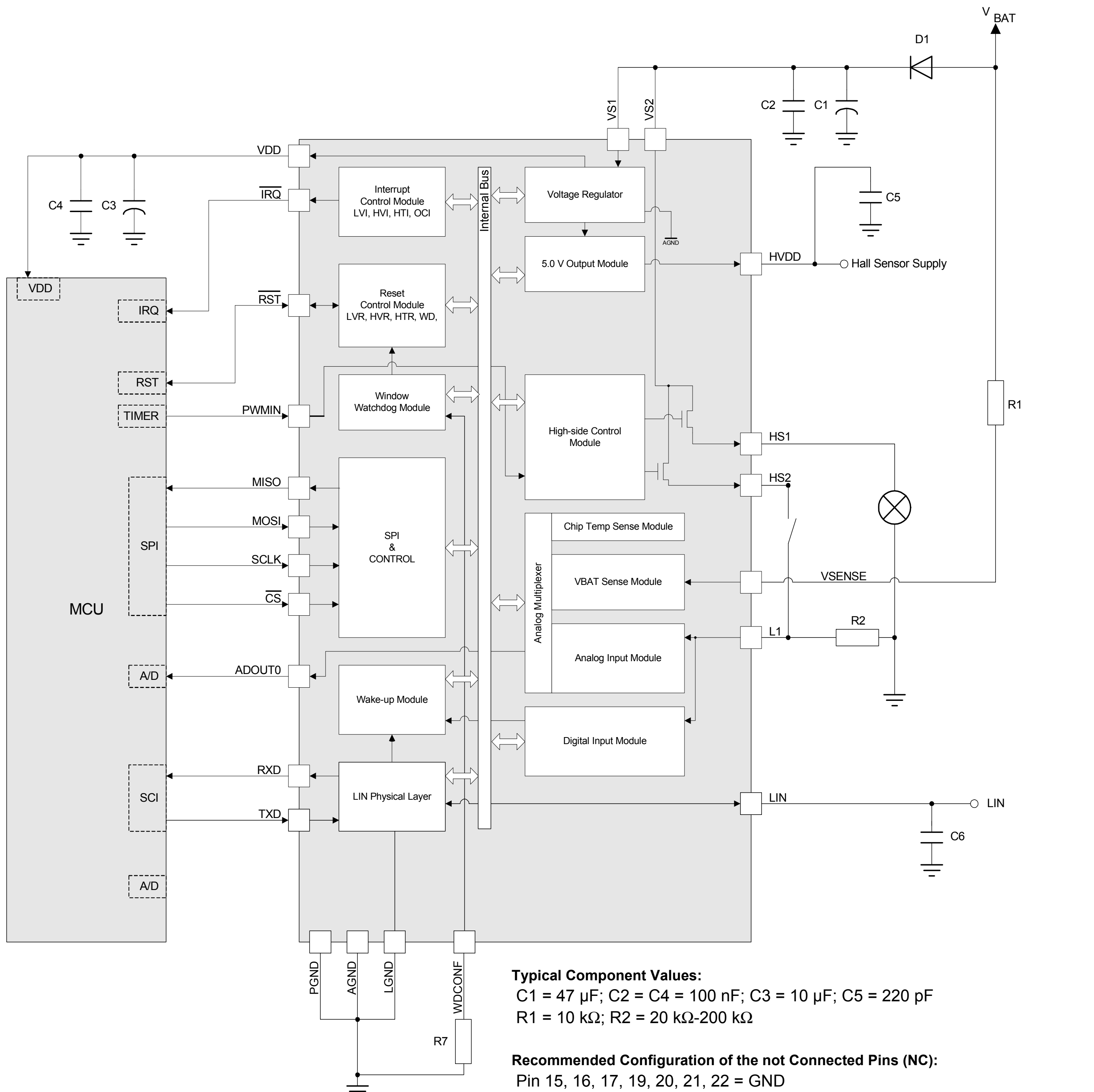
These read-only bits indicate the interrupt source following Table 30. If no interrupt is pending then all bits are 0. If more than one interrupt is pending, the interrupt sources are handled sequentially multiplex.

Table 30. Interrupt sources

ISR3	ISR2	ISR1	ISR0	Interrupt source		Priority
				none maskable	maskable	
0	0	0	0	no interrupt	no interrupt	none
0	0	0	1	L1 Wake-up from Stop and Sleep mode	-	highest
0	0	1	0	-	HS Interrupt (Overtemperature)	
0	0	1	1	-	Reserved	
0	1	0	0	LIN Wake-up	LIN Interrupt (RXSHORT, TXDOM, LIN OT)	
0	1	0	1	Voltage Monitor Interrupt (Low Voltage and VDD overtemperature)	Voltage Monitor Interrupt (High Voltage)	
0	1	1	0	Forced Wake-up	-	lowest

7 Typical application

The 33910 can be configured in several applications. The figure below shows the 33910 in the typical slave node application.



Typical Component Values:

C1 = 47 μF; C2 = C4 = 100 nF; C3 = 10 μF; C5 = 220 pF

R1 = 10 kΩ; R2 = 20 kΩ-200 kΩ

Recommended Configuration of the not Connected Pins (NC):

Pin 15, 16, 17, 19, 20, 21, 22 = GND

Pin 11 = open (floating)

Pin 28 = this pin is not internally connected and may be used for PCB routing optimization.

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9 Internal block diagram

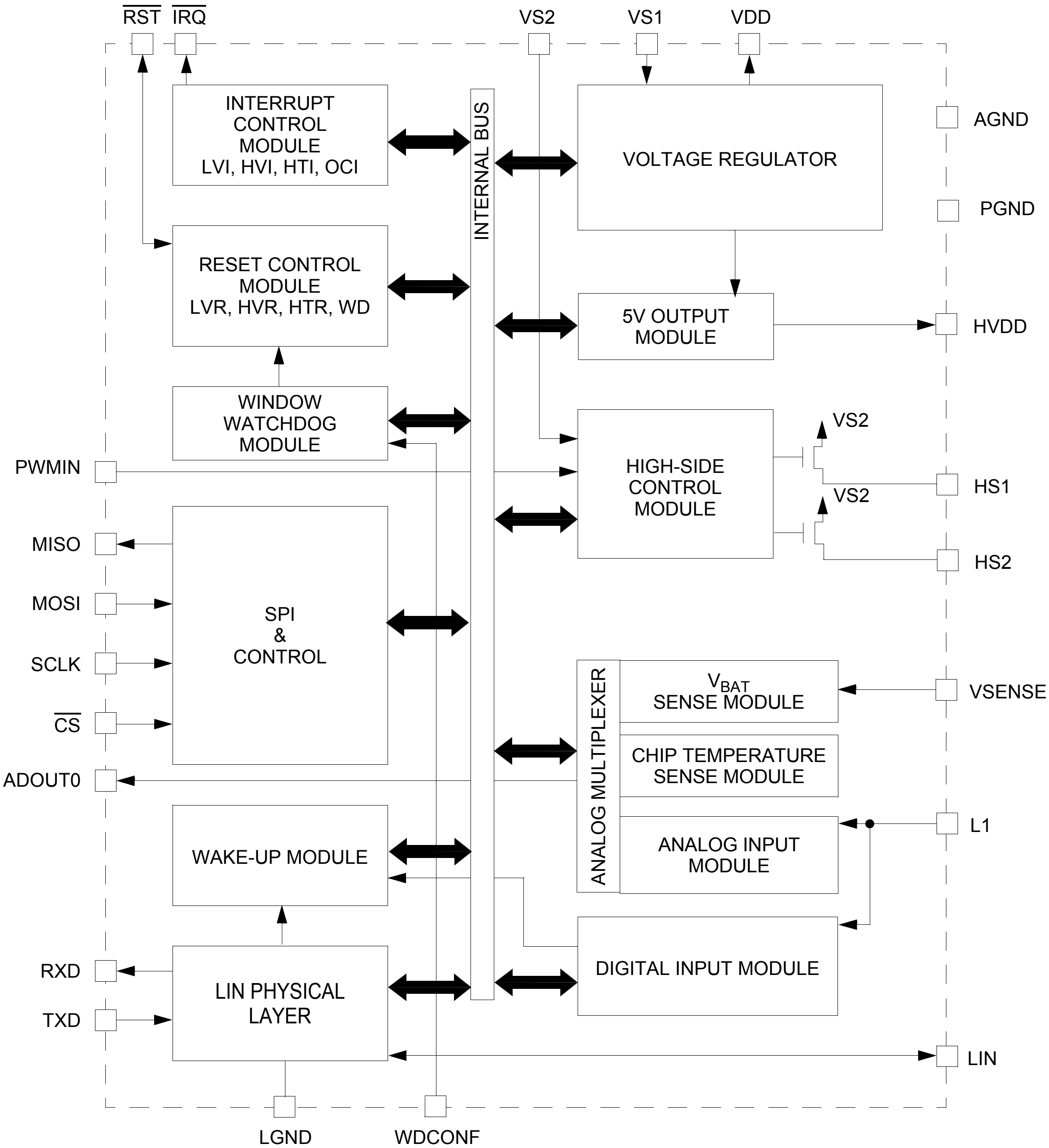


Figure 23. 33910 Simplified internal block diagram

10 Pin connections

10.1 Pinout diagram

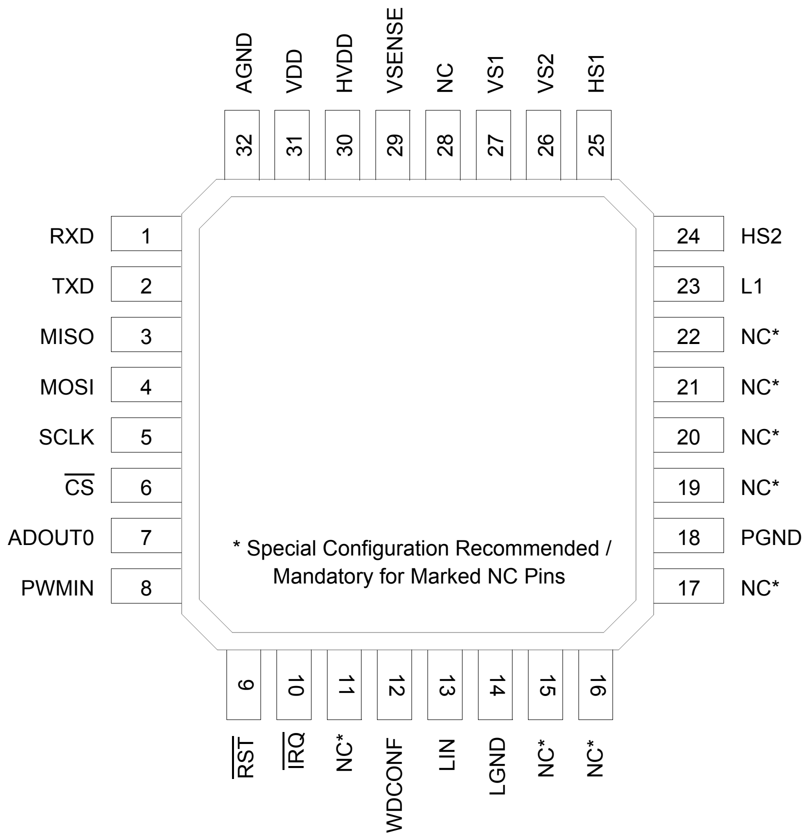


Figure 24. 33910 pin connections

10.2 Pin definitions

A functional description of each pin can be found in the Functional pin description.

Table 31. 33910 pin definitions

Pin	Pin name	Formal name	Definition
1	RXD	Receiver Output	This pin is the receiver output of the LIN interface which reports the state of the bus voltage to the MCU interface.
2	TXD	Transmitter Input	This pin is the transmitter input of the LIN interface which controls the state of the bus output.
3	MISO	SPI Output	SPI data output. When CS is high, the pin is in the high-impedance state.
4	MOSI	SPI Input	SPI data input.
5	SCLK	SPI Clock	SPI clock Input.
6	CS	SPI Chip Select	SPI chip select input pin. CS is active low.
7	ADOUT0	Analog Output Pin 0	Analog multiplexer output.
8	PWMIN	PWM Input	High-side pulse width modulation input.

Table 31. 33910 pin definitions (continued)

Pin	Pin name	Formal name	Definition
9	RST	Internal Reset I/O	Bidirectional reset I/O pin - driven low when any internal reset source is asserted. RST is active low.
10	IRQ	Internal Interrupt Output	Interrupt output pin, indicating wake-up events from Stop mode or events from Normal and Normal Request modes. IRQ is active low.
11, 15-17, 19-22, 28	NC		No connect
12	WDCONF	Watchdog Configuration Pin	This input pin is for configuration of the watchdog period and allows the disabling of the watchdog.
13	LIN	LIN Bus	This pin represents the single-wire bus transmitter and receiver.
14	LGND	LIN Ground Pin	This pin is the device LIN ground connection. It is internally connected to the PGND pin.
18	PGND	Power Ground Pin	This pin is the device power ground connection. It is internally connected to the LGND pin.
23	L1	Wake-up Input	This pin is a wake-up capable digital input [(71)]. In addition, L1 can be sensed analog via the analog multiplexer.
24, 25	HS2, HS1	High-side Outputs	High-side switch outputs.
26, 27	VS2, VS1	Power Supply Pin	These pins are device battery level power supply pins. VS2 is supplying the HS1 driver while VS1 supplies the remaining blocks.[(72)]
29	VSENSE	Voltage Sense Pin	Battery voltage sense input.[(73)]
30	HVDD	Hall Sensor Supply Output	+5.0 V switchable supply output pin.[(74)]
31	VDD	Voltage Regulator Output	+5.0 V main voltage regulator output pin.[(75)]
32	AGND	Analog Ground Pin	This pin is the device analog ground connection.

Notes

71. When used as digital input, a series 33 kΩ resistor must be used to protect against automotive transients.
72. Reverse battery protection series diodes must be used externally to protect the internal circuitry.
73. This pin can be connected directly to the battery line for voltage measurements. The pin is self protected against reverse battery connections. It is strongly recommended to connect a 10 kΩ resistor in series with this pin for protection purposes.
74. External capacitor (1.0 μF < C < 10 μF; 0.1 Ω < ESR < 5.0 Ω) required.
75. External capacitor (2.0 μF < C < 100 μF; 0.1 Ω < ESR < 10 Ω) required.

11 Electrical characteristics

11.1 Maximum ratings

Table 32. Maximum ratings

All voltages are with respect to ground, unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Symbol	Ratings	Value	Unit	Notes
Electrical ratings				
$V_{SUP(SS)}$ $V_{SUP(PK)}$	Supply Voltage at VS1 and VS2 • Normal Operation (DC) • Transient Conditions (load dump)	-0.3 to 27 -0.3 to 40	V	
V_{DD}	Supply Voltage at VDD	-0.3 to 5.5	V	
V_{IN} $V_{IN(IRQ)}$	Input / Output Pins Voltage • $\overline{CS}$, $\overline{RST}$, SCLK, PWMIN, ADOUT0, MOSI, MISO, TXD, RXD • Interrupt Pin ($\overline{IRQ}$)	-0.3 to V_{DD}+0.3 -0.3 to 11	V	(76) (77)
V_{HS1}	HS1 Pin Voltage (DC)	-0.3 to V_{SUP}+0.3	V	
V_{HS2}	HS2 Pin Voltage (DC)	-0.3 to V_{SUP}+0.3	V	
V_{L1DC} V_{L1TR}	L1 Pin Voltage • Normal Operation with a series 33 kΩ resistor (DC) • Transient input voltage with external component (according to ISO7637-2) (See Figure 26)	-18 to 40 ±100	V	
V_{VSENSE}	VSENSE Pin Voltage (DC)	-27 to 40	V	
V_{BUSDC} V_{BUSTR}	LIN Pin Voltage • Normal Operation (DC) • Transient input voltage with external component (according to ISO7637-2) (See Figure 26)	-18 to 40 -150 to 100	V	
I_{VDD}	VDD output current	Internally Limited	A	
V_{ESD1-1} V_{ESD1-2} V_{ESD2} V_{ESD3-1} V_{ESD3-2}	ESD Voltage • Human Body Model - LIN Pin • Human Body Model - all other Pins • Machine Model • Charge Device Model • Corner Pins (Pins 1, 8, 9, 16, 17, 24, 25, and 32) • All other Pins (Pins 2-7, 10-15, 18-23, 26-31)	±8000 ±2000 ±150 ±750 ±500	V	(78)
V_{NC}	NC Pin Voltage (NC pins 11, 15, 16, 17, 19, 20, 21, 22, and 28)	Note 79		(79)

Notes

76. Exceeding voltage limits on specified pins may cause a malfunction or permanent damage to the device.
77. Extended voltage range for programming purpose only.
78. Testing is performed in accordance with the Human Body Model (C_{ZAP} = 100 pF, R_{ZAP} = 1500 Ω), the Machine Model (C_{ZAP} = 200 pF, R_{ZAP} = 0 Ω), and the Charge Device Model, Robotic (C_{ZAP} = 4.0 pF).
79. Special configuration recommended / mandatory for marked NC pins. Please refer to the typical application.

Table 32. Maximum ratings (continued)

All voltages are with respect to ground, unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Symbol	Ratings	Value	Unit	Notes
Thermal ratings				
T_A	Operating Ambient Temperature • 33910 • 34910	 -40 to 125 -40 to 85	°C	(80)
T_J	Operating Junction Temperature	-40 to 150	°C	(80)
T_{STG}	Storage Temperature	-55 to 150	°C	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient • Natural Convection, Single Layer board (1s) • Natural Convection, Four Layer board (2s2p)	 85 56	°C/W	(81), (82) (81), (83)
$R_{\theta JC}$	Thermal Resistance, Junction to Case	23	°C/W	(84)
T_{PPRT}	Peak Package Reflow Temperature During Reflow	Note 86	°C	(85), (86)

Notes

80. The limiting factor is junction temperature; taking into account the power dissipation, thermal resistance, and heat sinking.
81. Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
82. Per JEDEC JESD51-2 with the single layer board (JESD51-3) horizontal.
83. Per JEDEC JESD51-6 with the board (JESD51-7) horizontal.
84. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
85. Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
86. NXP's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL), Go to www.NXP.com, search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts. (i.e. MC33xxxD enter 33xxx), and review parametrics.

11.2 Static electrical characteristics

Table 33. Static electrical characteristics

Characteristics noted under conditions 5.5 V ≤ V_{SUP} ≤ 18 V, -40 °C ≤ T_A ≤ 125 °C for the 33910 and -40 °C ≤ T_A ≤ 85 °C for the 34910, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
Supply voltage range (VS1, VS2)						
V_{SUP}	Nominal Operating Voltage	5.5	–	18	V	
V_{SUPOP}	Functional Operating Voltage	–	–	27	V	(87)
V_{SUPLD}	Load Dump	–	–	40	V	
Supply current range (V_{SUP} = 13.5 V)						
I_{RUN}	Normal Mode (I_{OUT} at V_{DD} = 10 mA), LIN Recessive State	–	4.5	10	mA	(88)
I_{STOP}	Stop Mode, VDD ON with I_{OUT} = 100 µA, LIN Recessive State • 5.5 V < V_{SUP} < 12 V • V_{SUP} = 13.5 V	– –	48 58	80 90	µA	(88), (89), (90)
I_{SLEEP}	Sleep Mode, VDD OFF, LIN Recessive State • 5.5 V < V_{SUP} < 12 V • 12 V ≤ V_{SUP} < 13.5 V	– –	27 37	35 48	µA	(88), (90)
I_{CYCLIC}	Cyclic Sense Supply Current Adder	–	10	–	µA	(91)
Supply under/overvoltage detections						
$V_{BATFAIL}$ $V_{BATFAIL\_HYS}$	Power-On Reset (BATFAIL) • Threshold (measured on VS1) • Hysteresis (measured on VS1)	1.5 –	3.0 0.9	3.9 –	V	(92), (91)
V_{SUV} V_{SUV_HYS}	V_{SUP} undervoltage detection (VSUV Flag) (Normal and Normal Request modes, Interrupt Generated) • Threshold (measured on VS1) • Hysteresis (measured on VS1)	5.55 –	6.0 1.0	6.6 –	V	
V_{SOV} V_{SOV_HYS}	V_{SUP} overvoltage detection (VSOV Flag) (Normal and Normal Request modes, Interrupt Generated) • Threshold (measured on VS1) • Hysteresis (measured on VS1)	18 –	19.25 1.0	20.5 –	V	

Notes

87. Device is fully functional. All features are operating.
88. Total current (I_{VS1} + I_{VS2}) measured at GND pins excluding all loads, Cyclic Sense disabled.
89. Total I_{DD} current (including loads) below 100 µA.
90. Stop and Sleep mode currents increases if V_{SUP} exceeds 13.5 V.
91. This parameter is guaranteed by process monitoring but, not production tested.
92. The flag is set during power up sequence. To clear the flag, a SPI read must be performed.

Table 33. Static electrical characteristics (continued)

Characteristics noted under conditions 5.5 V ≤ V_{SUP} ≤ 18 V, -40 °C ≤ T_A ≤ 125 °C for the 33910 and -40 °C ≤ T_A ≤ 85 °C for the 34910, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
Voltage regulator (93) (VDD)						
V_{DDRUN}	Normal Mode Output Voltage • 1.0 mA < I_{VDD} < 50 mA; 5.5 V < V_{SUP} < 27 V	4.75	5.00	5.25	V	
I_{VDDRUN}	Normal Mode Output Current Limitation	60	110	200	mA	
V_{DDDROP}	Dropout Voltage • I_{VDD} = 50 mA	–	0.1	0.25	V	(94)
V_{DDSTOP}	Stop Mode Output Voltage • I_{VDD} < 5.0 mA	4.75	5.0	5.25	V	
$I_{VDDSTOP}$	Stop Mode Output Current Limitation	6.0	12	36	mA	
LR_{RUN} LR_{STOP}	Line Regulation • Normal mode, 5.5 V < V_{SUP} < 18 V; I_{VDD} = 10 mA • Stop mode, 5.5 V < V_{SUP} < 18 V; I_{VDD} = 1.0 mA	– –	20 5.0	25 25	mV	
LD_{RUN} LD_{STOP}	Load Regulation • Normal mode, 1.0 mA < I_{VDD} < 50 mA • Stop mode, 0.1 mA < I_{VDD} < 5.0 mA	– –	15 10	80 50	mV	
T_{PRE}	Overtemperature Prewarning (Junction) • Interrupt generated, Bit VDDOT Set	110	125	140	°C	(95)
T_{PRE_HYS}	Overtemperature Prewarning hysteresis	–	10	–	°C	(95)
T_{SD}	Overtemperature Shutdown Temperature (Junction)	155	170	185	°C	(95)
T_{SD_HYS}	Overtemperature Shutdown hysteresis	–	10	–	°C	(95)
Hall sensor supply output (96) (HVDD)						
H_{VDDACC}	V_{DD} Voltage matching H_{VDDACC} = (H_{VDD}-V_{DD}) / V_{DD} * 100% • I_{HVDD} = 15 mA	-2.0	–	2.0	%	
I_{HVDD}	Current Limitation	20	30	50	mA	
$H_{VDDDROP}$	Dropout Voltage • I_{HVDD} = 15 mA; I_{VDD} = 5.0 mA	–	160	300	mV	
LR_{HVDD}	Line Regulation • I_{HVDD} = 5.0 mA; I_{VDD} = 5.0 mA	–	25	40	mV	
LD_{HVDD}	Load Regulation • 1.0 mA > I_{HVDD} > 15 mA; I_{VDD} = 5.0 mA	–	10	20	mV	

Notes

93. Specification with external capacitor 2.0 μF < C < 100 μF and 100 mΩ ≤ ESR ≤ 10 Ω.
94. Measured when voltage has dropped 250 mV below its nominal Value (5.0 V).
95. This parameter is guaranteed by process monitoring but, not production tested.
96. Specification with external capacitor 1.0 μF < C < 10 μF and 100 mΩ ≤ ESR ≤ 10 Ω.

Table 33. Static electrical characteristics (continued)

Characteristics noted under conditions 5.5 V ≤ V_{SUP} ≤ 18 V, -40 °C ≤ T_A ≤ 125 °C for the 33910 and -40 °C ≤ T_A ≤ 85 °C for the 34910, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
$\overline{RST}$ input/output pin ($\overline{RST}$)						
$V_{\overline{RST}TH}$	VDD Low Voltage Reset Threshold	4.3	4.5	4.7	V	
V_{OL}	Low-state Output Voltage • I_{OUT} = 1.5 mA; 3.5 V ≤ V_{SUP} ≤ 27 V	0.0	–	0.9	V	
I_{OH}	High-state Output Current (0 < V_{OUT} < 3.5 V)	-150	-250	-350	µA	
I_{PD_MAX}	Pull-down Current Limitation (internally limited) V_{OUT} = V_{DD}	1.5	–	8.0	mA	
V_{IL}	Low-state Input Voltage	-0.3	–	0.3 x V_{DD}	V	
V_{IH}	High-state Input Voltage	0.7 x V_{DD}	–	V_{DD} + 0.3	V	
MISO SPI output pin (MISO)						
V_{OL}	Low-state Output Voltage • I_{OUT} = 1.5 mA	0.0	–	1.0	V	
V_{OH}	High-state Output Voltage • I_{OUT} = -250 µA	V_{DD} - 0.9	–	V_{DD}	V	
$I_{TRIMISO}$	Tri-state Leakage Current • 0 V ≤ V_{MISO} ≤ V_{DD}	-10	–	10	µA	
SPI input pins (MOSI, SCLK, $\overline{CS}$)						
V_{IL}	Low-state Input Voltage	-0.3	–	0.3 x V_{DD}	V	
V_{IH}	High-state Input Voltage	0.7 x V_{DD}	–	V_{DD} + 0.3	V	
I_{IN}	MOSI, SCLK Input Current • 0 V ≤ V_{IN} ≤ V_{DD}	-10	–	10	µA	
$I_{PU\overline{CS}}$	$\overline{CS}$ Pull-up current • 0 V < V_{IN} < 3.5 V	10	20	30	µA	
Interrupt output pin ($\overline{IRQ}$)						
V_{OL}	Low-state Output Voltage • I_{OUT} = 1.5 mA	0.0	–	0.8	V	
V_{OH}	High-state Output Voltage • I_{OUT} = -250 µA	V_{DD} - 0.8	–	V_{DD}	V	
V_{OH}	Leakage current • V_{DD} ≤ V_{OUT} ≤ 10 V	–	–	2.0	mA	
Pulse width modulation input pin (PWMIN)						
V_{IL}	Low-state Input Voltage	-0.3	–	0.3 x V_{DD}	V	
V_{IH}	High-state Input Voltage	0.7 x V_{DD}	–	V_{DD} + 0.3	V	
$I_{PUPWMIN}$	Pull-up current • 0 V < V_{IN} < 3.5 V	10	20	30	µA	

Table 33. Static electrical characteristics (continued)

Characteristics noted under conditions 5.5 V ≤ V_{SUP} ≤ 18 V, -40 °C ≤ T_A ≤ 125 °C for the 33910 and -40 °C ≤ T_A ≤ 85 °C for the 34910, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
High-side output HS1 and HS2 pins (HS1, HS2)						
$R_{DS(on)}$	Output Drain-to-Source On Resistance • T_J = 25 °C, I_{LOAD} = 50 mA; V_{SUP} > 9.0 V • T_J = 150 °C, I_{LOAD} = 50 mA; V_{SUP} > 9.0 V • T_J = 150 °C, I_{LOAD} = 30 mA; 5.5 V < V_{SUP} < 9.0 V	– – –	– – –	7.0 10 14	Ω	(97)
I_{LIMHS1}	Output Current Limitation • 0 V < V_{OUT} < V_{SUP} - 2.0 V	60	120	250	mA	(98)
I_{OLHSx}	Open Load Current Detection	–	5.0	7.5	mA	(99)
I_{LEAK}	Leakage Current (-0.2 V < V_{HSx} < V_{S2} + 0.2 V)	–	–	10	µA	
V_{THSC}	Short-circuit Detection Threshold • 5.5 V < V_{SUP} < 27 V	V_{SUP} - 2	–	–	V	(100)
T_{HSSD}	Overtemperature Shutdown	150	165	180	°C	(101), (102)
T_{HSSD_HYS}	Overtemperature Shutdown Hysteresis	–	10	–	°C	(102)
L1 input pin (L1)						
V_{THL}	Low Detection Threshold • 5.5 V < V_{SUP} < 27 V	2.0	2.5	3.0	V	
V_{THH}	High Detection Threshold • 5.5 V < V_{SUP} < 27 V	3.0	3.5	4.0	V	
V_{HYS}	Hysteresis • 5.5 V < V_{SUP} < 27 V	0.5	1.0	1.5	V	
I_{IN}	Input Current • -0.2 V < V_{IN} < VS1	-10	–	10	µA	(103)
R_{L1IN}	Analog Input Impedance	800	1550	–	kΩ	(104)
$RATIO_{L1}$	Analog Input Divider Ratio ($RATIO_{L1}$ = V_{L1} / V_{ADOUT0}) • L1DS (L1 Divider Select) = 0 • L1DS (L1 Divider Select) = 1	0.95 3.42	1.0 3.6	1.05 3.78		
$V_{RATIOL1-OFFSET}$	Analog Output Offset Ratio • L1DS (L1 Divider Select) = 0 • L1DS (L1 Divider Select) = 1	-80 -22	0.0 0.0	80 22	mV	
$L1_{MATCHING}$	Analog Inputs Matching • L1DS (L1 Divider Select) = 0 • L1DS (L1 Divider Select) = 1	96 96	100 100	104 104	%	

Notes

97. This parameter is production tested up to T_A = 125 °C and guaranteed by process monitoring up to T_J = 150 °C.
98. When overcurrent occurs, the high-side stays ON with limited current capability and the HS1CL flag is set in the HSSR.
99. When open-load occurs, the flag (HS1OP) is set in the HSSR.
100. When short circuit occurs and if HVSE flag is enabled, HS1 automatic shutdown.
101. When overtemperature shutdown occurs, both high-sides are turned off. All flags in HSSR are set.
102. Guaranteed by characterization but, not production tested
103. Analog multiplexer input disconnected from L1 input pin.
104. Analog multiplexer input connected to L1 input pin.

Table 33. Static electrical characteristics (continued)

Characteristics noted under conditions 5.5 V ≤ V_{SUP} ≤ 18 V, -40 °C ≤ T_A ≤ 125 °C for the 33910 and -40 °C ≤ T_A ≤ 85 °C for the 34910, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
Window watchdog configuration pin (WDCONF)						
R_{EXT}	External Resistor Range	20	–	200	kΩ	
WD_{ACC}	Watchdog Period Accuracy with External Resistor (Excluding Resistor Accuracy)	-15	–	15	%	(105)
Analog multiplexer						
S_{TTOV}	Internal Chip Temperature Sense Gain	–	10.5	–	mV/K	
$RATIO_{VSENSE}$	VSENSE Input Divider Ratio ($RATIO_{VSENSE}$ = V_{VSENSE} / V_{ADOUT0}) • 5.5 V < V_{SUP} < 27 V	5.0	5.25	5.5		
$OFFSET_{VSENSE}$	VSENSE Output Related Offset • -40 °C < T_A < -20 °C	-30 -45	– –	30 45	mV	
Analog output (ADOUT0)						
V_{OUT_MAX}	Maximum Output Voltage • -5.0 mA < I_O < 5.0 mA	V_{DD} - 0.35	–	V_{DD}	V	
V_{OUT_MIN}	Minimum Output Voltage • -5.0 mA < I_O < 5.0 mA	0.0	–	0.35	V	
RXD output pin (LIN physical layer) (RXD)						
V_{OL}	Low-state Output Voltage • I_{OUT} = 1.5 mA	0.0	–	0.8	V	
V_{OH}	High-state Output Voltage • I_{OUT} = -250 µA	V_{DD}-0.8	–	V_{DD}	V	
TXD input pin (LIN physical layer) (TXD)						
V_{IL}	Low-state Input Voltage	-0.3	–	0.3 x nV_{DD}	V	
V_{IH}	High-state Input Voltage	0.7 x V_{DD}	–	V_{DD} + 0.3	V	
I_{PUIN}	Pin Pull-up Current, 0 < V_{IN} < 3.5 V	10	20	30	µA	

Notes

105. Watchdog timing period calculation formula: t_{PWD} [ms] = 0.466 * (R_{EXT} - 20) + 10 (R_{EXT} in kΩ)

Table 33. Static electrical characteristics (continued)

Characteristics noted under conditions 5.5 V ≤ V_{SUP} ≤ 18 V, -40 °C ≤ T_A ≤ 125 °C for the 33910 and -40 °C ≤ T_A ≤ 85 °C for the 34910, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
LIN physical layer, transceiver (LIN)[106]						
I_{BUSLIM}	Output Current Limitation • Dominant State, V_{BUS} = 18 V	40	120	200	mA	
 $I_{BUS\_PAS\_DOM}$ $I_{BUS\_PAS\_REC}$ $I_{BUS\_NO\_GND}$ I_{BUS}	Leakage Output Current to GND • Dominant State; V_{BUS} = 0 V; V_{BAT} = 12 V • Recessive State; 8.0 V < V_{BAT} < 18 V; 8.0 V < V_{BUS} < 18 V; V_{BUS} ≥ V_{BAT} • GND Disconnected; GND_{DEVICE} = V_{SUP}; V_{BAT} = 12 V; 0 < V_{BUS} < 18 V • V_{BAT} disconnected; V_{SUP_DEVICE} = GND; 0 < V_{BUS} < 18 V	 -1.0 – -1.0 –	 – – – –	 – 20 1.0 100	 mA µA mA µA	
 V_{BUSDOM} V_{BUSREC} V_{BUS_CNT} V_{HYS}	Receiver Input Voltages • Receiver Dominant State • Receiver Recessive State • Receiver Threshold Center (V_{TH_DOM} + V_{TH_REC})/2 • Receiver Threshold Hysteresis (V_{TH_REC} - V_{TH_DOM})	 – 0.6 0.475 –	 – – 0.5 –	 0.4 – 0.525 0.175	V_{SUP}	
 V_{LIN_REC} $V_{LIN\_DOM\_0}$ $V_{LIN\_DOM\_1}$	LIN Transceiver Output Voltage • Recessive State, TXD HIGH, I_{OUT} = 1.0 µA • Dominant State, TXD LOW, 500 Ω External Pull-up Resistor, LDVS = 0 • Dominant State, TXD LOW, 500 Ω External Pull-up Resistor, LDVS = 1	 V_{SUP}-1 – –	 – 1.1 1.7	 – 1.4 2.0	V	
R_{SLAVE}	LIN Pull-up Resistor to V_{SUP}	20	30	60	kΩ	
T_{LINSD}	Overtemperature Shutdown	150	165	180	°C	(107)
T_{LINSD_HYS}	Overtemperature Shutdown Hysteresis	–	10	–	°C	

Notes

106. Parameters guaranteed for 7.0 V ≤ V_{SUP} ≤ 18 V.

107. When Overtemperature shutdown occurs, the LIN bus goes in recessive state and the flag LINOT in LINSR is set.

11.3 Dynamic electrical characteristics

Table 34. Dynamic electrical characteristics

Characteristics noted under conditions 5.5 V ≤ V_{SUP} ≤ 18 V, -40 °C ≤ T_A ≤ 125 °C for the 33910 and -40 °C ≤ T_A ≤ 85 °C for the 34910, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
SPI interface timing (Figure 34)						
f_{SPIOP}	SPI Operating Frequency	–	–	4.0	MHz	
t_{PSCLK}	SCLK Clock Period	250	–	N/A	ns	
t_{WSCLKH}	SCLK Clock High Time	110	–	N/A	ns	(108)
t_{WSCLKL}	SCLK Clock Low Time	110	–	N/A	ns	(108)
t_{LEAD}	Falling Edge of $\overline{CS}$ to Rising Edge of SCLK	100	–	N/A	ns	(108)
t_{LAG}	Falling Edge of SCLK to $\overline{CS}$ Rising Edge	100	–	N/A	ns	(108)
t_{SISU}	MOSI to Falling Edge of SCLK	40	–	N/A	ns	(108)
t_{SIH}	Falling Edge of SCLK to MOSI	40	–	N/A	ns	(108)
t_{RSO}	MISO Rise Time • C_L = 220 pF	–	40	–	ns	(108)
t_{FSO}	MISO Fall Time • C_L = 220 pF	–	40	–	ns	(108)
t_{SOEN} t_{SODIS}	Time from Falling or Rising Edges of $\overline{CS}$ to: • MISO Low-impedance • MISO High-impedance	0.0 0.0	– –	50 50	ns	(108)
t_{VALID}	Time from Rising Edge of SCLK to MISO Data Valid • 0.2 x V_{DD} ≤ MISO ≥ 0.8 x V_{DD}, C_L = 100 pF	0.0	–	75	ns	(108)
$\overline{RST}$ output pin						
$t_{\overline{RST}}$	Reset Low-level Duration after V_{DD} High (See Figure 33)	0.65	1.0	1.35	ms	
$t_{\overline{RSTDF}}$	Reset Deglitch Filter Time	350	600	900	ns	
Window watchdog configuration pin (WDCONF)						
t_{PWD}	Watchdog Time Period • External Resistor R_{EXT} = 20 kΩ (1%) • External Resistor R_{EXT} = 200 kΩ (1%) • Without External Resistor R_{EXT} (WDCONF Pin Open)	8.5 79 110	10 94 150	11.5 108 205	ms	(109)

Notes

108. This parameter is guaranteed by process monitoring but, not production tested.
109. Watchdog timing period calculation formula: t_{PWD} [ms] = 0.466 * (R_{EXT} - 20) + 10 (R_{EXT} in kΩ)

Table 34. Dynamic electrical characteristics (continued)

Characteristics noted under conditions 5.5 V ≤ V_{SUP} ≤ 18 V, -40 °C ≤ T_A ≤ 125 °C for the 33910 and -40 °C ≤ T_A ≤ 85 °C for the 34910, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
L1 input						
t_{WUF}	Wake-up Filter Time	8.0	20	38	µs	
State machine timing						
t_{STOP}	Delay Between $\overline{CS}$ LOW-to-HIGH Transition (at End of SPI Stop Command) and Stop Mode Activation	–	–	5.0	µs	(110)
t_{NRTOUT}	Normal Request Mode Timeout (see Figure 33)	110	150	205	ms	
$t_{S\text{-}ON}$	Delay Between SPI Command and HS Turn On • 9.0 V < V_{SUP} < 27 V	–	–	10	µs	(111)
$t_{S\text{-}OFF}$	Delay Between SPI Command and HS Turn Off • 9.0 V < V_{SUP} < 27 V	–	–	10	µs	(111)
t_{SNR2N}	Delay Between Normal Request and Normal Mode After a Watchdog Trigger Command (Normal Request mode)	–	–	10	µs	(110)
$t_{WU\overline{CS}}$ t_{WUSPI}	Delay Between $\overline{CS}$ Wake-up ($\overline{CS}$ LOW to HIGH) in Stop Mode and: • Normal Request mode, VDD ON and $\overline{RST}$ HIGH • First Accepted SPI Command	9.0 90	15 —	80 N/A	µs	
$t_{2\overline{CS}}$	Minimum Time Between Rising and Falling Edge on the $\overline{CS}$	4.0	—	—	µs	
LIN physical layer: driver characteristics for normal slew rate - 20.0 kBit/sec (112), (113)						
D1	Duty Cycle 1: D1 = $t_{BUS\_REC(MIN)}/(2 \times t_{BIT})$, t_{BIT} = 50 µs • 7.0 V ≤ V_{SUP} ≤ 18 V	0.396	—	—		
D2	Duty Cycle 2: D2 = $t_{BUS\_REC(MAX)}/(2 \times t_{BIT})$, t_{BIT} = 50 µs • 7.6 V ≤ V_{SUP} ≤ 18 V	—	—	0.581		
LIN physical layer: driver characteristics for slow slew rate - 10.4 kBit/sec (112),(114)						
D3	Duty Cycle 3: D3 = $t_{BUS\_REC(MIN)}/(2 \times t_{BIT})$, t_{BIT} = 96 µs • 7.0 V ≤ V_{SUP} ≤ 18 V	0.417	—	—	µs	
D4	Duty Cycle 4: D4 = $t_{BUS\_REC(MAX)}/(2 \times t_{BIT})$, t_{BIT} = 96 µs • 7.6 V ≤ V_{SUP} ≤ 18 V	—	—	0.590	µs	

Notes

110. This parameter is guaranteed by process monitoring but, not production tested.
111. Delay between turn on or off command (rising edge on $\overline{CS}$) and HS ON or OFF, excluding rise or fall time due to external load.
112. Bus load R_{BUS} and C_{BUS} 1.0 nF / 1.0 kΩ, 6.8 nF / 660 Ω, 10 nF / 500 Ω. Measurement thresholds: 50% of TXD signal to LIN signal threshold defined at each parameter. See Figure 27.
113. See Figure 28.
114. See Figure 29.

Table 34. Dynamic electrical characteristics (continued)

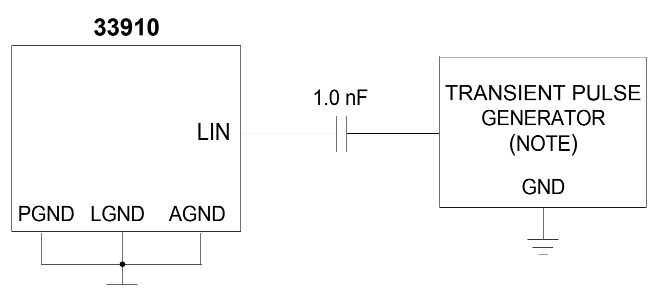
Characteristics noted under conditions 5.5 V $\leq V_{SUP} \leq$ 18 V, -40 °C $\leq T_A \leq$ 125 °C for the 33910 and -40 °C $\leq T_A \leq$ 85 °C for the 34910, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
LIN physical layer: driver characteristics for fast slew rate						
SR_{FAST}	LIN Fast Slew Rate (Programming mode)	—	20	—	V/µs	
LIN physical layer: characteristics and wake-up timings [115]						
 t_{REC_PD} t_{REC_SYM}	Propagation Delay and Symmetry • Propagation Delay Receiver, t_{REC_PD} = max (t_{REC_PDR}, t_{REC_PDF}) • Symmetry of Receiver Propagation Delay t_{REC_PDF} - t_{REC_PDR}	 — -2.0	 3.0 —	 6.0 2.0	µs	[116]
t_{PROPWL}	Bus Wake-up Deglitcher (Sleep and Stop modes)	42	70	95	µs	[117]
 t_{WAKE} t_{WAKE}	Bus Wake-up Event Reported • From Sleep mode • From Stop mode	 — 9.0	 — 13	 1500 17	µs	 [118] [119]
t_{TXDDOM}	TXD Permanent Dominant State Delay	0.65	1.0	1.35	s	
Pulse width modulation input pin (PWMIN)						
f_{PWMIN}	PWMIN pin • Max. frequency to drive HS output pins	—	10	—	kHz	[120]

Notes

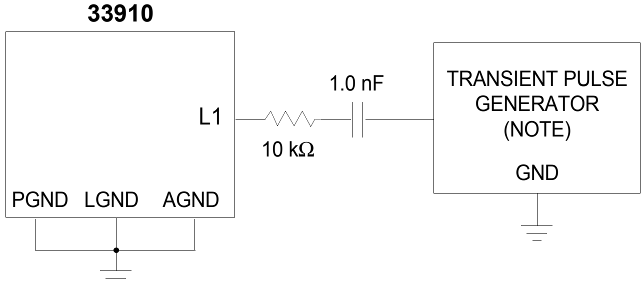
115. V_{SUP} from 7.0 V to 18 V, bus load R_{BUS} and C_{BUS} 1.0 nF / 1.0 kΩ, 6.8 nF / 660 Ω, 10 nF / 500 Ω. Measurement thresholds: 50% of TXD signal to LIN signal threshold defined at each parameter. See Figure 6.
116. See Figure 9.
117. See Figure 10, for Sleep and Figure 11, for Stop mode.
118. The measurement is done with 1.0 µF capacitor and 0 mA current load on V_{DD}. The value takes into account the delay to charge the capacitor. The delay is measured between the bus wake-up threshold (V_{BUSWU}) rising edge of the LIN bus and when V_{DD} reaches 3.0 V. See Figure 10. The delay depends of the load and capacitor on V_{DD}.
119. In Stop mode, the delay is measured between the bus wake-up threshold (V_{BUSWU}) and the falling edge of the $\overline{IRQ}$ pin. See Figure 11.
120. This parameter is guaranteed by process monitoring but, not production tested.

11.4 Timing diagrams



NOTE: Waveform Per ISO 7637-2. Test Pulses 1, 2, 3a, 3b.

Figure 25. Test circuit for transient test pulses (LIN)



NOTE: Waveform Per ISO 7637-2. Test Pulses 1, 2, 3a, 3b.

Figure 26. Test circuit for transient test pulses (L1)

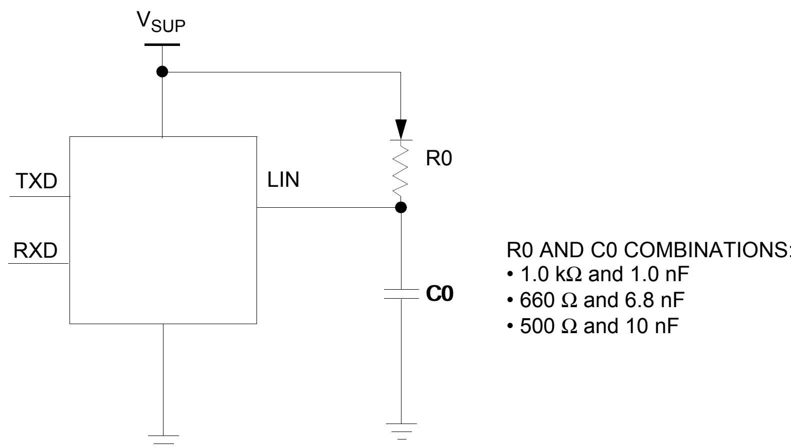


Figure 27. Test circuit for LIN timing measurements

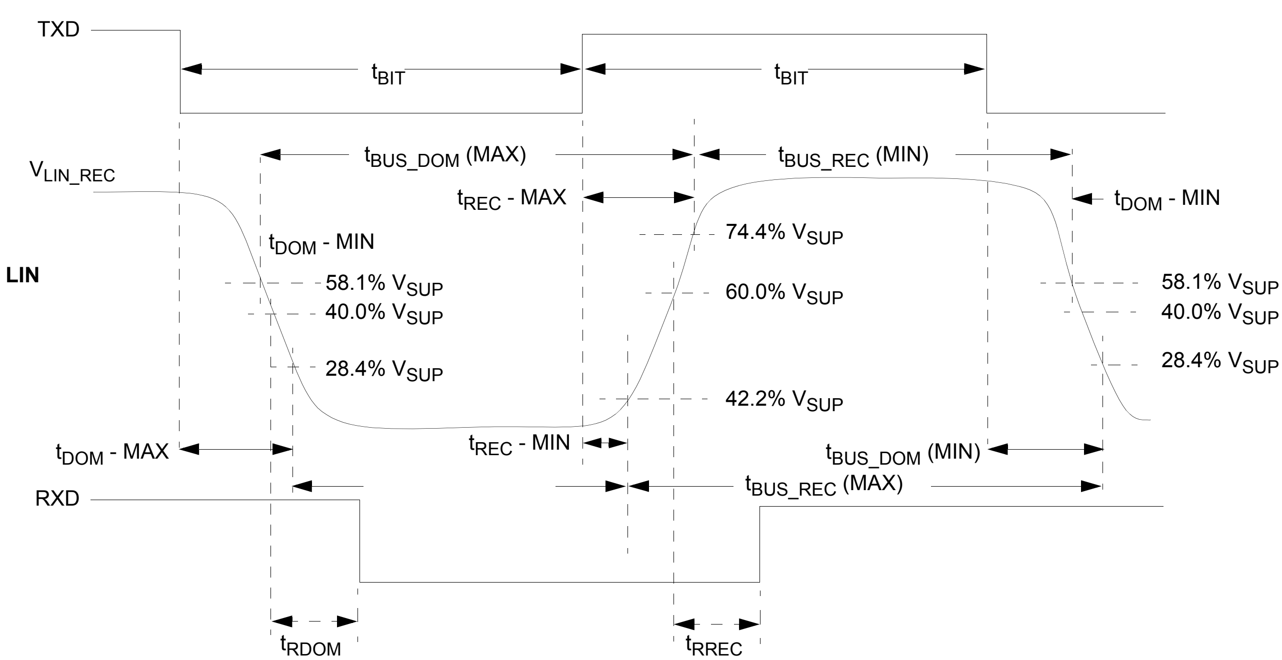


Figure 28. LIN timing measurements for normal slew rate

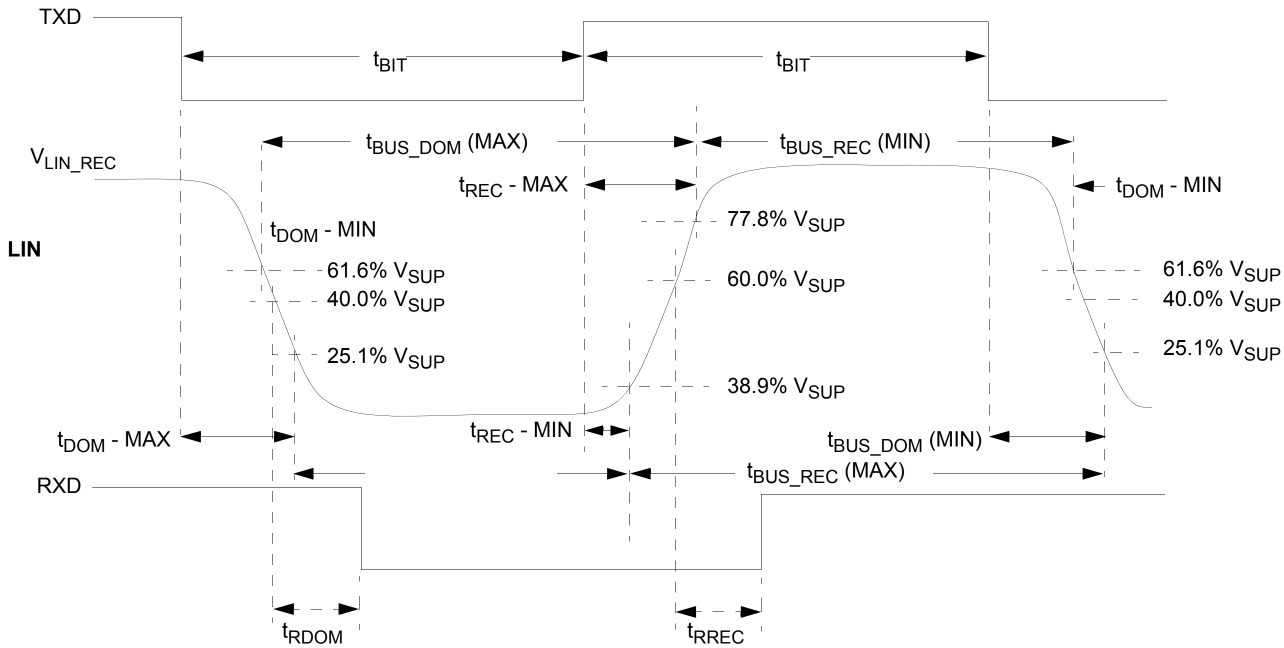


Figure 29. LIN timing measurements for slow slew rate

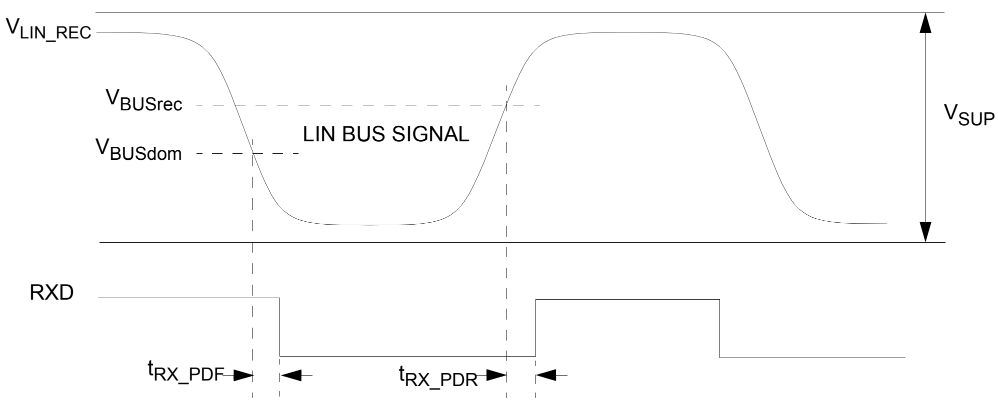


Figure 30. LIN receiver timing

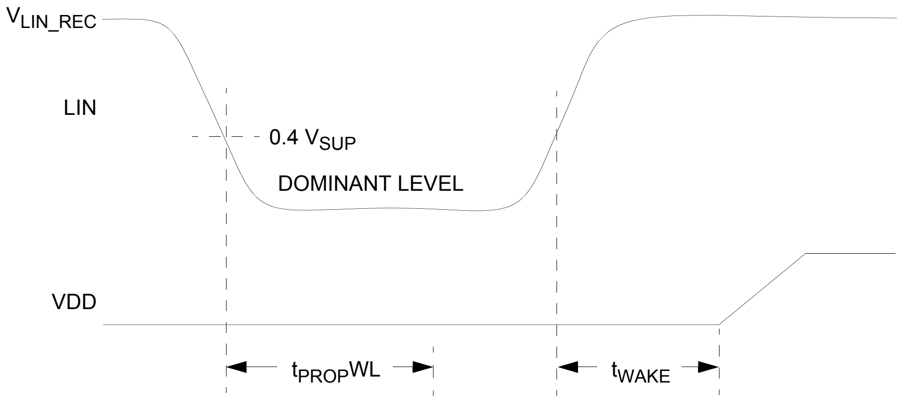


Figure 31. LIN wake-up sleep mode timing

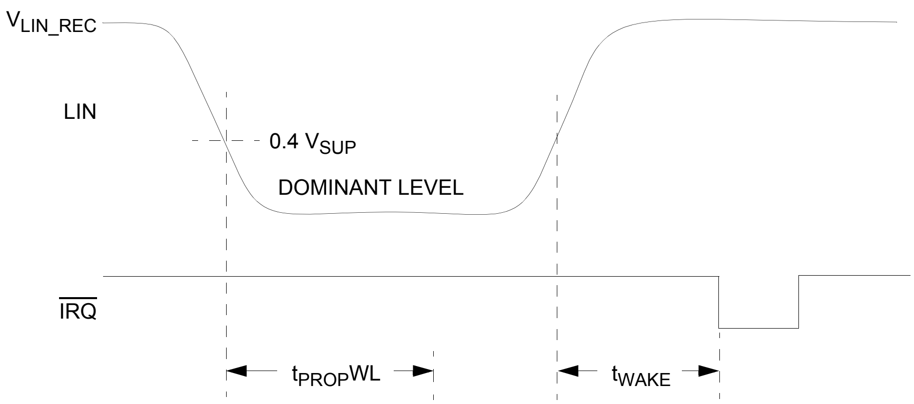


Figure 32. LIN wake-up stop mode timing

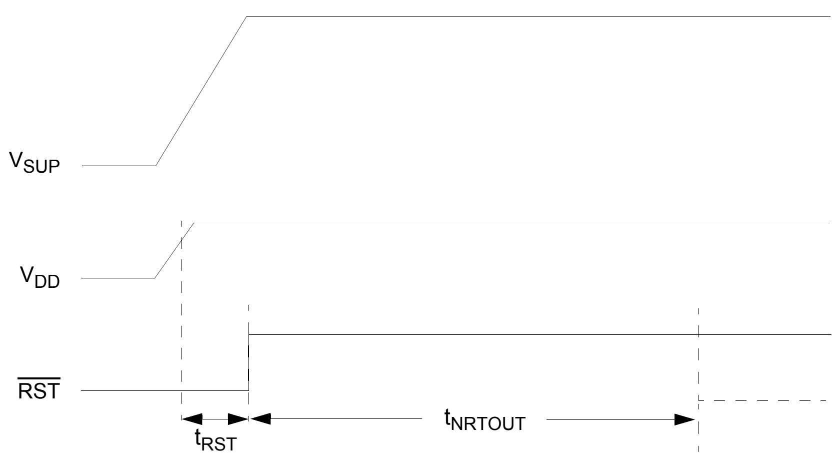


Figure 33. Power on reset and normal request timeout timing

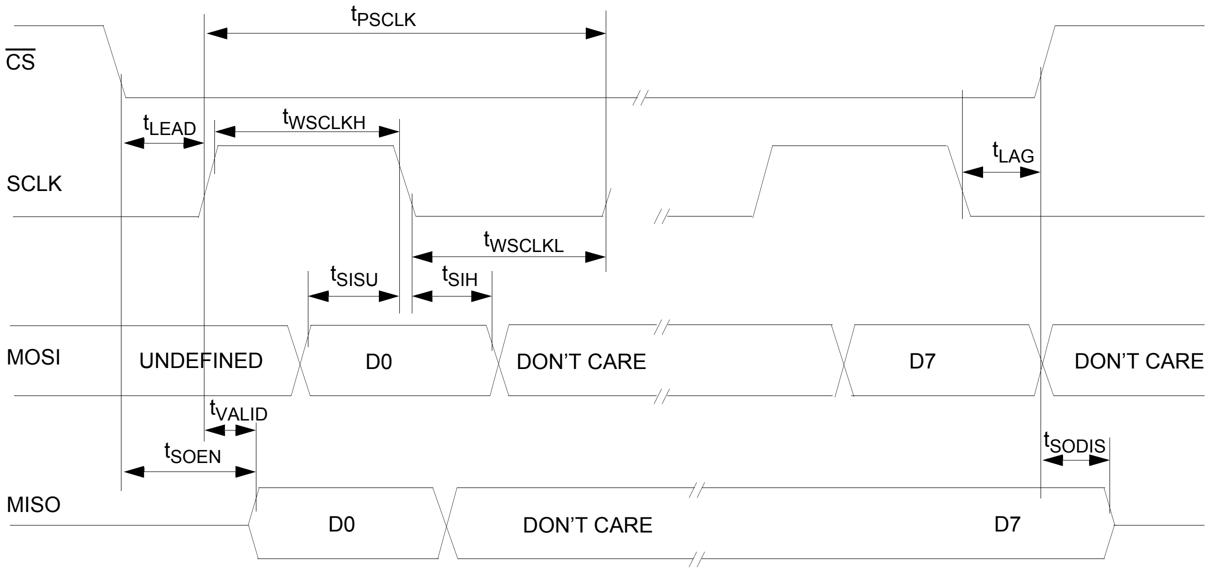


Figure 34. SPI timing characteristics

12 Functional description

12.1 Introduction

The 33910 is designed and developed as a highly integrated and cost-effective solution for automotive and industrial applications. For automotive body electronics, the 33910 is well suited to perform keypad applications via the LIN bus. Two power switches are provided on the device configured as high-side outputs. Other ports are also provided, which include a wake-up capable pin and a Hall Sensor port supply. An internal voltage regulator provides power to a MCU device. Also included in this device is a LIN physical layer, which communicates using a single wire. This enables this device to be compatible with 3-wire bus systems, where one wire is used for communication, one for battery, and one for ground.

12.2 Functional pin description

See Table 1, 33910 simplified application diagram, for a graphic representation of the various pins referred to in the following paragraphs. Also, see the 33910 pin connections for a description of the pin locations in the package.

12.2.1 Receiver output (RXD)

The RXD pin is a digital output. It is the receiver output of the LIN interface and reports the state of the bus voltage: RXD low when LIN bus is dominant, RXD high when LIN bus is recessive.

12.2.2 Transmitter input (TXD)

The TXD pin is a digital input. It is the transmitter input of the LIN interface and controls the state of the bus output (dominant when TXD is Low, recessive when TXD is High). This pin has an internal pull-up to force recessive state in case the input is left floating.

12.2.3 LIN bus (LIN)

The LIN pin represents the single-wire bus transmitter and receiver. It is suited for automotive bus systems and is compliant to the LIN bus specification 2.0. The LIN interface is only active during Normal and Normal Request modes.

12.2.4 Serial data clock (SCLK)

The SCLK pin is the SPI clock input pin. MISO data changes on the negative transition of the SCLK. MOSI is sampled on the positive edge of the SCLK.

12.2.5 Master out slave in (MOSI)

The MOSI digital pin receives SPI data from the MCU. This data input is sampled on the positive edge of SCLK.

12.2.6 Master in slave out (MISO)

The MISO pin sends data to an SPI-enabled MCU. It is a digital tri-state output used to shift serial data to the microcontroller. Data on this output pin changes on the negative edge of the SCLK. When $\overline{CS}$ is High, this pin remains in high-impedance state.

12.2.7 Chip select ($\overline{CS}$)

$\overline{CS}$ is a active low digital input. It must remain low during a valid SPI communication and allow for several devices to be connected in the same SPI bus without contention. A rising edge on $\overline{CS}$ signals the end of the transmission and the moment the data shifted in is latched. A valid transmission must consist of 8 bits only. While in STOP mode a low-to-high level transition on this pin generates a wake-up condition for the 33910.

12.2.8 Analog multiplexer (ADOUT0)

The ADOUT0 pin can be configured via the SPI to allow the MCU A/D converter to read the several inputs of the Analog Multiplexer, including the L1 input voltage and the internal junction temperature.

12.2.9 PWM input control (PWMIN)

This digital input can control the high-sides in Normal Request and Normal mode. To enable PWM control, the MCU must perform a write operation to the high-side control register (HSCR). This pin has an internal 20 µA current pull-up.

12.2.10Reset ($\overline{RST}$)

This bidirectional pin is used to reset the MCU in case the 33910 detects a reset condition, or to inform the 33910 the MCU has just been reset. After release of the $\overline{RST}$ pin Normal Request mode is entered. The $\overline{RST}$ pin is an active low filtered input and output formed by a weak pull-up and a switchable pull-down structure which allows this pin to be shorted either to V_{DD} or to GND during software development without the risk of destroying the driver.

12.2.11Interrupt ($\overline{IRQ}$)

The $\overline{IRQ}$ pin is a digital output used to signal events or faults to the MCU while in Normal and Normal Request mode or to signal a wake-up from Stop mode. This active low output transitions to high, only after the interrupt is acknowledged by a SPI read of the respective status bits.

12.2.12Watchdog configuration (WDCONF)

The WDCONF pin is the configuration pin for the internal watchdog. A resistor can be connected to this pin to configure the window watchdog period. When connected directly to ground, the watchdog is disabled. When this pin is left open, the watchdog period is fixed to its lower precision internal default value (150 ms typical).

12.2.13Ground connection (AGND, PGND, LGND)

The AGND, PGND and LGND pins are the Analog and Power ground pins. The AGND pin is the ground reference of the voltage regulator.

The PGND and LGND pins are used for high current load return as in the LIN interface pin.

Note: PGND, AGND and LGND pins must be connected together.

12.2.14Digital/analog (L1)

The L1 pin is a multi purpose input. It can be used as a digital input, which can be sampled by reading the SPI and used for wake-up when 33910 is in Low Power mode or used as analog inputs for the analog multiplexer. When used to sense voltage outside the module, a 33kohm series resistor must be used on each input.

When used as a wake-up input L1 can be configured to operate in Cyclic-sense mode. In this mode, one of the high-side switches is configured to be periodically turned on and sample the wake-up input. If a state change is detected between two cycles a wake-up is initiated. The 33910 can also wake-up from Stop or Sleep by a simple state change on L1. When used as analog input, the voltage present on the L1 pins is scaled down by an selectable internal voltage divider and can be routed to the ADOUT0 output through the analog multiplexer.

Note: If L1 input is selected in the analog multiplexer, it is disabled as digital input and remains disabled in Low-power mode. No wake-up feature is available in this condition.

When the L1 input is not selected in the analog multiplexer, the voltage divider is disconnected from this input.

12.2.15High-side outputs (HS1 and HS2)

These high-side switches are able to drive loads such as relays or lamps. Their structure is connected to the VS2 supply pin. The pins are short-circuit protected and also protected against overheating. HS1and HS2 are controlled by SPI and can respond to a signal applied to the PWMIN input pin. The HS1 and HS2 outputs can also be used during Low-power mode for the cyclic-sense of the WAKE input.