

## Excellent Integrated System Limited

Stocking Distributor

Click to view price, real time Inventory, Delivery & Lifecycle Information:

[ON Semiconductor](#)  
[NSBA123TDP6T5G](#)

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# NSBA123TDP6

## Dual PNP Bias Resistor Transistors

**R1 = 2.2 kΩ, R2 = ∞ kΩ**

### PNP Transistors with Monolithic Bias Resistor Network

This series of digital transistors is designed to replace a single device and its external resistor bias network. The Bias Resistor Transistor (BRT) contains a single transistor with a monolithic bias network consisting of two resistors; a series base resistor and a base-emitter resistor. The BRT eliminates these individual components by integrating them into a single device. The use of a BRT can reduce both system cost and board space.

#### Features

- Simplifies Circuit Design
- Reduces Board Space
- Reduces Component Count
- S and NSV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- This Device is Pb-Free, Halogen Free/BFR Free and is RoHS Compliant

#### MAXIMUM RATINGS

(T<sub>A</sub> = 25°C, common for Q<sub>1</sub> and Q<sub>2</sub>, unless otherwise noted)

Rating	Symbol	Max	Unit
Collector-Base Voltage	V <sub>CBO</sub>	50	Vdc
Collector-Emitter Voltage	V <sub>CEO</sub>	50	Vdc
Collector Current – Continuous	I <sub>C</sub>	100	mA <sub>dc</sub>
Input Forward Voltage	V <sub>IN(fwd)</sub>	12	Vdc
Input Reverse Voltage	V <sub>IN(rev)</sub>	5	Vdc

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

#### ORDERING INFORMATION

Device	Package	Shipping <sup>†</sup>
NSBA123TDP6T5G	SOT-963	8,000/Tape & Reel

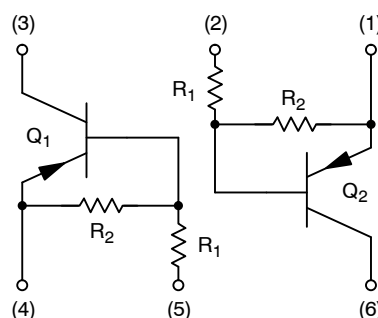
<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



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<http://onsemi.com>

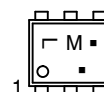
#### PIN CONNECTIONS



#### MARKING DIAGRAM



**SOT-963  
CASE 527AD**



- L = Specific Device Code
- M = Date Code\*
- = Pb-Free Package

(Note: Microdot may be in either location)

\*Date Code orientation may vary depending upon manufacturing location.

## NSBA123TDP6

### THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
<b>NSBA123TDP6 (SOT-963) ONE JUNCTION HEATED</b>			
Total Device Dissipation $T_A = 25^\circ\text{C}$  Derate above $25^\circ\text{C}$	$P_D$    (Note 1) (Note 2) (Note 1) (Note 2)	   231 269 1.9 2.2	   MW mW/ $^\circ\text{C}$
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$  (Note 1) (Note 2)	 540 464	 $^\circ\text{C/W}$
<b>NSBA123TDP6 (SOT-963) BOTH JUNCTION HEATED (Note 3)</b>			
Total Device Dissipation $T_A = 25^\circ\text{C}$  Derate above $25^\circ\text{C}$	$P_D$    (Note 1) (Note 2) (Note 1) (Note 2)	   339 408 2.7 3.3	   MW mW/ $^\circ\text{C}$
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$  (Note 1) (Note 2)	 369 306	 $^\circ\text{C/W}$
Junction and Storage Temperature Range	$T_J, T_{stg}$	-55 to +150	$^\circ\text{C}$

1. FR-4 @ 100 mm<sup>2</sup>, 1 oz. copper traces, still air.

2. FR-4 @ 500 mm<sup>2</sup>, 1 oz. copper traces, still air.

3. Both junction heated values assume total power is sum of two equally powered channels.

## NSBA123TDP6

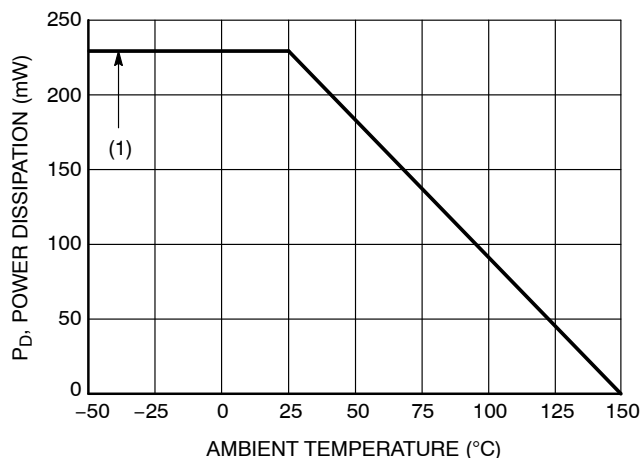
### ELECTRICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ , common for $Q_1$ and $Q_2$ , unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
<b>OFF CHARACTERISTICS</b>					
Collector-Base Cutoff Current ( $V_{CB} = 50\text{ V}$ , $I_E = 0$ )	$I_{CBO}$	–	–	100	nA <sub>dc</sub>
Collector-Emitter Cutoff Current ( $V_{CE} = 50\text{ V}$ , $I_B = 0$ )	$I_{CEO}$	–	–	500	nA <sub>dc</sub>
Emitter-Base Cutoff Current ( $V_{EB} = 6.0\text{ V}$ , $I_C = 0$ )	$I_{EBO}$	–	–	4.0	mA <sub>dc</sub>
Collector-Base Breakdown Voltage ( $I_C = 10\text{ }\mu\text{A}$ , $I_E = 0$ )	$V_{(BR)CBO}$	50	–	–	V <sub>dc</sub>
Collector-Emitter Breakdown Voltage (Note 4) ( $I_C = 2.0\text{ mA}$ , $I_B = 0$ )	$V_{(BR)CEO}$	50	–	–	V <sub>dc</sub>

### ON CHARACTERISTICS

DC Current Gain (Note 4) ( $I_C = 5.0\text{ mA}$ , $V_{CE} = 10\text{ V}$ )	$h_{FE}$	160	350	–	
Collector-Emitter Saturation Voltage (Note 4) ( $I_C = 10\text{ mA}$ , $I_B = 0.3\text{ mA}$ )	$V_{CE(sat)}$	–	–	0.25	V
Input Voltage (Off) ( $V_{CE} = 5.0\text{ V}$ , $I_C = 100\text{ }\mu\text{A}$ )	$V_{i(off)}$	–	0.6	–	V <sub>dc</sub>
Input Voltage (On) ( $V_{CE} = 0.2\text{ V}$ , $I_C = 10\text{ mA}$ )	$V_{i(on)}$	–	0.9	–	V <sub>dc</sub>
Output Voltage (On) ( $V_{CC} = 5.0\text{ V}$ , $V_B = 2.5\text{ V}$ , $R_L = 1.0\text{ k}\Omega$ )	$V_{OL}$	–	–	0.2	V <sub>dc</sub>
Output Voltage (Off) ( $V_{CC} = 5.0\text{ V}$ , $V_B = 0.5\text{ V}$ , $R_L = 1.0\text{ k}\Omega$ )	$V_{OH}$	4.9	–	–	V <sub>dc</sub>
Input Resistor	$R_1$	1.5	2.2	2.9	k $\Omega$
Resistor Ratio	$R_1/R_2$	–	–	–	

4. Pulsed Condition: Pulse Width = 300 ms, Duty Cycle  $\leq 2\%$ .



(1) SOT-963; 100 mm<sup>2</sup>, 1 oz. Copper Trace

**Figure 1. Derating Curve**

## NSBA123TDP6

### TYPICAL CHARACTERISTICS NSBA123TDP6

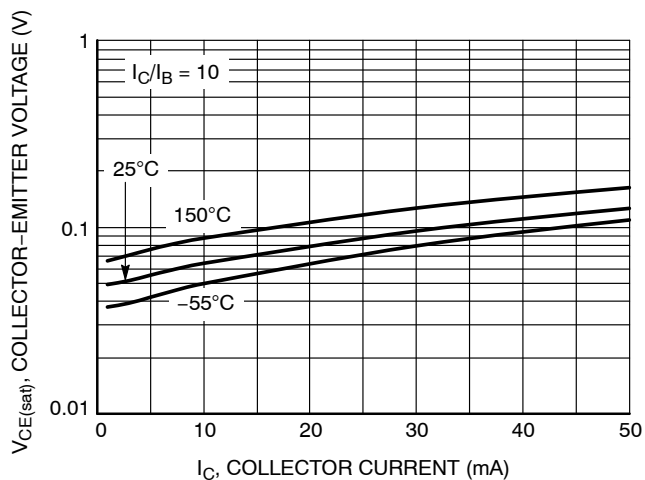


Figure 2.  $V_{CE(sat)}$  vs.  $I_C$

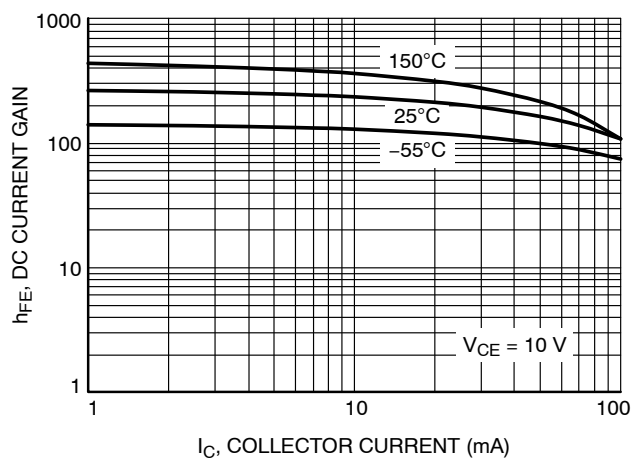


Figure 3. DC Current Gain

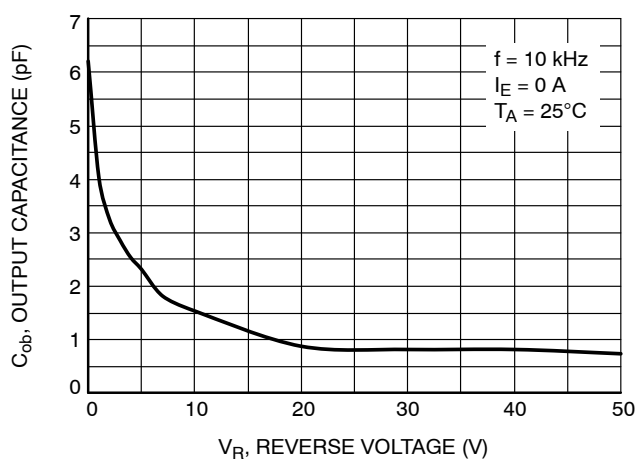


Figure 4. Output Capacitance

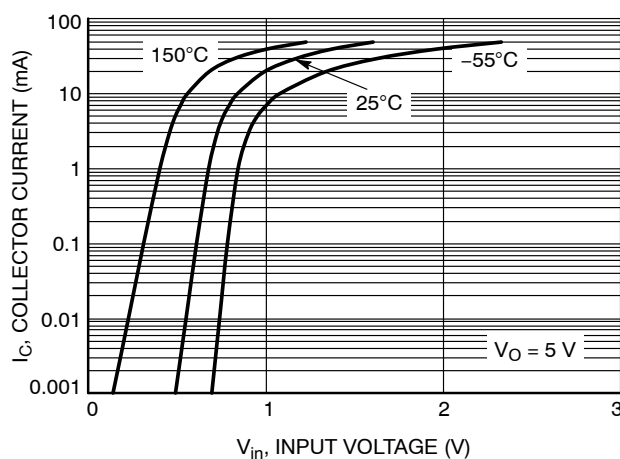


Figure 5. Output Current vs. Input Voltage

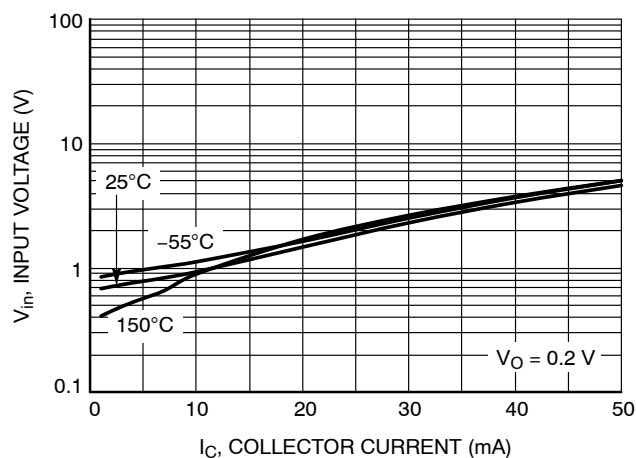
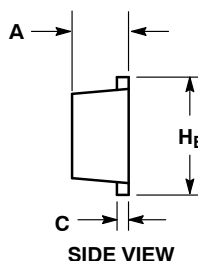
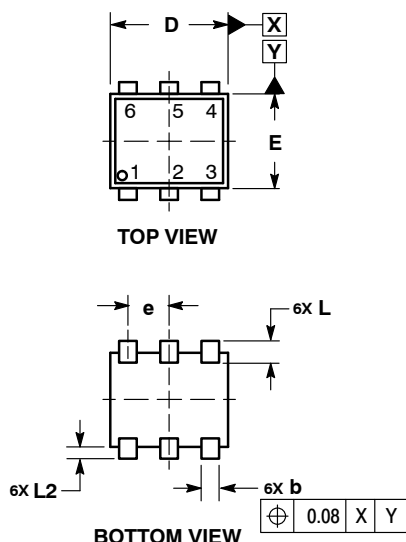


Figure 6. Input Voltage vs. Output Current

## NSBA123TDP6

### PACKAGE DIMENSIONS

#### SOT-963 CASE 527AD ISSUE E

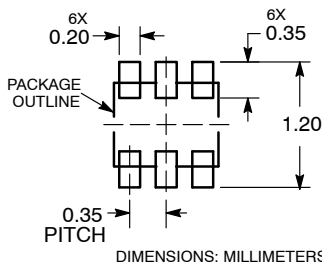


#### NOTES:


1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.34	0.37	0.40
b	0.10	0.15	0.20
C	0.07	0.12	0.17
D	0.95	1.00	1.05
E	0.75	0.80	0.85
e	0.35 BSC		
HE	0.95	1.00	1.05
L	0.19 REF		
L2	0.05	0.10	0.15

#### RECOMMENDED MOUNTING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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