TPS256x Dual Channel Precision Adjustable Current-limited Power Switches

1 Features

- Two Separate Current Limiting Channels
- Meets USB Current-Limiting Requirements
- Adjustable Current Limit, 250 mA to 2.8 A (typ)
- ± 7.5% Current-Limit Accuracy at 2.8 A
- Fast Overcurrent Response - 3.5-μs (typ)
- Two 44-mΩ High-Side MOSFETs
- Operating Range: 2.5 V to 6.5 V
- 2-μA Maximum Standby Supply Current
- Built-in Soft-Start
- 15-kV / 8-kV System-Level ESD Capable
- UL Listed – File No. E169910
- CB and Nemko Certified

2 Applications

- USB Ports/Hubs
- Digital TV
- Set-Top Boxes
- VOIP Phones

3 Description

The TPS2560 and TPS2561 are dual-channel power-distribution switches intended for applications where precision current limiting is required or heavy capacitive loads and short circuits are encountered. These devices offer a programmable current-limit threshold between 250 mA and 2.8 A (typ) per channel through an external resistor. The power-switch rise and fall times are controlled to minimize current surges during turn on and off.

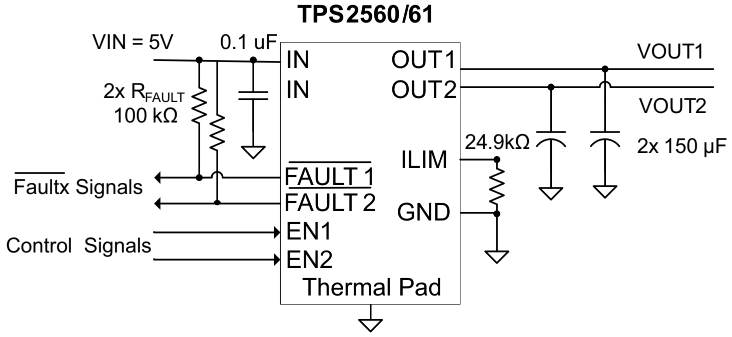
Each channel of the TPS256x devices limit the output current to a safe level by switching into a constant-current mode when the output load exceeds the current-limit threshold. The $\overline{\text{FAULTx}}$ logic output for each channel independently asserts low during overcurrent and overtemperature conditions.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS2560 TPS2561	VSON (10)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Diagram



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

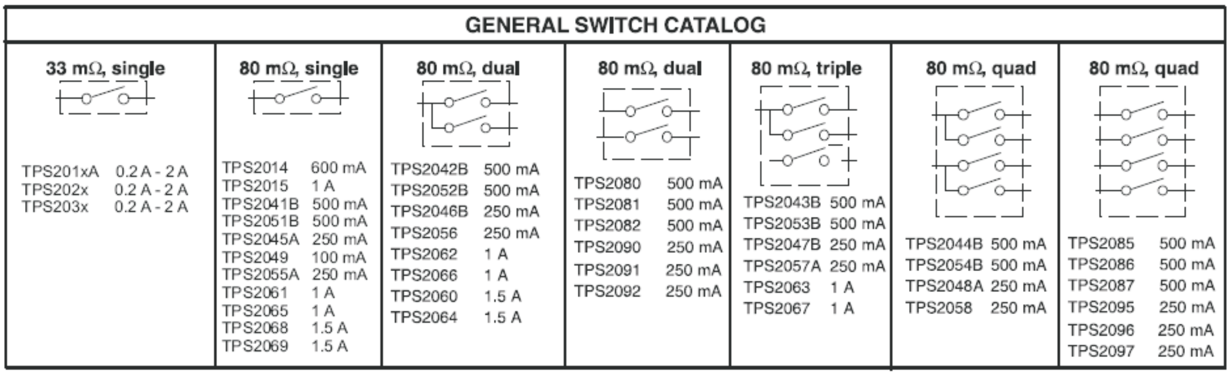
Changes from Revision A (February 2012) to Revision B — **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

Changes from Original (December 2009) to Revision A — **Page**

- Changed V_{ENx} to $V_{\overline{ENx}}$ in Recommended Operating Conditions ... 4
- Changed $V_{\overline{ENx}}$ to V_{ENx} in Recommended Operating Conditions ... 4

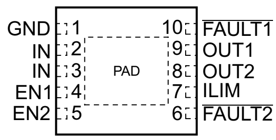
5 Device Comparison Table



GENERAL SWITCH CATALOG						
33 mΩ, single	80 mΩ, single	80 mΩ, dual	80 mΩ, dual	80 mΩ, triple	80 mΩ, quad	80 mΩ, quad
TPS201xA 0.2 A - 2 A TPS202x 0.2 A - 2 A TPS203x 0.2 A - 2 A	TPS2014 600 mA TPS2015 1 A TPS2041B 500 mA TPS2051B 500 mA TPS2045A 250 mA TPS2049 100 mA TPS2055A 250 mA TPS2061 1 A TPS2065 1 A TPS2068 1.5 A TPS2069 1.5 A	TPS2042B 500 mA TPS2052B 500 mA TPS2046B 250 mA TPS2056 250 mA TPS2062 1 A TPS2066 1 A TPS2060 1.5 A TPS2064 1.5 A	TPS2080 500 mA TPS2081 500 mA TPS2082 500 mA TPS2090 250 mA TPS2091 250 mA TPS2092 250 mA	TPS2043B 500 mA TPS2053B 500 mA TPS2047B 250 mA TPS2057A 250 mA TPS2063 1 A TPS2067 1 A	TPS2044B 500 mA TPS2054B 500 mA TPS2048A 250 mA TPS2058 250 mA	TPS2085 500 mA TPS2086 500 mA TPS2087 500 mA TPS2095 250 mA TPS2096 250 mA TPS2097 250 mA

6 Pin Configuration and Functions

DRC Package
10-Pin VSON
Top View



Pin Functions

PIN			I/O	DESCRIPTION
NAME	TPS2560	TPS2561		
$\overline{\text{EN1}}$	4	—	I	Enable input, logic low turns on channel one power switch
EN1	—	4	I	Enable input, logic high turns on channel one power switch
$\overline{\text{EN2}}$	5	—	I	Enable input, logic low turns on channel two power switch
EN2	—	5	I	Enable input, logic high turns on channel two power switch
GND	1	1	—	Ground connection; connect externally to the thermal pad
IN	2, 3	2, 3	I	Input voltage; connect a 0.1 μF or greater ceramic capacitor from IN to GND as close to the IC as possible.
$\overline{\text{FAULT1}}$	10	10	O	Active-low open-drain output, asserted during overcurrent or overtemperature condition on channel one.
$\overline{\text{FAULT2}}$	6	6	O	Active-low open-drain output, asserted during overcurrent or overtemperature condition on channel two
OUT1	9	9	O	Power-switch output for channel one
OUT2	8	8	O	Power-switch output for channel two
ILIM	7	7	O	External resistor used to set current-limit threshold; recommended 20 kΩ ≤ R_{ILIM} ≤ 187 kΩ.
Thermal pad	PAD	PAD	—	Internally connected to GND; used to heat-sink the part to the circuit board traces. Connect the thermal pad to GND pin externally.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[(1)(2)]

		MIN	MAX	UNIT
	Voltage on IN, OUTx, ENx or $\overline{\text{ENx}}$, ILIM, $\overline{\text{FAULTx}}$	–0.3	7	V
	Voltage from IN to OUTx	–7	7	V
	Continuous output current	Internally limited		–
	Continuous total power dissipation	See *Dissipation Ratings*		–
	Continuous $\overline{\text{FAULTx}}$ sink current		25	mA
	ILIM source current	Internally limited		–
T_J	Maximum junction temperature	–40	OTSD2[(3)]	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Voltages are referenced to GND unless otherwise noted.
(3) Ambient over temperature shutdown threshold

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[(1)]	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[(2)]	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 ESD Ratings: Surge

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	IEC 61000-4-2 contact discharge[(1)]	±8000	V
		IEC 61000-4-2 air-gap discharge[(1)]	±15000	

(1) Surges per EN61000-4-2. 1999 applied to output terminals of EVM. These are passing test levels, not failure threshold.

7.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	2.5		6.5	V
$V_{\overline{ENx}}$	TPS2560 enable voltage	0		6.5	V
V_{ENx}	TPS2561 enable voltage	0		6.5	V
V_{IH}	High-level input voltage on ENx or $\overline{\text{ENx}}$	1.1			V
V_{IL}	Low-level input voltage on ENx or $\overline{\text{ENx}}$			0.66	V
I_{OUTx}	Continuous output current per channel	0		2.5	A
	Continuous $\overline{\text{FAULTx}}$ sink current	0		10	mA
R_{ILIM}	Recommended resistor limit	20		187	kΩ
T_J	Operating junction temperature	–40		125	°C

7.5 Thermal Information

THERMAL METRIC(1)		TPS256x DRC (VSON) 10 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	47.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	66.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	22.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	22.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	4.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.6 Electrical Characteristics

over recommended operating conditions, $V_{/ENx}$ = 0 V, or V_{ENx} = V_{IN} (unless otherwise noted)

PARAMETER		TEST CONDITIONS(1)		MIN	TYP	MAX	UNIT
POWER SWITCH							
$r_{DS(on)}$	Static drain-source on-state resistance per channel, IN to OUTx	T_J = 25 °C			44	50	mΩ
		–40 °C ≤ T_J ≤ 125 °C				70	
t_r	Rise time, output	C_{Lx} = 1 µF, R_{Lx} = 100 Ω (see Figure 12)	V_{IN} = 6.5 V	2	3	4	ms
			V_{IN} = 2.5 V	1	2	3	
t_f	Fall time, output	C_{Lx} = 1 µF, R_{Lx} = 100 Ω (see Figure 12)	V_{IN} = 6.5 V	0.6	0.8	1.0	ms
			V_{IN} = 2.5 V	0.4	0.6	0.8	
ENABLE INPUT, EN OR $\overline{EN}$							
	Enable pin turn on/off threshold			0.66		1.1	V
	Hysteresis				55(2)		mV
I_{EN}	Input current	V_{ENx} = 0 V or 6.5 V, $V_{/ENx}$ = 0 V or 6.5 V		–0.5		0.5	µA
t_{on}	Turnon time	C_{Lx} = 1 µF, R_{Lx} = 100 Ω, (see Figure 12)				9	ms
t_{off}	Turnoff time					6	ms
CURRENT LIMIT							
I_{OS}	Current-limit threshold per channel (Maximum DC output current I_{OUTx} delivered to load) and Short-circuit current, OUTx connected to GND	R_{ILIM} = 20 kΩ		2590	2800	3005	mA
		R_{ILIM} = 61.9 kΩ		800	900	1005	
		R_{ILIM} = 100 kΩ		470	560	645	
t_{IOS}	Response time to short circuit	V_{IN} = 5.0 V, (see Figure 13)			3.5(2)		µs

(1) Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.
(2) These parameters are provided for reference only, and do not constitute part of TI's published specifications for purposes of TI's product warranty.

Electrical Characteristics (continued)

over recommended operating conditions, $V_{/ENx}$ = 0 V, or V_{ENx} = V_{IN} (unless otherwise noted)

PARAMETER		TEST CONDITIONS(1)		MIN	TYP	MAX	UNIT
SUPPLY CURRENT							
I_{IN_off}	Supply current, low-level output	V_{IN} = 6.5 V, no load on OUTx, $V_{\overline{ENx}}$ = 6.5 V or V_{ENx} = 0 V			0.1	2.0	μA
I_{IN_on}	Supply current, high-level output	V_{IN} = 6.5 V, no load on OUT	R_{ILIM} = 20 kΩ		100	125	μA
			R_{ILIM} = 100 kΩ		85	110	μA
I_{REV}	Reverse leakage current	V_{OUTx} = 6.5 V, V_{IN} = 0 V	T_J = 25°C		0.01	1.0	μA
UNDERVOLTAGE LOCKOUT							
UVLO	Low-level input voltage, IN	V_{IN} rising			2.35	2.45	V
	Hysteresis, IN	T_J = 25°C			35		mV
$\overline{\text{FAULTx}}$ FLAG							
V_{OL}	Output low voltage, $\overline{\text{FAULTx}}$	$I_{\overline{FAULTx}}$ = 1 mA				180	mV
	Off-state leakage	$V_{\overline{FAULTx}}$ = 6.5 V				1	μA
	$\overline{\text{FAULTx}}$ deglitch	$\overline{\text{FAULTx}}$ assertion or de-assertion due to overcurrent condition		6	9	13	ms
THERMAL SHUTDOWN							
OTSD2	Thermal shutdown threshold			155			°C
OTSD	Thermal shutdown threshold in current-limit			135			°C
	Hysteresis				20(2)		°C

7.7 Dissipation Ratings

BOARD	PACKAGE	THERMAL RESISTANCE(1) $R_{θJA}$	THERMAL RESISTANCE $R_{θJC}$	T_A ≤ 25°C POWER RATING
High-K(2)	DRC	41.6 °C/W	10.7 °C/W	2403 mW

(1) Mounting per the *PowerPAD™ Thermally Enhanced Package* application report (SLMA002)
(2) The JEDEC high-K (2s2p) board used to derive this data was a 3in × 3in, multilayer board with 1-ounce internal power and ground planes and 2-ounce copper traces on top and bottom of the board.

7.8 Typical Characteristics

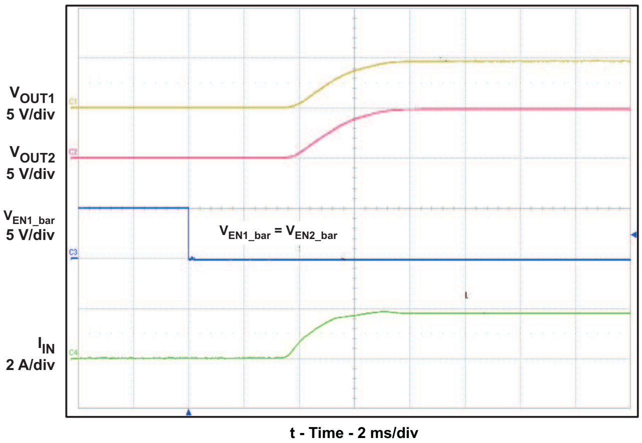


Figure 1. Turn-on Delay and Rise Time

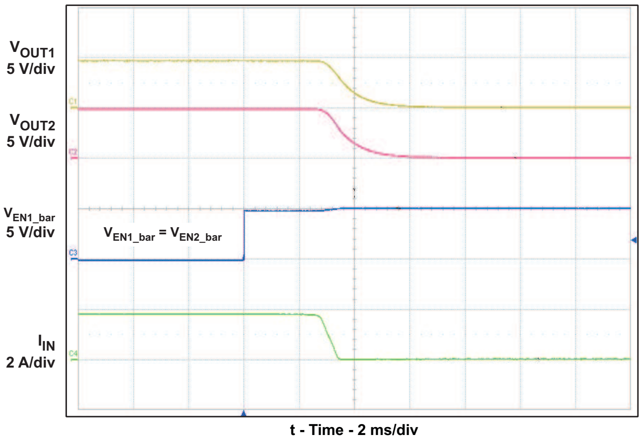


Figure 2. Turn-off Delay and Fall Time

Typical Characteristics (continued)

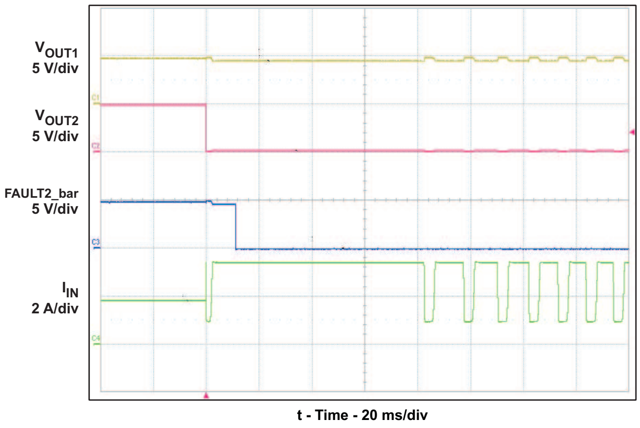


Figure 3. Full-Load to Short-Circuit Transient Response

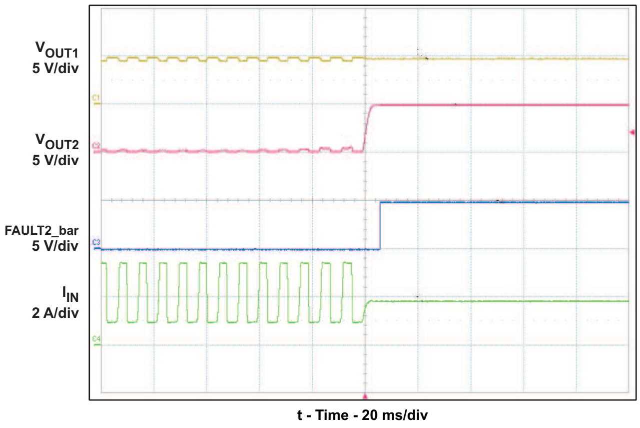


Figure 4. Short-Circuit to Full-Load Recovery Response

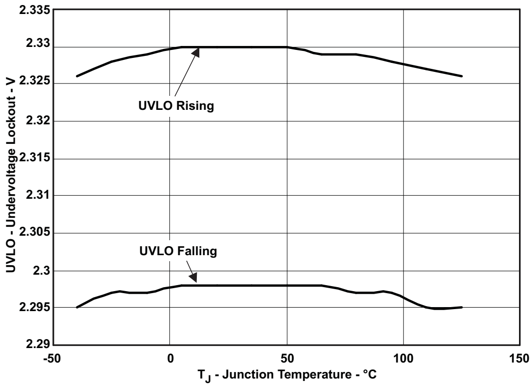


Figure 5. UVLO – Undervoltage Lockout – V

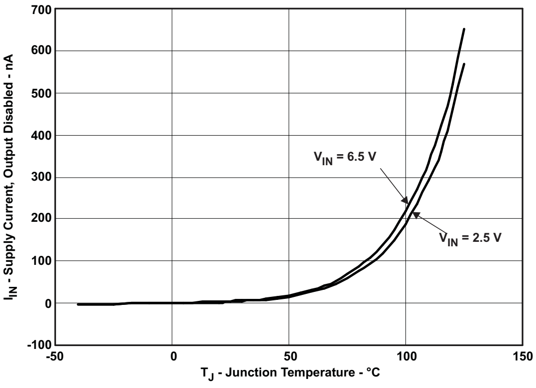


Figure 6. I_{IN} – Supply Current, Output Disabled – nA

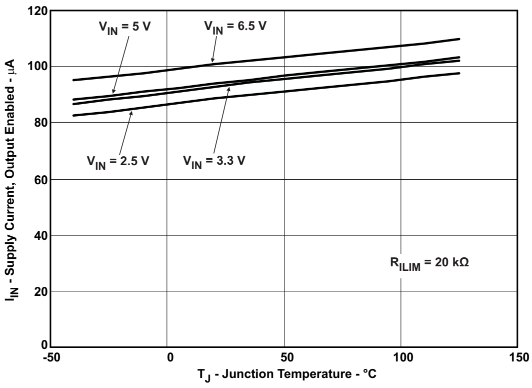


Figure 7. I_{IN} – Supply Current, Output Enabled – µA

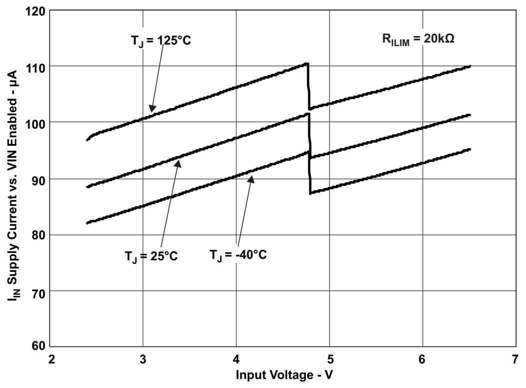


Figure 8. I_{IN} – Supply Current, Output Enabled – µA

Typical Characteristics (continued)

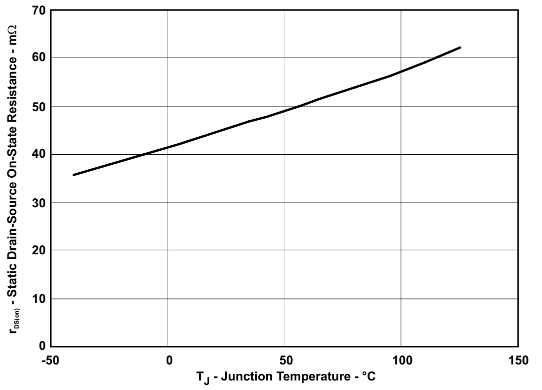


Figure 9. MOSFET $r_{DS(on)}$ vs Junction Temperature

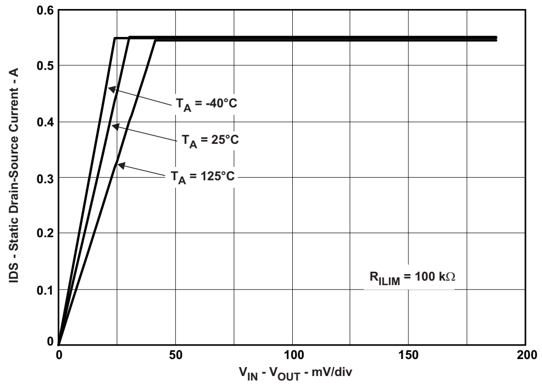


Figure 10. Switch Current vs Drain-Source Voltage Across Switch

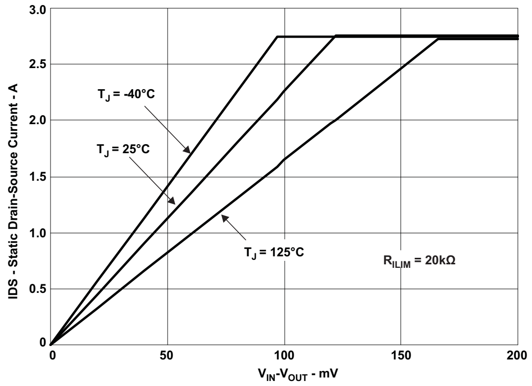


Figure 11. Switch Current vs Drain-Source Voltage Across Switch

8 Parameter Measurement Information

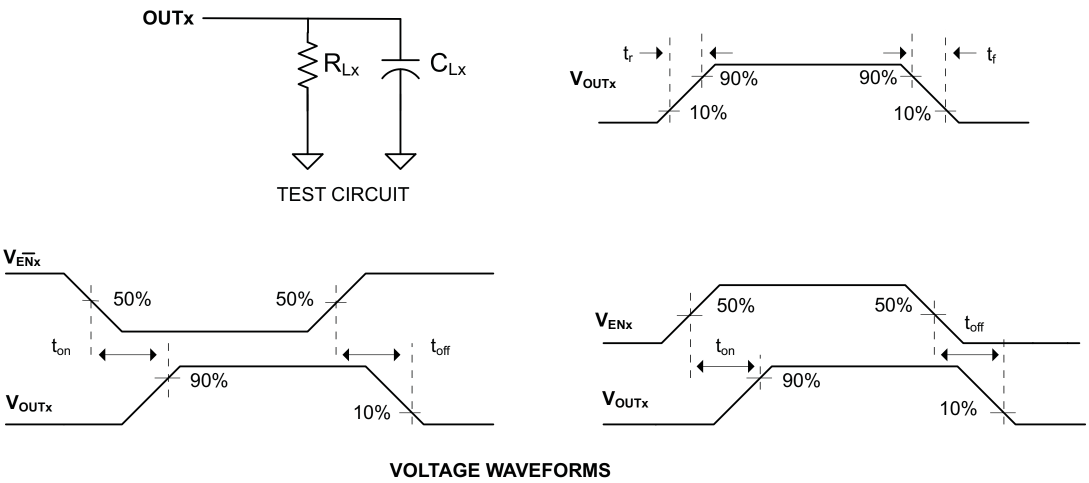


Figure 12. Test Circuit and Voltage Waveforms

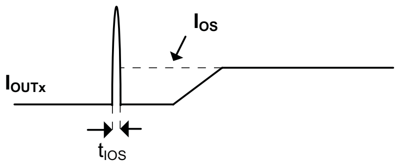


Figure 13. Response Time to Short Circuit Waveform

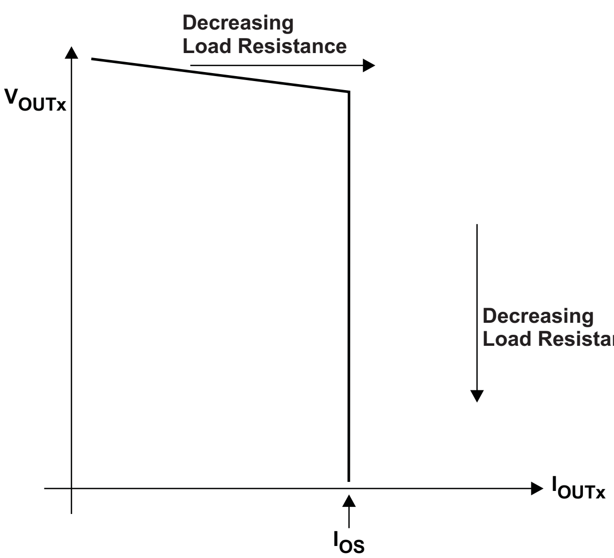


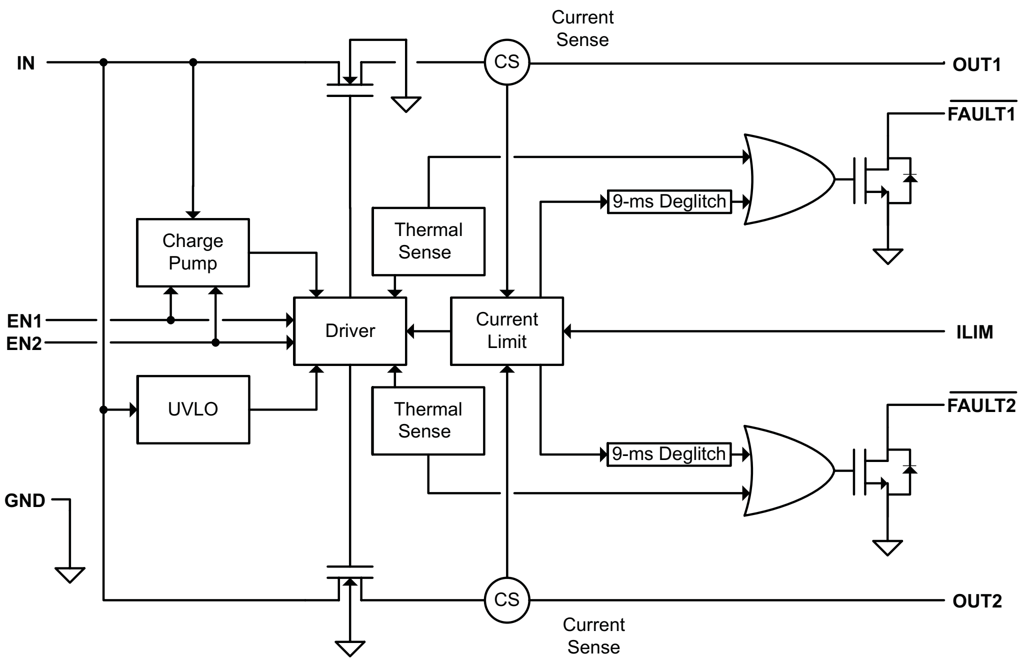
Figure 14. Output Voltage vs Current-Limit Threshold

9 Detailed Description

9.1 Overview

The TPS256x is a dual-channel, current-limited power-distribution switch using N-channel MOSFETs for applications where short circuits or heavy capacitive loads will be encountered. This device allows the user to program the current-limit threshold between 250 mA and 2.8 A (typ) per channel via an external resistor. This device incorporates an internal charge pump and gate drive circuitry necessary to drive the N-channel MOSFETs. The charge pump supplies power to the driver circuit for each channel and provides the necessary voltage to pull the gate of the MOSFET above the source. The charge pump operates from input voltages as low as 2.5 V and requires little supply current. The driver controls the gate voltage of the power switch. The driver incorporates circuitry that controls the rise and fall times of the output voltage to limit large current and voltage surges and provides built-in soft-start functionality. Each channel of the TPS256x limits the output current to the programmed current-limit threshold I_{OS} during an overcurrent or short-circuit event by reducing the charge pump voltage driving the N-channel MOSFET and operating it in the linear range of operation. The result of limiting the output current to I_{OS} reduces the output voltage at OUTx because the N-channel MOSFET is no longer fully enhanced.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Overcurrent Conditions

The TPS256x responds to overcurrent conditions by limiting the output current per channel to I_{OS}. When an overcurrent condition is detected, the device maintains a constant output current and reduces the output voltage accordingly. Two possible overload conditions can occur.

The first condition is when a short circuit or partial short circuit is present when the device is powered-up or enabled. The output voltage is held near zero potential with respect to ground and the TPS256x ramps the output current to I_{OS}. The TPS256x devices will limit the current to I_{OS} until the overload condition is removed or the device begins to thermal cycle.

Feature Description (continued)

The second condition is when a short circuit, partial short circuit, or transient overload occurs while the device is enabled and powered on. The device responds to the overcurrent condition within time t_{IOS} (see Figure 13). The current-sense amplifier is overdriven during this time and momentarily disables the internal current-limit MOSFET. The current-sense amplifier recovers and ramps the output current to I_{OS}. Similar to the previous case, the TPS256x will limit the current to I_{OS} until the overload condition is removed or the device begins to thermal cycle.

The TPS256x thermal cycles if an overload condition is present long enough to activate thermal limiting in any of the above cases. The device turns off when the junction temperature exceeds 135°C (min) while in current limit. The device remains off until the junction temperature cools 20°C (typ) and then restarts. The TPS256x cycles on/off until the overload is removed (see Figure 4).

9.3.2 $\overline{\text{FAULTx}}$ Response

The $\overline{\text{FAULTx}}$ open-drain outputs are asserted (active low) on an individual channel during an overcurrent or overtemperature condition. The TPS256x asserts the $\overline{\text{FAULTx}}$ signal until the fault condition is removed and the device resumes normal operation on that channel. The TPS256x is designed to eliminate false $\overline{\text{FAULTx}}$ reporting by using an internal delay "deglitch" circuit (9-ms typ) for overcurrent conditions without the need for external circuitry. This ensures that $\overline{\text{FAULTx}}$ is not accidentally asserted due to normal operation such as starting into a heavy capacitive load. The deglitch circuitry delays entering and leaving current-limited induced fault conditions. The $\overline{\text{FAULTx}}$ signal is not deglitched when the MOSFET is disabled due to an overtemperature condition but is deglitched after the device has cooled and begins to turn on. This unidirectional deglitch prevents $\overline{\text{FAULTx}}$ oscillation during an overtemperature event.

9.3.3 Undervoltage Lockout (UVLO)

The undervoltage lockout (UVLO) circuit disables the power switch until the input voltage reaches the UVLO turn-on threshold. Built-in hysteresis prevents unwanted on/off cycling due to input voltage droop during turn on.

9.3.4 Enable ($\overline{\text{ENx}}$ or ENx)

The logic enables control the power switches and device supply current. The supply current is reduced to less than 2-µA when a logic high is present on $\overline{\text{ENx}}$ or when a logic low is present on ENx. A logic low input on $\overline{\text{ENx}}$ or a logic high input on ENx enables the driver, control circuits, and power switches. The enable inputs are compatible with both TTL and CMOS logic levels.

9.3.5 Thermal Sense

The TPS256x self protects by using two independent thermal sensing circuits that monitor the operating temperature of the power switch and disable operation if the temperature exceeds recommended operating conditions. Each channel of the TPS256x operates in constant-current mode during an overcurrent conditions, which increases the voltage drop across the power switch. The power dissipation in the package is proportional to the voltage drop across the power switch, which increases the junction temperature during an overcurrent condition. The first thermal sensor (OTSD) turns off the individual power switch channel when the die temperature exceeds 135°C (min) and the channel is in current limit. Hysteresis is built into the thermal sensor, and the switch turns on after the device has cooled approximately 20°C.

The TPS256x also has a second ambient thermal sensor (OTSD2). The ambient thermal sensor turns off both power switch channels when the die temperature exceeds 155°C (min) regardless of whether the power switch channels are in current limit and will turn on the power switches after the device has cooled approximately 20°C. The TPS256x continues to cycle off and on until the fault is removed.

9.4 Device Functional Modes

There are no other functional modes.

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

10.1.1 Auto-Retry Functionality

Some applications require that an overcurrent condition disables the part momentarily during a fault condition and re-enables after a pre-set time. This auto-retry functionality can be implemented with an external resistor and capacitor. During a fault condition, FAULTx pulls ENx low disabling the part. The part is disabled when ENx is pulled below the turn-off threshold, and FAULTx goes high impedance allowing C_{RETRY} to begin charging. The part re-enables when the voltage on ENx reaches the turn-on threshold, and the auto-retry time is determined by the resistor/capacitor time constant. The part will continue to cycle in this manner until the fault condition is removed.

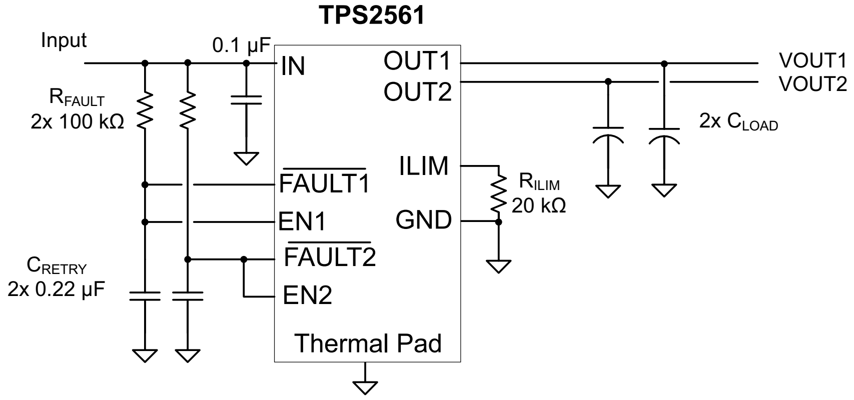


Figure 15. Auto-Retry Functionality

Some applications require auto-retry functionality and the ability to enable/disable with an external logic signal. The figure below shows how an external logic signal can drive EN through R_{FAULT} and maintain auto-retry functionality. The resistor/capacitor time constant determines the auto-retry time-out period.

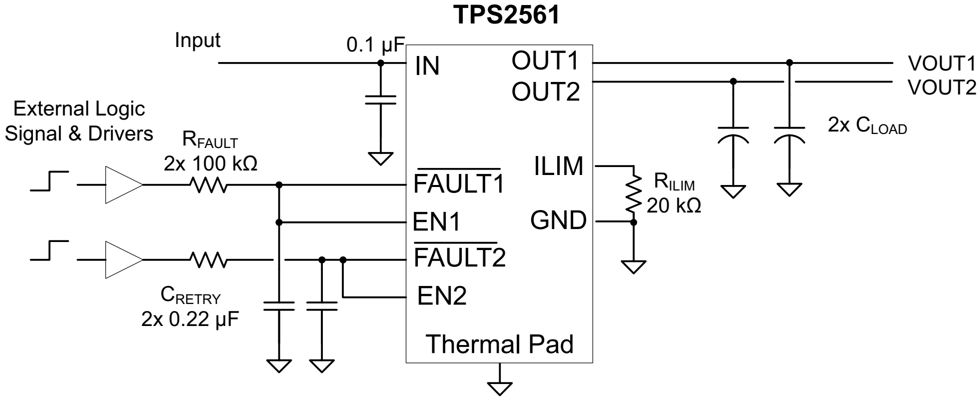


Figure 16. Auto-Retry Functionality With External EN Signal

Application Information (continued)

10.1.2 Two-Level Current-Limit Circuit

Some applications require different current-limit thresholds depending on external system conditions. Figure 17 shows an implementation for an externally controlled, two-level current-limit circuit. The current-limit threshold is set by the total resistance from ILIM to GND (see previously discussed *Programming the Current-Limit Threshold* section). A logic-level input enables/disables MOSFET Q1 and changes the current-limit threshold by modifying the total resistance from ILIM to GND. Additional MOSFET/resistor combinations can be used in parallel to Q1/R2 to increase the number of additional current-limit levels.

NOTE
ILIM should never be driven directly with an external signal.

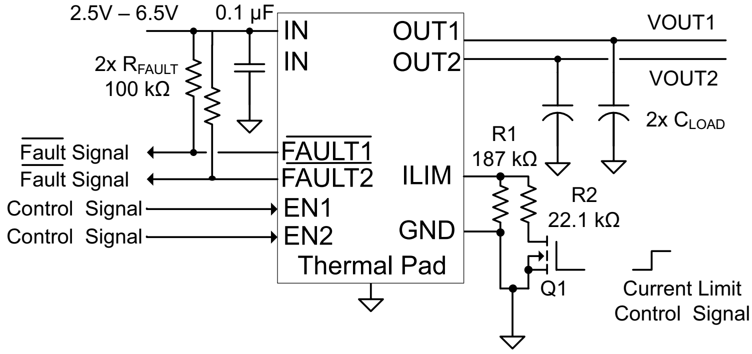


Figure 17. Two-Level Current-Limit Circuit

10.2 Typical Application

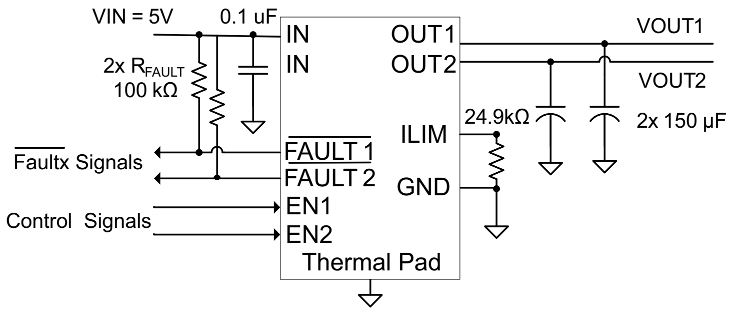


Figure 18. Typical Application Circuit

10.2.1 Design Requirements

See the design parameters in Table 1.

Table 1. Design Parameters

PARAMETER	VALUE
Input voltage	5 V
Output voltage	5 V
Above a minimum current limit	2000 mA
Below a minimum current limit	1000 mA

10.2.2 Detailed Design Procedure

10.2.2.1 Input and Output Capacitance

Input and output capacitance improves the performance of the device; the actual capacitance should be optimized for the particular application. For all applications, a 0.1µF or greater ceramic bypass capacitor between IN and GND is recommended as close to the device as possible for local noise decoupling. This precaution reduces ringing on the input due to power-supply transients. Additional input capacitance may be needed on the input to reduce voltage overshoot from exceeding the absolute maximum voltage of the device during heavy transient conditions. This is especially important during bench testing when long, inductive cables are used to connect the evaluation board to the bench power supply.

Output capacitance is not required, but placing a high-value electrolytic capacitor on the output pin is recommended when large transient currents are expected on the output.

10.2.2.2 Programming the Current-Limit Threshold

The overcurrent threshold is user programmable via an external resistor, R_{ILIM}. R_{ILIM} sets the current-limit threshold for both channels. The TPS256x use an internal regulation loop to provide a regulated voltage on the ILIM pin. The current-limit threshold is proportional to the current sourced out of ILIM. The recommended 1% resistor range for R_{ILIM} is 20 kΩ ≤ R_{ILIM} ≤ 187 kΩ to ensure stability of the internal regulation loop. Many applications require that the minimum current limit is above a certain current level or that the maximum current limit is below a certain current level, so it is important to consider the tolerance of the overcurrent threshold when selecting a value for R_{ILIM}. The following equations calculates the resulting overcurrent threshold for a given external resistor value (R_{ILIM}). The traces routing the R_{ILIM} resistor to the TPS256x should be as short as possible to reduce parasitic effects on the current-limit accuracy.

$$I_{OSmax}(mA) = \frac{52850V}{R_{ILIM}{}^{0.957}k\Omega}$$
$$I_{OSnom}(mA) = \frac{56000V}{R_{ILIM}k\Omega}$$
$$I_{OSmin}(mA) = \frac{61200V}{R_{ILIM}{}^{1.056}k\Omega} \quad (1)$$

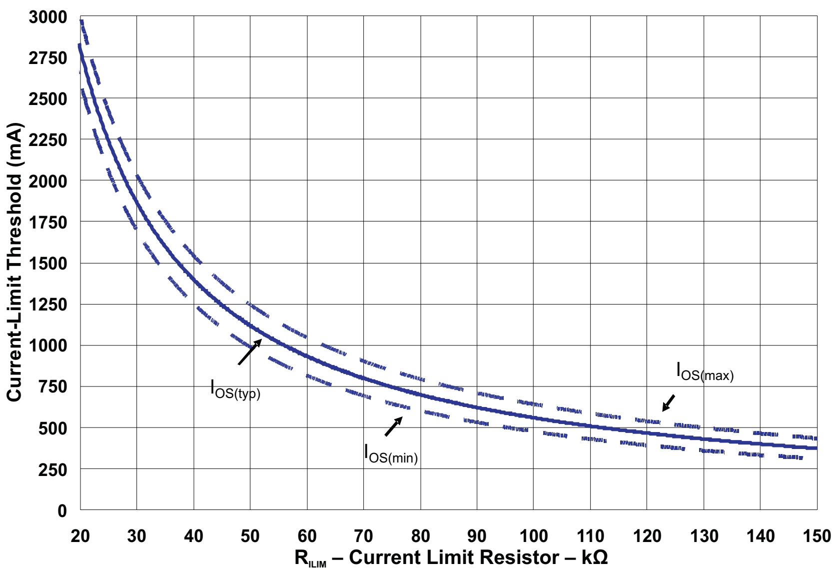


Figure 19. Current-Limit Threshold vs R_{ILIM}

10.2.2.3 Application 1: Designing Above a Minimum Current Limit

Some applications require that current limiting cannot occur below a certain threshold. For this example, assume that 2 A must be delivered to the load so that the minimum desired current-limit threshold is 2000 mA. Use the I_{OS} equations and Figure 19 to select R_{ILIM}.

$$I_{OSmin}(mA) = 2000mA$$
$$I_{OSmin}(mA) = \frac{61200V}{R_{ILIM}{}^{1.056}k\Omega}$$
$$R_{ILIM}(k\Omega) = \left(\frac{61200V}{I_{OSmin}mA}\right)^{\frac{1}{1.056}}$$
$$R_{ILIM}(k\Omega) = 25.52k\Omega \tag{2}$$

Select the closest 1% resistor less than the calculated value: R_{ILIM} = 25.5 kΩ. This sets the minimum current-limit threshold at 2 A . Use the I_{OS} equations, Figure 19, and the previously calculated value for R_{ILIM} to calculate the maximum resulting current-limit threshold.

$$R_{ILIM}(k\Omega) = 25.5k\Omega$$
$$I_{OSmax}(mA) = \frac{52850V}{R_{ILIM}{}^{0.957}k\Omega}$$
$$I_{OSmax}(mA) = \frac{52850V}{25.5^{0.957}k\Omega}$$
$$I_{OSmax}(mA) = 2382mA \tag{3}$$

The resulting maximum current-limit threshold is 2382 mA with a 25.5 kΩ resistor.

10.2.2.4 Application 2: Designing Below a Maximum Current Limit

Some applications require that current limiting must occur below a certain threshold. For this example, assume that the desired upper current-limit threshold must be below 1000 mA to protect an up-stream power supply. Use the I_{OS} equations and Figure 19 to select R_{ILIM}.

$$I_{OSmax}(mA) = 1000mA$$
$$I_{OSmax}(mA) = \frac{52850V}{R_{ILIM}{}^{0.957}k\Omega}$$
$$R_{ILIM}(k\Omega) = \left(\frac{52850V}{I_{OSmax}mA}\right)^{\frac{1}{0.957}}$$
$$R_{ILIM}(k\Omega) = 63.16k\Omega \tag{4}$$

Select the closest 1% resistor greater than the calculated value: R_{ILIM} = 63.4 kΩ. This sets the maximum current-limit threshold at 1000 mA . Use the I_{OS} equations, Figure 19, and the previously calculated value for R_{ILIM} to calculate the minimum resulting current-limit threshold.

$$R_{ILIM}(k\Omega) = 63.4k\Omega$$
$$I_{OSmin}(mA) = \frac{61200V}{R_{ILIM}{}^{1.056}k\Omega}$$
$$I_{OSmin}(mA) = \frac{61200V}{63.4^{1.056}k\Omega}$$
$$I_{OSmin}(mA) = 765mA \tag{5}$$

The resulting minimum current-limit threshold is 765 mA with a 63.4 kΩ resistor.

10.2.2.5 Accounting for Resistor Tolerance

The previous sections described the selection of R_{ILIM} given certain application requirements and the importance of understanding the current-limit threshold tolerance. The analysis focused only on the TPS256x performance and assumed an exact resistor value. However, resistors sold in quantity are not exact and are bounded by an upper and lower tolerance centered around a nominal resistance. The additional R_{ILIM} resistance tolerance directly affects the current-limit threshold accuracy at a system level. The following table shows a process that accounts for worst-case resistor tolerance assuming 1% resistor values. Step one follows the selection process outlined in the application examples above. Step two determines the upper and lower resistance bounds of the selected resistor. Step three uses the upper and lower resistor bounds in the I_{OS} equations to calculate the threshold limits. It is important to use tighter tolerance resistors, e.g. 0.5% or 0.1%, when precision current limiting is desired.

Table 2. Common R_{ILIM} Resistor Selections

DESIRED NOMINAL CURRENT LIMIT	IDEAL RESISTOR	CLOSEST 1% RESISTOR	1% LOW RESISTOR TOLERANCE	1% HIGH RESISTOR TOLERANCE	IOS ACTUAL LIMITS			
					MIN	NOM	MAX	UNIT
300 mA	186.7 kΩ	187 kΩ	185.1 kΩ	188.9 kΩ	241.6	299.5	357.3	mA
400 mA	140.0 kΩ	140 kΩ	138.6 kΩ	141.4 kΩ	328.0	400.0	471.4	mA
600 mA	93.3 kΩ	93.1 kΩ	92.2 kΩ	94.0 kΩ	504.6	601.5	696.5	mA
800 mA	70.0 kΩ	69.8 kΩ	69.1 kΩ	70.5 kΩ	684.0	802.3	917.6	mA
1000 mA	56.0 kΩ	56.2 kΩ	55.6 kΩ	56.8 kΩ	859.9	996.4	1129.1	mA
1200 mA	46.7 kΩ	46.4 kΩ	45.9 kΩ	46.9 kΩ	1052.8	1206.9	1356.3	mA
1400 mA	40.0 kΩ	40.2 kΩ	39.8 kΩ	40.6 kΩ	1225.0	1393.0	1555.9	mA
1600 mA	35.0 kΩ	34.8 kΩ	34.5 kΩ	35.1 kΩ	1426.5	1609.2	1786.2	mA
1800 mA	31.1 kΩ	30.9 kΩ	30.6 kΩ	31.2 kΩ	1617.3	1812.3	2001.4	mA
2000 mA	28.0 kΩ	28 kΩ	27.7 kΩ	28.3 kΩ	1794.7	2000.0	2199.3	mA
2200 mA	25.5 kΩ	25.5 kΩ	25.2 kΩ	25.8 kΩ	1981.0	2196.1	2405.3	mA
2400 mA	23.3 kΩ	23.2 kΩ	23.0 kΩ	23.4 kΩ	2188.9	2413.8	2633.0	mA
2600 mA	21.5 kΩ	21.5 kΩ	21.3 kΩ	21.7 kΩ	2372.1	2604.7	2831.9	mA
2800 mA	20.0 kΩ	20 kΩ	19.8 kΩ	20.2 kΩ	2560.4	2800.0	3034.8	mA

10.2.3 Application Curves

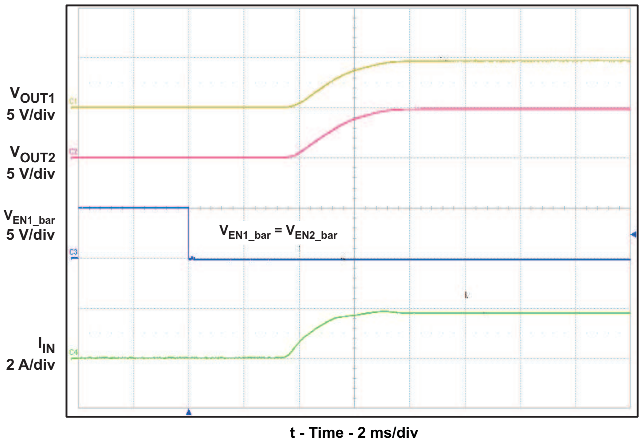


Figure 20. Turn-on Delay and Rise Time

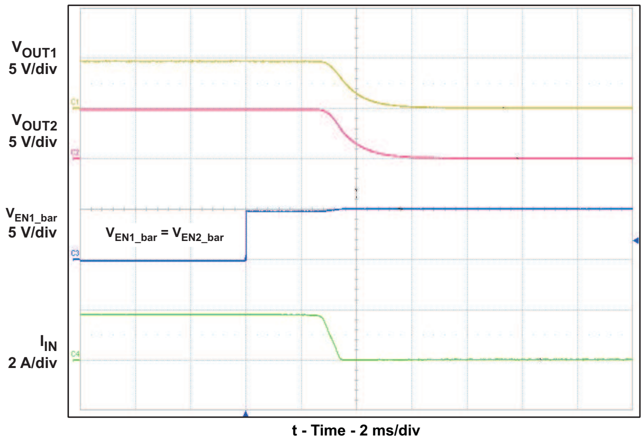


Figure 21. Turn-off Delay and Fall Time

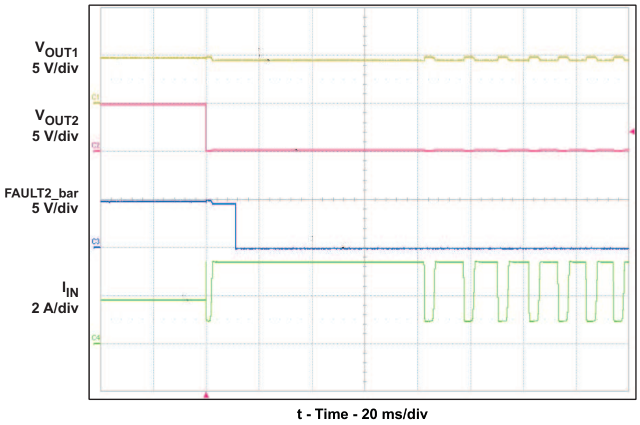


Figure 22. Full-Load to Short-Circuit Transient Response

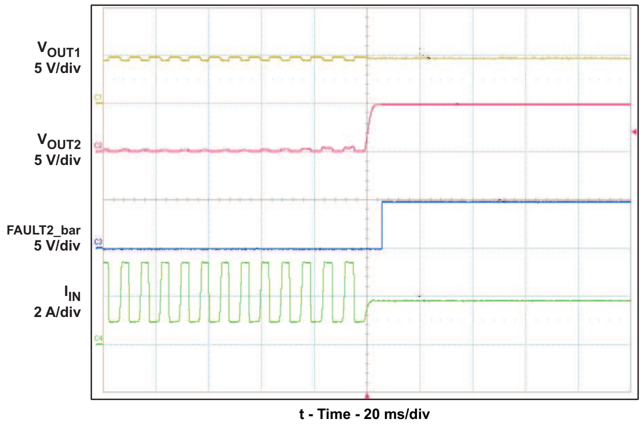


Figure 23. Short-Circuit to Full-Load Recovery Response

11 Power Supply Recommendations

11.1 Self-Powered and Bus-Powered Hubs

A SPH has a local power supply that powers embedded functions and downstream ports. This power supply must provide between 4.75 V to 5.25 V to downstream facing devices under full-load and no-load conditions. SPHs are required to have current-limit protection and must report overcurrent conditions to the USB controller. Typical SPHs are desktop PCs, monitors, printers, and stand-alone hubs. A BPH obtains all power from an upstream port and often contains an embedded function. It must power up with less than 100 mA. The BPH usually has one embedded function, and power is always available to the controller of the hub. If the embedded function and hub require more than 100 mA on power up, the power to the embedded function may need to be kept off until enumeration is completed. This is accomplished by removing power or by shutting off the clock to the embedded function. Power switching the embedded function is not necessary if the aggregate power draw for the function and controller is less than 100 mA. The total current drawn by the bus-powered device is the sum of the current to the controller, the embedded function, and the downstream ports, and it is limited to 500 mA from an upstream port.

11.2 Low-Power Bus-Powered and High-Power Bus-Powered Functions

Both low-power and high-power bus-powered functions obtain all power from upstream ports. Low-power functions always draw less than 100 mA; high-power functions must draw less than 100 mA at power up and can draw up to 500 mA after enumeration. If the load of the function is more than the parallel combination of 44 Ω and 10 µF at power up, the device must implement inrush current limiting.

12 Layout

12.1 Layout Guidelines

- Place the 100-nF bypass capacitor near the IN and GND pins, and make the connections using a low-inductance trace
- Place a high-value electrolytic capacitor and a 100-nF bypass capacitor on the output pin is recommended when large transient currents are expected on the output
- The traces routing the RILIM resistor to the device should be as short as possible to reduce parasitic effects on the current limit accuracy
- The thermal pad should be directly connected to PCB ground plane using wide and short copper trace

12.2 Layout Example

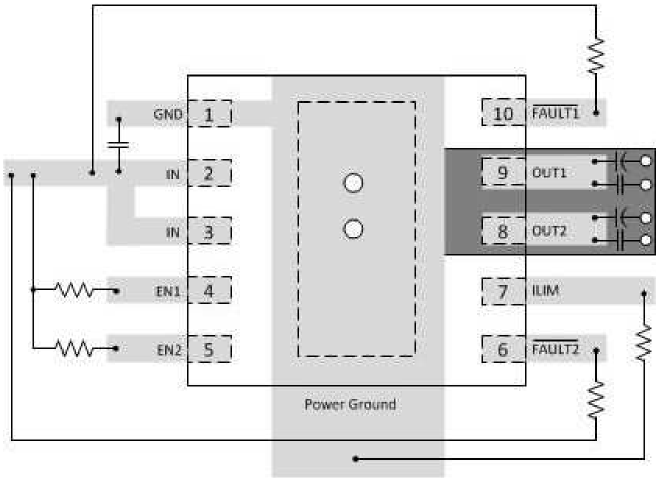


Figure 24. Layout Recommendation

12.3 Power Dissipation

The low on-resistance of the N-channel MOSFET allows small surface-mount packages to pass large currents. It is good design practice to estimate power dissipation and junction temperature. The below analysis gives an approximation for calculating junction temperature based on the power dissipation in the package. However, it is important to note that thermal analysis is strongly dependent on additional system level factors. Such factors include air flow, board layout, copper thickness and surface area, and proximity to other devices dissipating power. Good thermal design practice must include all system level factors in addition to individual component analysis.

Begin by determining the $r_{DS(on)}$ of the N-channel MOSFET relative to the input voltage and operating temperature. As an initial estimate, use the highest operating ambient temperature of interest and read $r_{DS(on)}$ from the typical characteristics graph. Using this value, the power dissipation can be calculated with Equation 6. This step calculates the total power dissipation of the N-channel MOSFET.

$$P_D = (R_{DS(on)} \times I_{OUT1}^2) + (R_{DS(on)} \times I_{OUT2}^2)$$

where

- P_D = Total power dissipation (W)
- $r_{DS(on)}$ = Power switch on-resistance of one channel (Ω)
- I_{OUTx} = Maximum current-limit threshold set by R_{ILIM}(A) (6)

Power Dissipation (continued)

Finally, calculate the junction temperature with Equation 7.

$$T_J = P_D \times R_{\theta JA} + T_A \tag{7}$$

where

- T_A = Ambient temperature (°C)
- $R_{\theta JA}$ = Thermal resistance (°C/W)
- P_D = Total power dissipation (W)

Compare the calculated junction temperature with the initial estimate. If they are not within a few degrees, repeat the calculation using the "refined" $r_{DS(on)}$ from the previous calculation as the new estimate. Two or three iterations are generally sufficient to achieve the desired result. The final junction temperature is highly dependent on thermal resistance $R_{\theta JA}$, and thermal resistance is highly dependent on the individual package and board layout. The *Dissipation Ratings* table provides example thermal resistances for specific packages and board layouts.

13 Device and Documentation Support

13.1 Documentation Support

13.1.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 3. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS2560	Click here	Click here	Click here	Click here	Click here
TPS2561	Click here	Click here	Click here	Click here	Click here

13.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

13.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS2560DRCR	ACTIVE	VSON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	2560	Samples
TPS2560DRCT	ACTIVE	VSON	DRC	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	2560	Samples
TPS2561DRCR	ACTIVE	VSON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	2561	Samples
TPS2561DRCT	ACTIVE	VSON	DRC	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	2561	Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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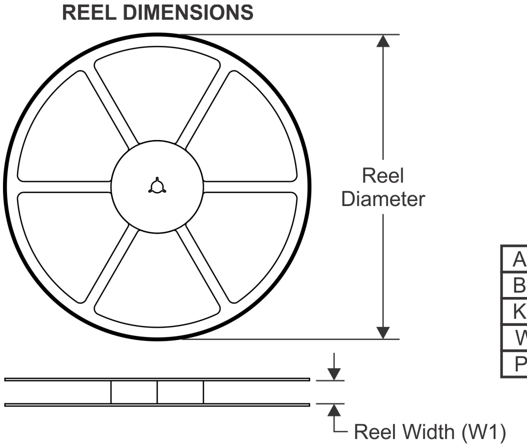
OTHER QUALIFIED VERSIONS OF TPS2561 :

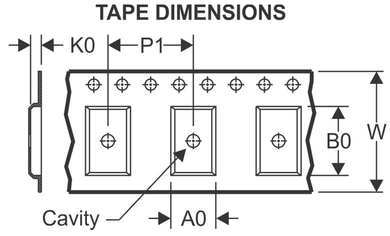
- Automotive: TPS2561-Q1

NOTE: Qualified Version Definitions:

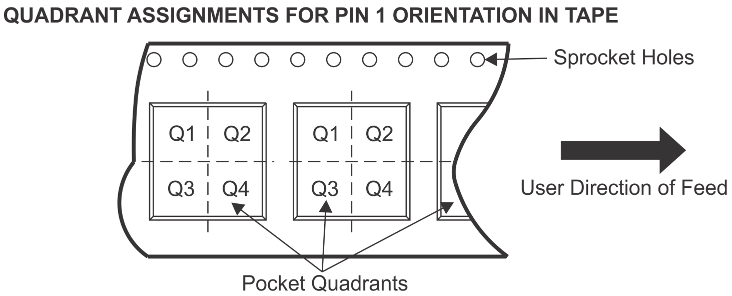
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION





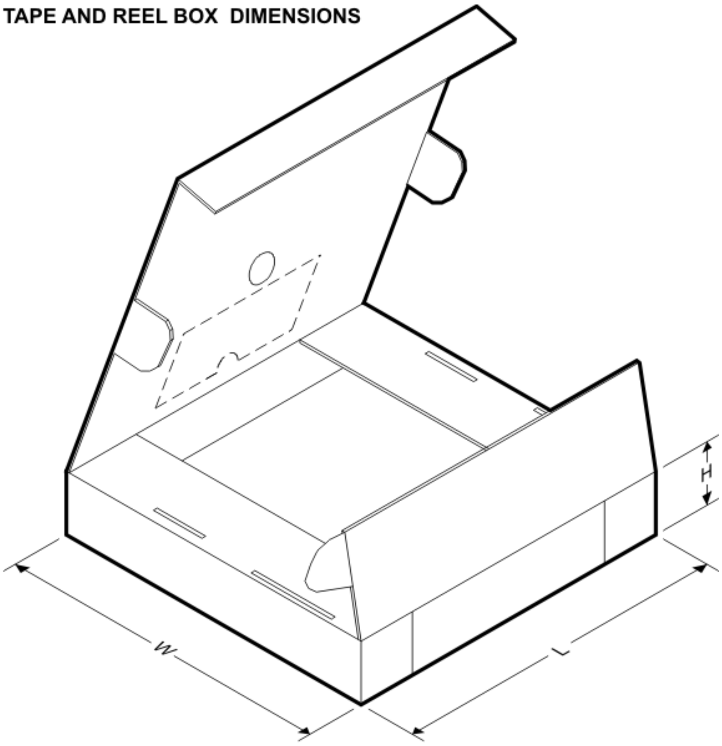
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS2560DRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS2560DRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS2560DRCT	VSON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS2560DRCT	VSON	DRC	10	250	180.0	12.5	3.3	3.3	1.1	8.0	12.0	Q2
TPS2561DRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS2561DRCT	VSON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS

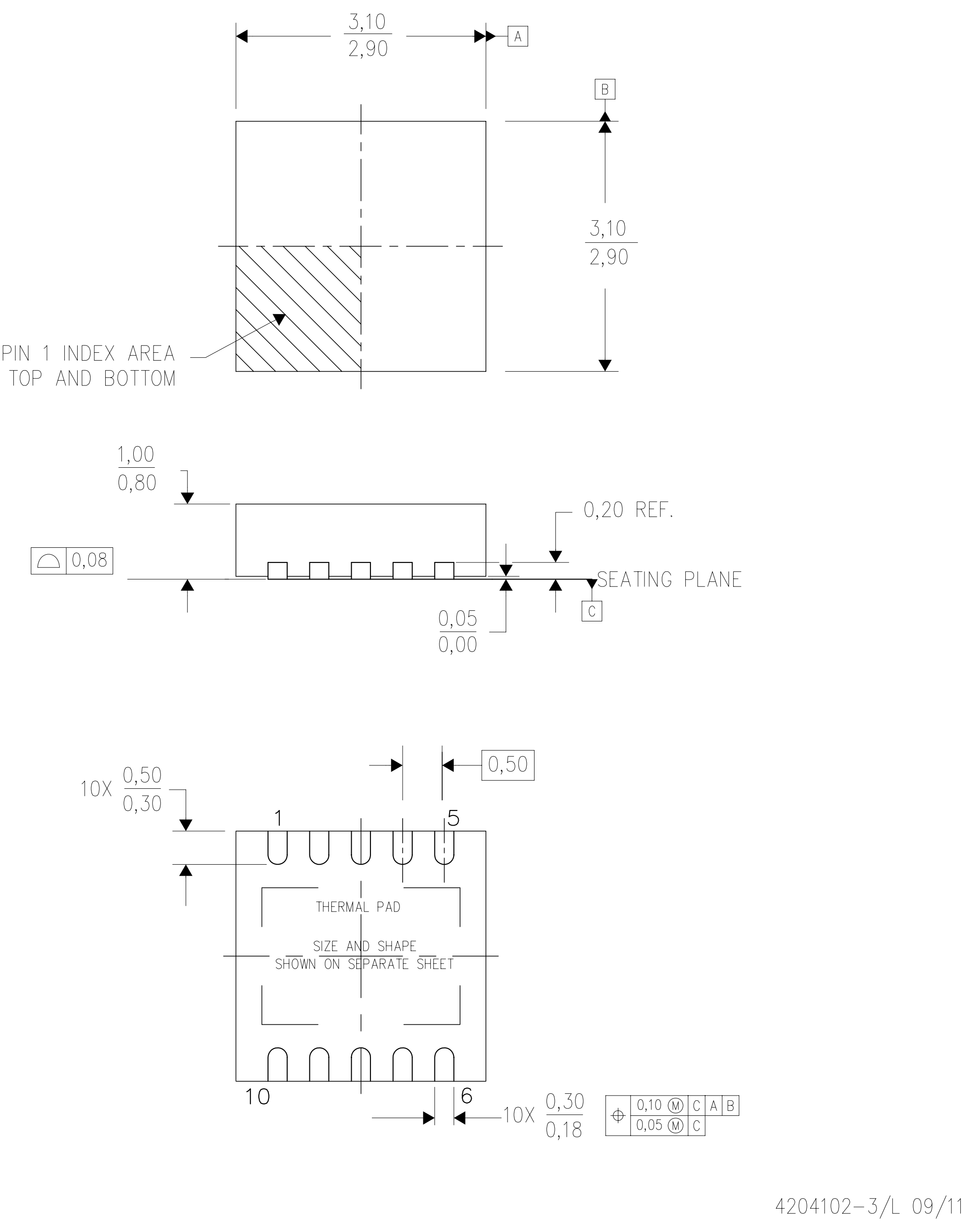


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS2560DRCR	VSON	DRC	10	3000	367.0	367.0	35.0
TPS2560DRCR	VSON	DRC	10	3000	338.0	355.0	50.0
TPS2560DRCT	VSON	DRC	10	250	210.0	185.0	35.0
TPS2560DRCT	VSON	DRC	10	250	338.0	355.0	50.0
TPS2561DRCR	VSON	DRC	10	3000	367.0	367.0	35.0
TPS2561DRCT	VSON	DRC	10	250	210.0	185.0	35.0

MECHANICAL DATA

DRC (S–PVSON–N10) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance, if present.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions, if present

THERMAL PAD MECHANICAL DATA

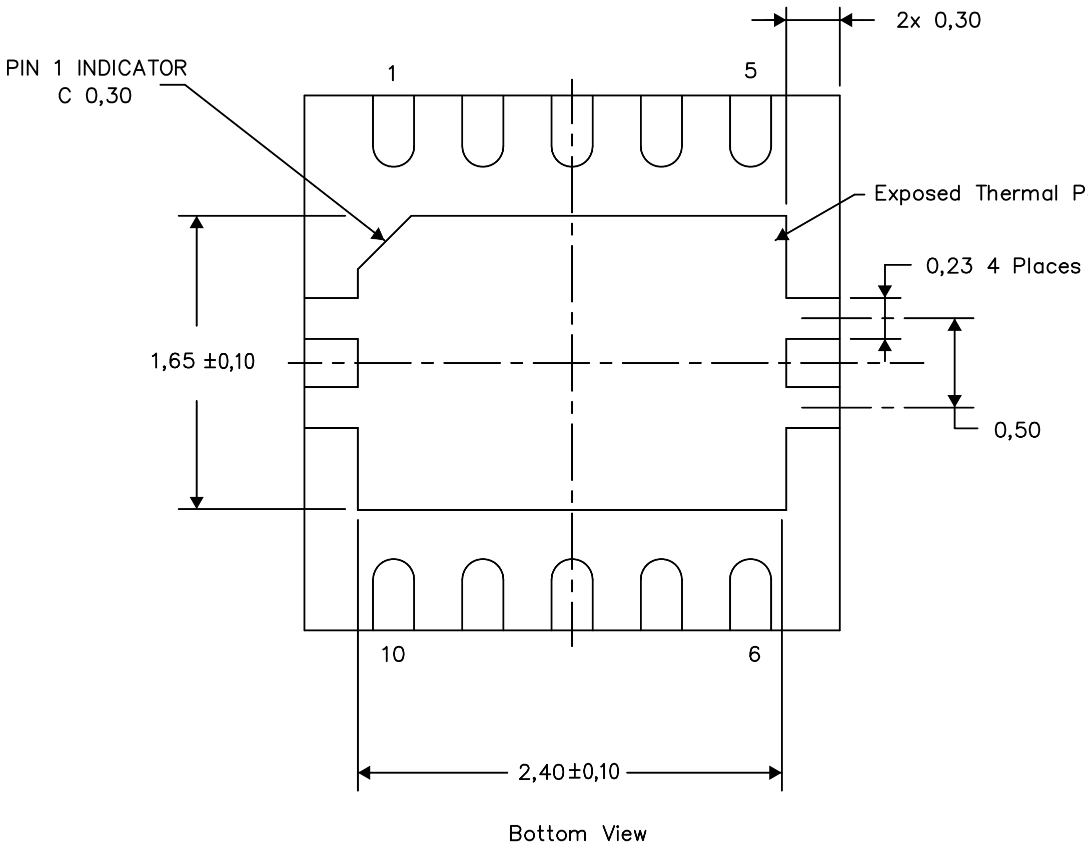
DRC (S-PVSON-N10) PLASTIC SMALL OUTLINE NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



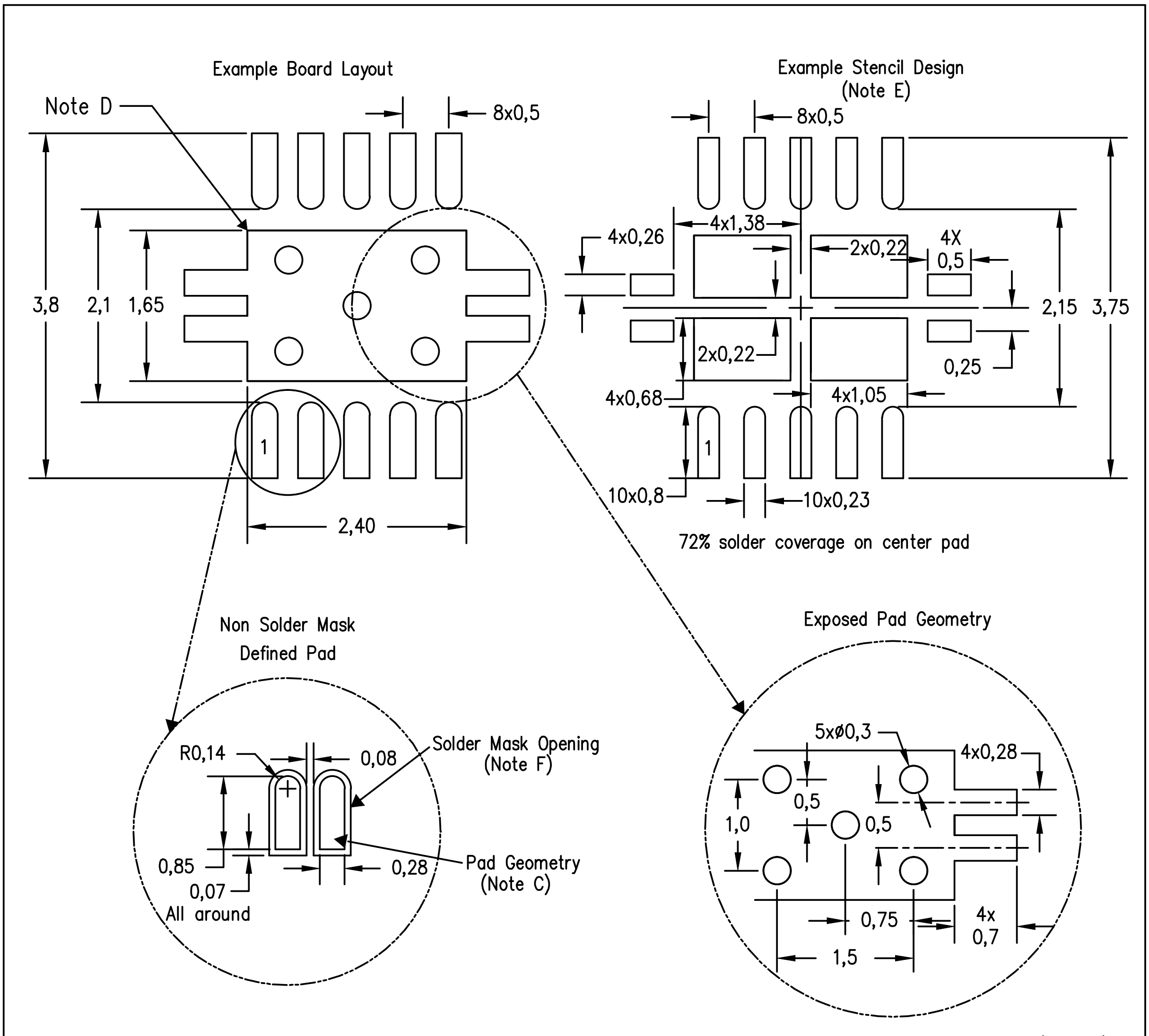
Exposed Thermal Pad Dimensions

4206565-3/Y 08/15

NOTE: A. All linear dimensions are in millimeters

LAND PATTERN DATA

DRC (S-PVSON-N10) PLASTIC SMALL OUTLINE NO-LEAD



4206987-2/P 04/16

NOTES:

A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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