UCC28C4x-Q1 BiCMOS Low-Power Current-Mode PWM Controllers

1 Features

- Qualified for Automotive Applications
- Enhanced Replacements for UC2842A Family With Pin-to-Pin Compatibility
- 1-MHz Operation
- 50-µA Standby Current, 100-µA Maximum
- Low Operating Current of 2.3 mA at 52 kHz
- Fast 35-ns Cycle-by-Cycle Overcurrent Limiting
- ±1-A Peak Output Current
- Rail-to-Rail Output Swings With 25-ns Rise and 20-ns Fall Times
- ±1% Initial Trimmed 2.5-V Error Amplifier Reference
- Trimmed Oscillator Discharge Current
- New Undervoltage Lockout Versions

2 Applications

- Switch Mode Power Supplies
- DC-to-DC Converters
- Board Mount Power Modules

3 Description

The UCC28C4x family are high performance current-mode PWM controllers. They are enhanced BiCMOS versions with pin-for-pin compatibility to the industry standard UC284xA family and UC284x family of PWM controllers. In addition, a lower startup voltage versions of 7 V is offered as UCC28C41.

Providing necessary features to control fixed frequency, peak current mode power supplies, this family offers several performance advantages. These devices offer high frequency operation up to 1 MHz with low start up and operating currents, thus minimizing start up loss and low operating power consumption for improved efficiency. The devices also feature a fast current sense to output delay time of 35 ns, and a ±1-A peak output current capability with improved rise and fall times for driving large external MOSFETs directly.

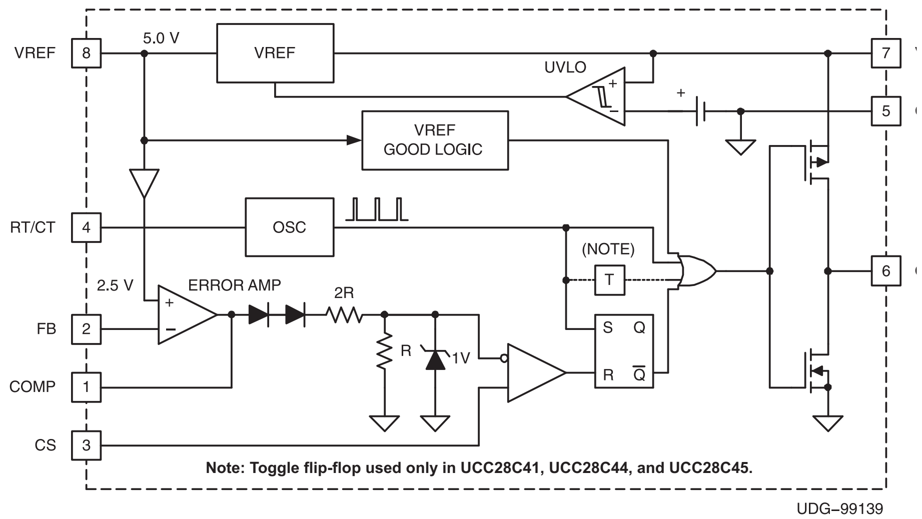
The UCC28C4x family is offered in the 8-pin SOIC (D) package.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
UCC28C4x	SOIC (8)	4.90 mm × 3.91 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Functional Block Diagram



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (December 2009) to Revision A — **Page**

- Deleted Ordering Information table, see POA at the end of the datasheet. ... 1
- Added *Device Information* table, *Pin Configuration and Functions* section, *Detailed Description* section, *Application and Implementation* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. ... 1
- Deleted T_J max on Elec Chars condition. Updated T_A from 105°C to 125°C ... 5

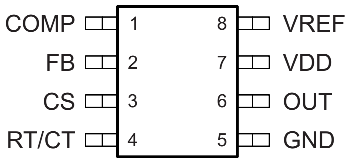
5 Device Comparison Table

MAXIMUM DUTY CYCLE	UVLO ON/OFF	ORDERABLE PART NUMBER
100%	8.4 V / 7.6 V	UCC28C43QDRQ1 (1)
50%	8.4 V / 7.6 V	UCC28C45QDRQ1 (1)
	7.0 V / 6.6 V	UCC28C41QDRQ1

(1) Product Preview

6 Pin Configuration and Functions

D Package
8-Pin SOIC
Top View



Pin Functions

PINS		I/O	DESCRIPTION
NAME	NO.		
COMP	1	O	This pin provides the output of the error amplifier for compensation. In addition, the COMP pin is frequently used as a control port by utilizing a secondary-side error amplifier to send an error signal across the secondary-primary isolation boundary through an opto-isolator.
CS	3	I	The current-sense pin is the noninverting input to the PWM comparator. This is compared to a signal proportional to the error amplifier output voltage. A voltage ramp can be applied to this pin to run the device with a voltage mode control configuration.
FB	2	I	This pin is the inverting input to the error amplifier. The noninverting input to the error amplifier is internally trimmed to 2.5 V ± 1%.
GND	5		Ground return pin for the output driver stage and the logic-level controller section.
OUT	6	O	The output of the on-chip drive stage. OUT is intended to directly drive a MOSFET. The OUT pin in the UCC28C43 is the same frequency as the oscillator, and can operate near 100% duty cycle. In the UCC28C41 UCC28C45, the frequency of OUT is one-half that of the oscillator due to an internal T flipflop. This limits the maximum duty cycle to <50%.
RT/CT	4		Timing resistor and timing capacitor. The timing capacitor should be connected to the device ground using minimal trace length.
VDD	7		Power supply pin for the device. This pin should be bypassed with a 0.1 µF capacitor with minimal trace lengths. Additional capacitance may be needed to provide hold up power to the device during startup.
VREF	8	O	5-V reference. For stability, the reference should be bypassed with a 0.1 µF capacitor to ground using the minimal trace length possible.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted), see [(1)(2)]

			MIN	MAX	UNIT
VDD	Supply voltage			20	V
I_{CC}	Maximum supply current			30	mA
$I_{OUT(pk)}$	Output current, peak			±1	A
	Output energy, capacitive load			5	µJ
	Voltage rating	COMP, CS, FB	–0.3	6.3	V
		OUT	–0.3	20	
		RT/CT	–0.3	6.3	
		VREF		7	
	Error amplifier output sink current			10	mA
T_J	Operating junction temperature range		–40	150	°C
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to ground. Currents are positive into and negative out of the specified terminals.

7.2 Recommended Operating Conditions

		MIN	MAX	UNIT
V_{DD}	Input voltage		18	V
V_{OUT}	Output voltage		18	V
I_{OUT} [(1)]	Average output current		200	mA
$I_{OUT(ref)}$ [(1)]	Reference output current		–20	mA

(1) It is not recommended that the device operate under conditions beyond those specified in this table for extended periods of time.

7.3 Electrical Characteristics

V_{DD} = 15 V(1), R_T = 10 kΩ, C_T = 3.3 nF, C_{VDD} = 0.1 μF and no load on the outputs, T_A = –40°C to 125°C

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Reference						
	Output voltage, initial accuracy	T_A = 25°C , I_{OUT} = 1 mA	4.9	5	5.1	V
	Line regulation	V_{DD} = 12 V to 18 V		0.2	20	mV
	Load regulation	1 mA to 20 mA		3	25	mV
	Temperature stability	(2)		0.2	0.4	mV/°C
	Total output variation	(2)	4.82		5.18	V
	Output noise voltage	10 Hz to 10 kHz, T_A = 25°C		50		μV
	Long term stability	1000 hours, T_A = 125°C(2)		5	25	mV
	Output short circuit current		–30	–45	–60	mA
Oscillator						
	Initial accuracy	T_A = 25°C(3)	50.5	53	55	kHz
		T_A = Full Range(3)	50.5		57	KHz
	Voltage stability	V_{DD} = 12 V to 18 V		0.2	2.85	%
	Temperature stability	T_{MIN} to T_{MAX}(2)		1	2.5	%
	Amplitude	RT/CT pin peak to peak		1.9		V
	Discharge current	T_A = 25°C, RT/CT = 2 V(4)	7.7	8.4	9	mA
		RT/CT = 2 V(4)	7.2	8.4	9.5	mA
Error Amplifier						
	Feedback input voltage, initial accuracy	V_{COMP} = 2.5 V, T_A = 25°C	2.475	2.500	2.525	V
	Feedback input voltage, total variation	V_{COMP} = 2.5 V	2.4	2.5	2.55	V
	Input bias current			–0.1	–2	μA
A_{VOL}	Open-loop voltage gain	V_{OUT} = 2 V to 4 V	65	90		dB
	Unity gain bandwidth			1.5		MHz
PSRR	Power-supply rejection ratio	V_{DD} = 12 V to 18 V	60			dB
	Output sink current	V_{FB} = 2.7 V, V_{COMP} = 1.1 V	2	14		mA
	Output source current	V_{FB} = 2.3 V, V_{COMP} = 5 V	–0.5	–1		mA
V_{OH}	High-level output voltage	V_{FB} = 2.3 V, R_{LOAD} = 15 k to GND	5	6.8		V
V_{OL}	Low-level output voltage	V_{FB} = 2.7 V, R_{LOAD} = 15 k to VREF		0.1	1.1	V
Current Sense						
	Gain	T_A = 25°C (5)(6)	2.75	3	3.15	V/V
		T_A = Full Range (5)(6)	2.825		3.15	V/V
	Maximum input signal	V_{FB} < 2.4 V	0.9	1	1.1	V
PSRR	Power-supply rejection ratio	V_{DD} = 12 V to 18 V(2)(5)		70		dB
	Input bias current			–0.1	–2	μA
	CS to output delay			35	70	ns
	COMP to CS offset	V_{CS} = 0 V		1.15		V
Output						
	V_{OUT} low ($R_{DS(on)}$ pulldown)	I_{SINK} = 200 mA		5.5	15	Ω
	V_{OUT} high ($R_{DS(on)}$ pullup)	I_{SOURCE} = 200 mA		10	25	Ω
	Rise tIme	T_A = 25°C, C_{LOAD} = 1 nF		25	50	ns
	Fall time	T_A = 25°C, C_{LOAD} = 1 nF		20	40	ns

(1) Adjust V_{DD} above the start threshold before setting at 15 V.
(2) Specified by design; not production tested
(3) Output frequencies of the UCC28C41 and UCC28C45 are one-half the oscillator frequency.
(4) Oscillator discharge current is measured with R_T = 10 kΩ to V_{REF}.
(5) Parameter measured at trip point of latch with V_{FB} = 0 V.
(6) Gain is defined as $ACS = \frac{\Delta V_{COM}}{\Delta V_{CS}}, 0\ V \le V_{CS} \le 900\ mV$

Electrical Characteristics (continued)

V_{DD} = 15 V(1), R_T = 10 kΩ, C_T = 3.3 nF, C_{VDD} = 0.1 µF and no load on the outputs, T_A = –40°C to 125°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Undervoltage Lockout (UVLO)						
	Start threshold	UCC28C43, UCC28C45	7.8	8.4	9	V
		UCC28C41	6.5	7	7.5	V
	Minimum operating voltage	UCC28C43, UCC28C45	7	7.6	8.2	V
		UCC28C41	6.1	6.6	7.1	V
PWM						
	Maximum duty cycle	UCC28C43	94	96		%
		UCC28C45, UCC28C41	47	48		%
	Minimum duty cycle				0%	
Current Supply						
$I_{START-UP}$	Start-up current	V_{DD} = UVLO start threshold (–0.5 V)		50	100	µA
I_{DD}	Operating supply current	V_{FB} = V_{CS} = 0 V		2.3	3	mA

7.4 Typical Characteristics

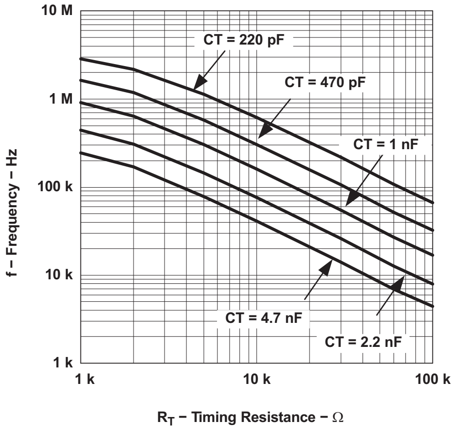


Figure 1. Oscillator Frequency vs Timing Resistance and Capacitance

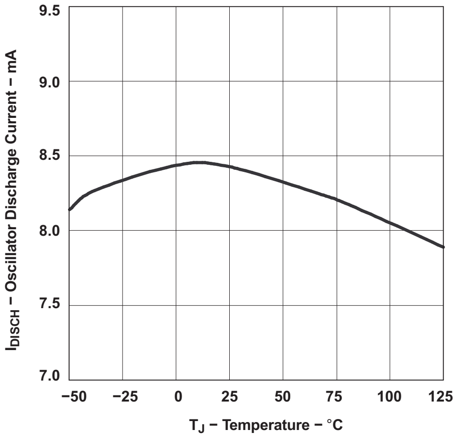


Figure 2. Oscillator Discharge Current vs Temperature

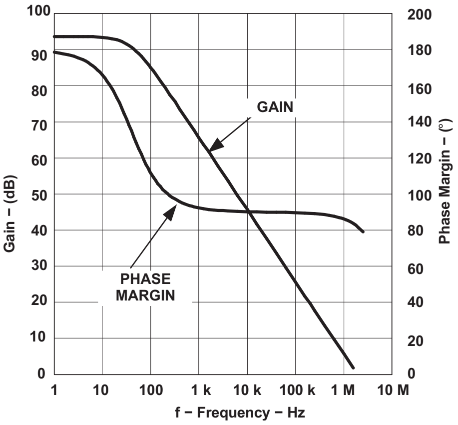


Figure 3. Error Amplifier Frequency Response

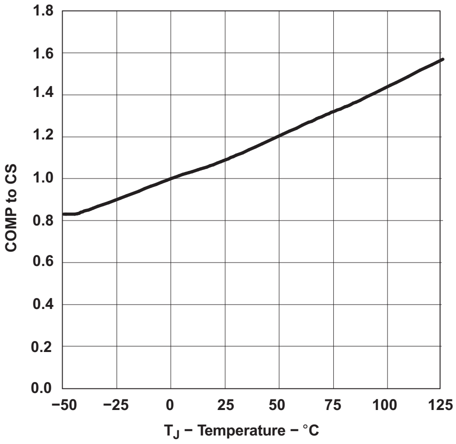


Figure 4. COMP to CS Offset Voltage (with CS = 0) vs Temperature

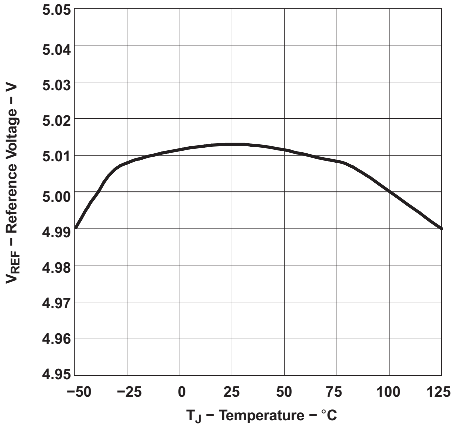


Figure 5. Reference Voltage vs Temperature

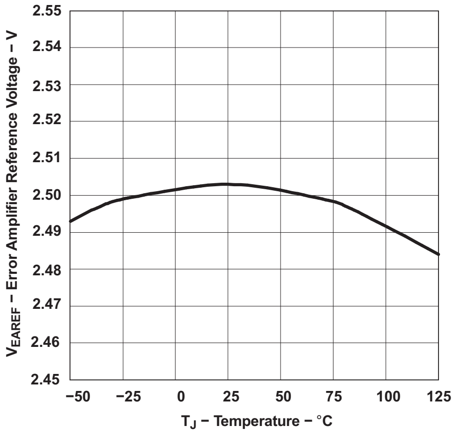


Figure 6. Error Amplifier Reference Voltage vs Temperature

Typical Characteristics (continued)

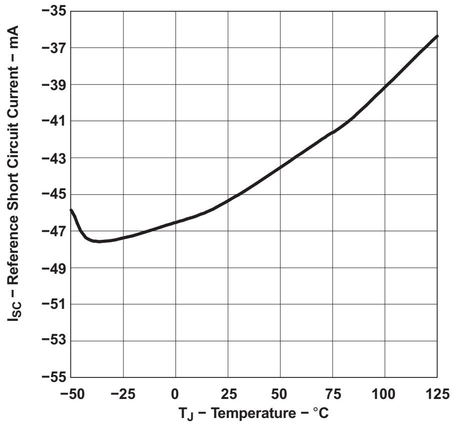


Figure 7. Reference Short-Circuit Current vs Temperature

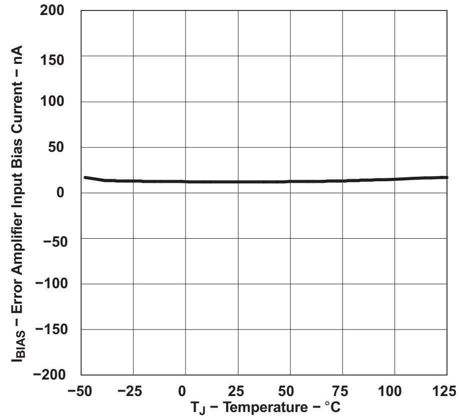


Figure 8. Error Amplifier Input BIAS Current vs Temperature

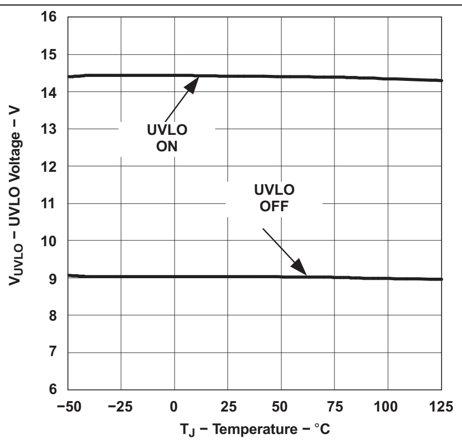


Figure 9. Undervoltage Lockout vs Temperature (UCC28C44)

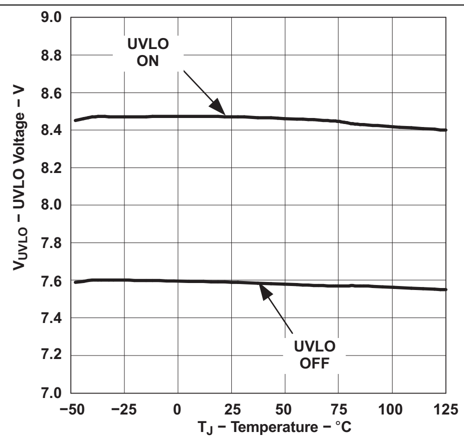


Figure 10. Undervoltage Lockout vs Temperature (UCC28C45)

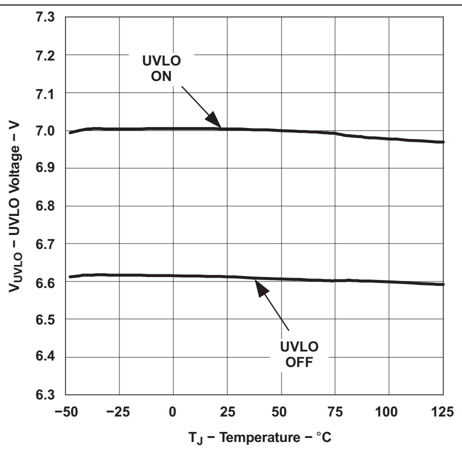


Figure 11. Undervoltage Lockout vs Temperature (UCC28C41)

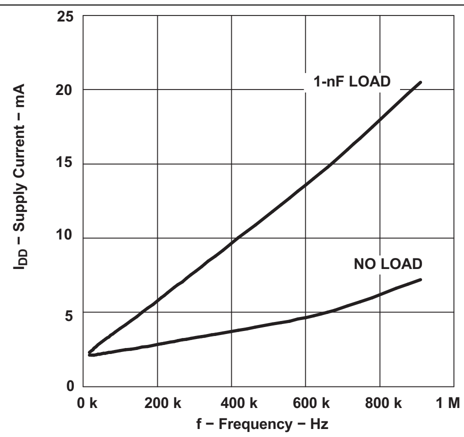


Figure 12. Supply Current vs Oscillator Frequency

Typical Characteristics (continued)

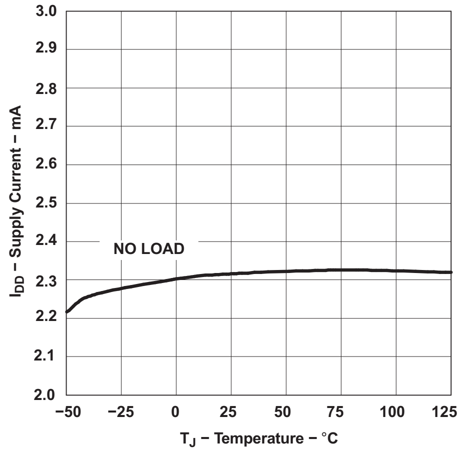


Figure 13. Supply Current vs Temperature

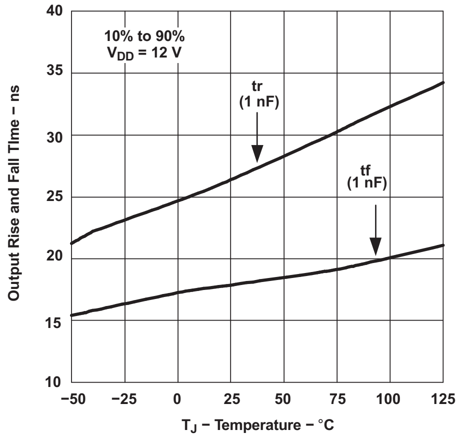


Figure 14. Output Rise Time and Fall Time vs Temperature

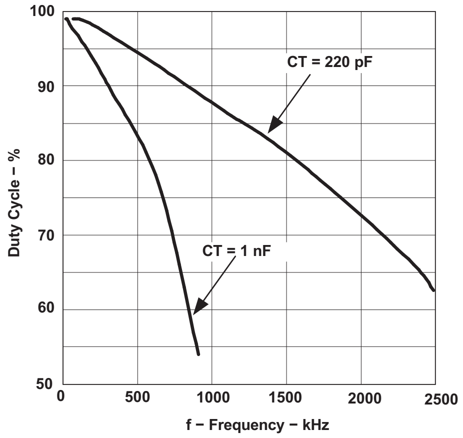


Figure 15. Maximum Duty Cycle vs Oscillator Frequency

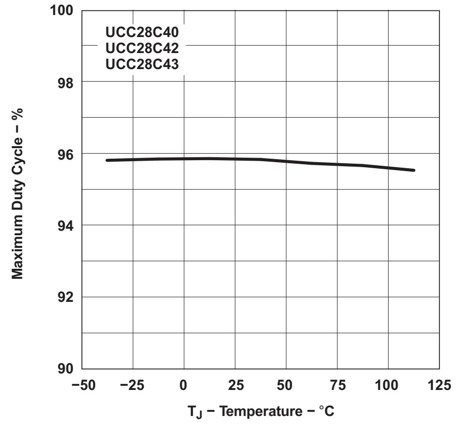


Figure 16. Maximum Duty Cycle vs Temperature

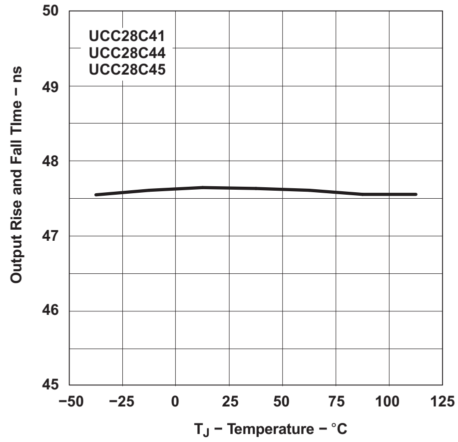


Figure 17. Maximum Duty Cycle vs Temperature

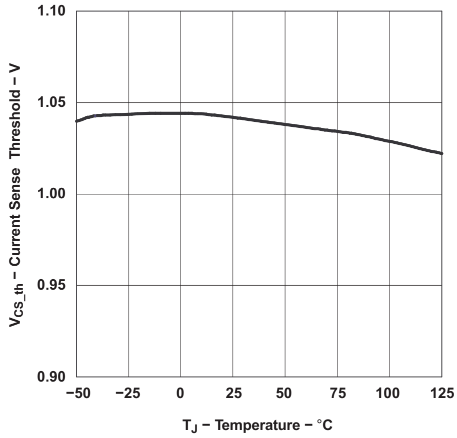


Figure 18. Current-Sense Threshold Voltage vs Temperature

Typical Characteristics (continued)

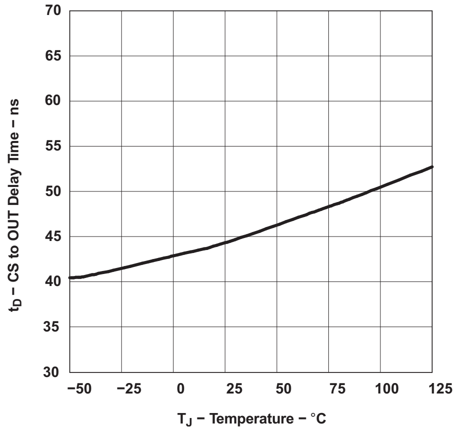


Figure 19. CS to Out Delay Time vs Temperature

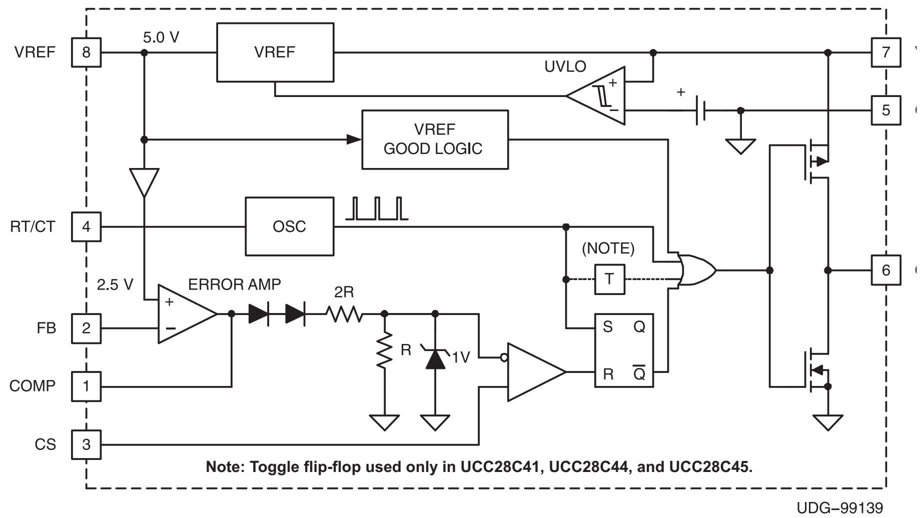
8 Detailed Description

8.1 Overview

This device is a pin-for-pin replacement of the bipolar UC2842 family of controllers—the industry standard PWM controller for single-ended converters. Familiarity with this controller family is assumed.

The UCC28C4x series is an enhanced replacement with pin-to-pin compatibility to the bipolar UC284x and UC284xA families. The new series offers improved performance when compared to older bipolar devices and other competitive BiCMOS devices with similar functionality. Note that these improvements discussed generally consist of tighter specification limits that are a subset of the older product ratings, maintaining drop-in capability. In new designs these improvements can be utilized to reduce the component count or enhance circuit performance when compared to the previously available devices.

8.2 Functional Block Diagram



9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

This device increases the total circuit efficiency whether operating off-line or in dc input circuits. In off-line applications the low start-up current of this device reduces steady state power dissipation in the startup resistor, and the low operating current maximizes efficiency while running. The low running current also provides an efficiency boost in battery-operated supplies.

9.1.1 Low-Voltage Operation

One member of the UCC28C4x family is intended for applications that require a lower start-up voltage than the original family members. The UCC28C41 has a turn-on voltage of 7 V typical and exhibit hysteresis of 0.4 V for a turn-off voltage of 6.6 V. This reduced start-up voltage enables use in systems with lower voltages, such as 12 V battery systems that are nearly discharged.

9.1.2 High-Speed Operation

The BiCMOS design allows operation at high frequencies that were not feasible in the predecessor bipolar devices. First, the output stage has been redesigned to drive the external power switch in approximately one-half the time of the earlier devices. Second, the internal oscillator is more robust, with less variation as frequency increases. In addition, the current sense to output delay has been reduced by a factor of three, to 45 ns typical. These features combine to provide a device capable of reliable high-frequency operation.

The UCC28C4x family oscillator is true to the curves of the original bipolar devices at lower frequencies, yet extends the frequency programmability range to at least 1 MHz. This allows the device to offer pin-to-pin capability where required, yet capable of extending the operational range to the higher frequencies typical of latest applications. When the original UC2842 was released in 1984, most switching supplies operated between 20 kHz and 100 kHz. Today, the UCC28C4x can be used in designs cover a span roughly ten times higher than those numbers.

9.1.3 Start/Run Current Improvements

The start-up current is only 60 µA typical, a significant reduction from the bipolar device's ratings of 300 µA (UC284xA). For operation over the full temperature range, the UCC28C4x devices offer a maximum startup current of 100 µA, an improvement over competitive BiCMOS devices. This allows the power-supply designer to further optimize the selection of the start-up resistor value to provide a more efficient design. In applications where low component cost overrides maximum efficiency the low run current of 2.3 mA typical may allow the control device to run directly through the single resistor to (+) rail, rather than needing a bootstrap winding on the power transformer, along with a rectifier. The start/run resistor for this case must also pass enough current to allow driving the primary switching MOSFET, which may be a few milliamps in small devices.

9.1.4 ±1% Initial Reference Voltage

The BiCMOS internal reference of 2.5 V has an enhanced design and utilizes production trim to allow initial accuracy of ±1% at room temperature and ±2% over the full temperature range. This can be used to eliminate an external reference in applications that do not require the extreme accuracy afforded by the additional device. This is very useful for nonisolated dc-to-dc applications where the control device is referenced to the same common as the output. It is also applicable in offline designs that regulate on the primary side of the isolation boundary by looking at a primary bias winding, or perhaps from a winding on the output inductor of a buck-derived circuit.

Application Information (continued)

9.1.5 Reduced Discharge Current Variation

The original UC2842 oscillator did not have trimmed discharged current, and the parameter was not specified on the data sheet. Since many customers attempted to use the discharge current to set a crude dead-time limit, the UC2842A family was released with a trimmed discharge current specified at 25°C. The UCC28C4x series now offers even tighter control of this parameter, with approximately ±3% accuracy at 25°C, and less than 10% variation over temperature using the UCC28C4x devices. This level of accuracy can enable a meaningful limit to be programmed, a feature not currently seen in competitive BiCMOS devices. The improved oscillator and reference also contribute to decreased variation in the peak-to-peak variation in the oscillator waveform, which is often used as the basis for slope compensation for the complete power system.

9.1.6 Soft-Start

Figure 20 provides a typical soft-start circuit for use with the UCC28C42. The values of R and C should be selected to bring the COMP pin up at a controlled rate, limiting the peak current supplied by the power stage. After the soft-start interval is complete, the capacitor continues to charge to V_{REF}, effectively removing the PNP transistor from circuit considerations.

The optional diode in parallel with the resistor forces a soft-start each time the PWM goes through UVLO and the reference (V_{REF}) goes low. Without the diode, the capacitor otherwise remains charged during a brief loss of supply or brownout, and no soft-start is enabled upon reapplication of VIN.

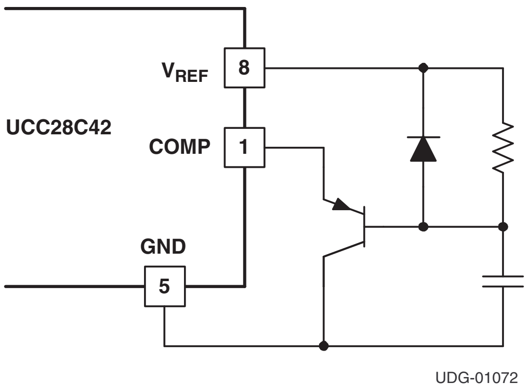


Figure 20. Typical Soft-Start Circuit

9.1.7 Oscillator Synchronization

The UCC28C4x oscillator has the same synchronization characteristics as the original bipolar devices. Thus, the information in the application report U-100A, *UC2842/3/4/5 Provides Low-Cost Current-Mode Control* (SLUA143) still applies. The application report describes how a small resistor from the timing capacitor to ground can offer an insertion point for synchronization to an external clock (see Figure 21 and Figure 22). Figure 21 shows how the UCC28C42 can be synchronized to an external clock source. This allows precise control of frequency and dead time with a digital pulse train.

Application Information (continued)

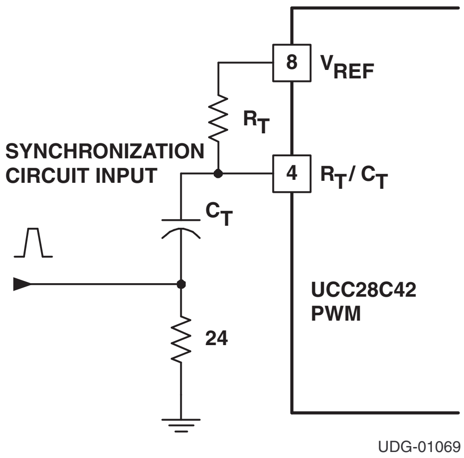


Figure 21. Oscillator Synchronization Circuit

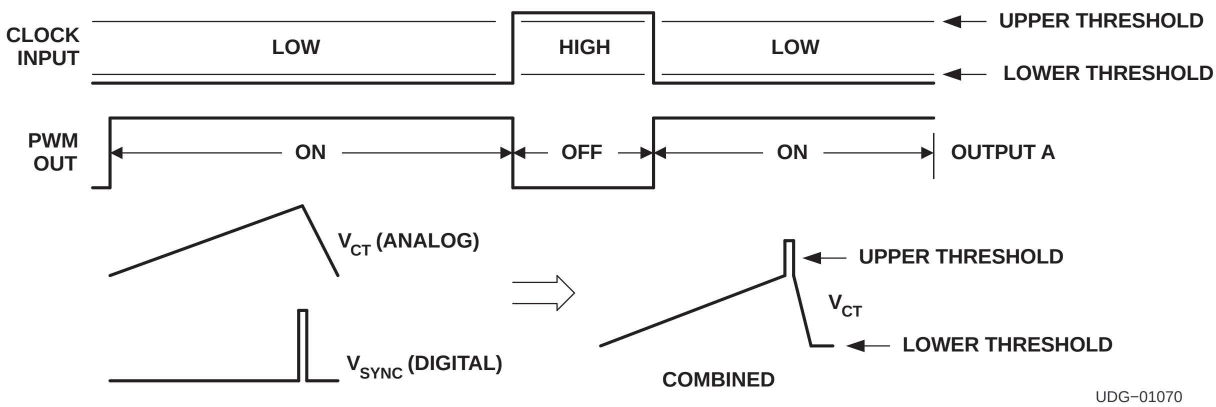


Figure 22. Synchronization to an External Clock

9.2 Typical Application

Figure 23 shows a typical off-line application.

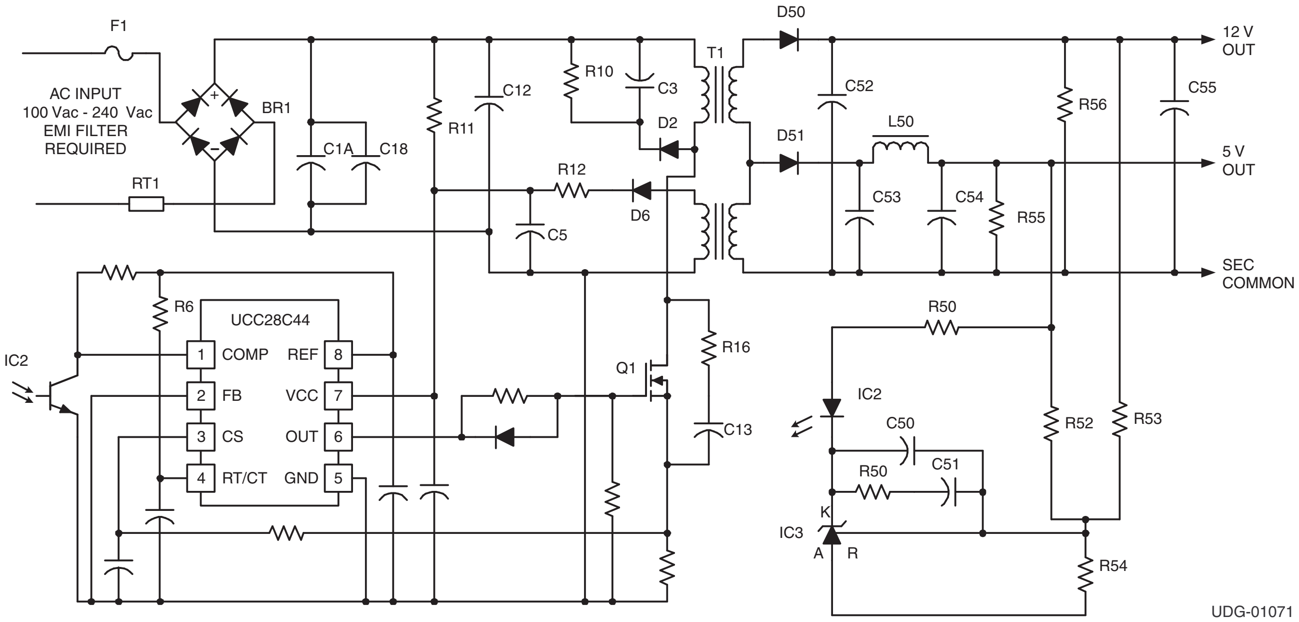


Figure 23. Typical Off-Line Application

Figure 24 shows the forward converter with synchronous rectification. This application provides 48 V to 3.3 V at 10 A with over 85% efficiency, and uses the UCC28C42 as the secondary-side controller and UCC3961 as the primary-side startup control device.

Typical Application (continued)

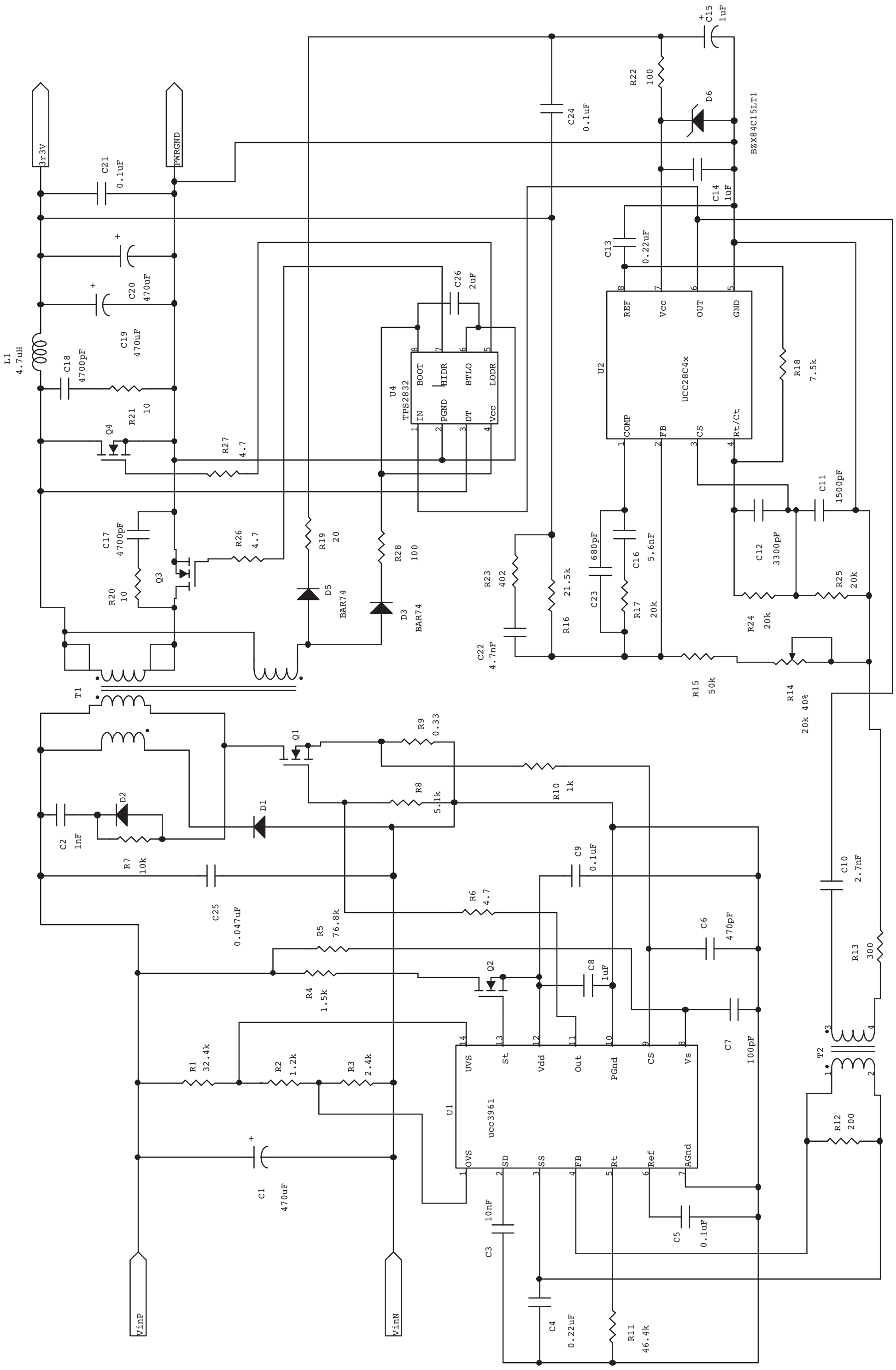


Figure 24. Forward Converter With Synchronous Rectification Using The UCC28C42 as the Secondary-Side Controller

10 Power Supply Recommendations

The absolute maximum supply voltage is 20 V, including any transients that may be present. If this voltage is exceeded, device damage is likely. This is in contrast to the predecessor bipolar devices that could survive up to 30 V. Thus, the supply pin should be decoupled as close to the ground pin as possible. Also, since no clamp is included in the device, the supply pin should be protected from external sources that could exceed the 20 V level.

11 Layout

11.1 Layout Guidelines

Careful layout of the printed board has always been a necessity for high-frequency power supplies. As the device switching speeds and operating frequencies increase, the layout of the converter becomes increasingly important.

This 8-pin device has only a single ground for the logic and power connections. This forces the gate drive current pulses to flow through the same ground that the control circuit uses for reference. Thus, the interconnect inductance should be minimized as much as possible. One implication is to place the device (gate driver) circuitry close to the MOSFET it is driving. Note that this can conflict with the need for the error amplifier and the feedback path to be away from the noise generating components.

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

UC2842/3/4/5 Provides Low-Cost Current-Mode Control (SLUA143)

12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
UCC28C41-Q1	Click here	Click here	Click here	Click here	Click here
UCC28C43-Q1	Click here	Click here	Click here	Click here	Click here
UCC28C45-Q1	Click here	Click here	Click here	Click here	Click here

12.3 Community Resource

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCC28C41QDRQ1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	28C41Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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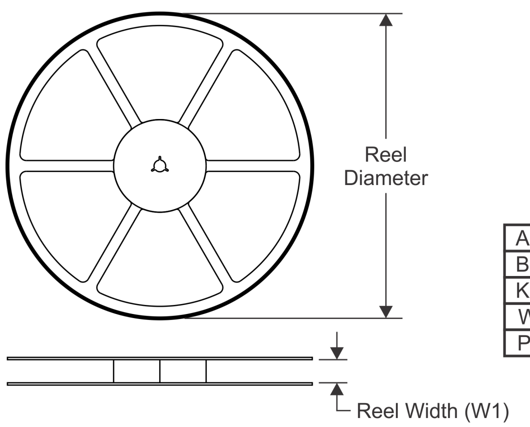
OTHER QUALIFIED VERSIONS OF UCC28C41-Q1 :

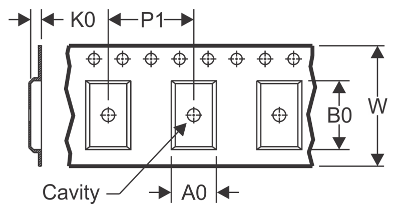
- Catalog: UCC28C41

NOTE: Qualified Version Definitions:

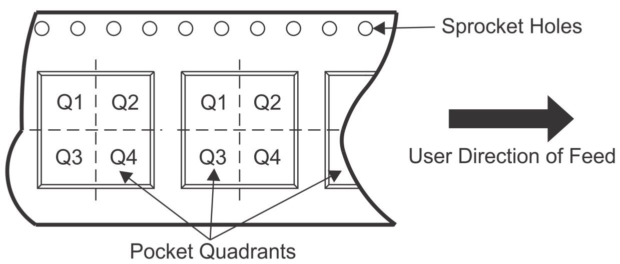
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION





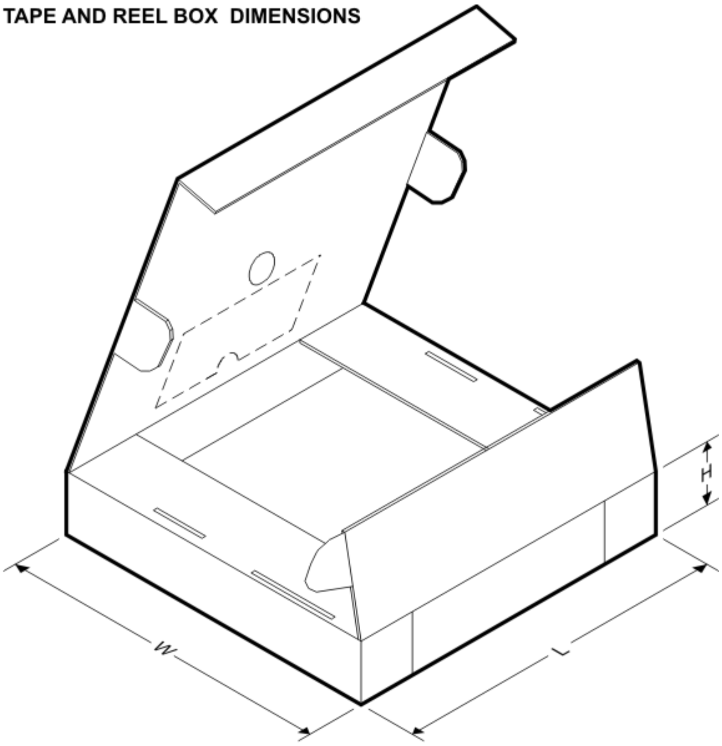
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC28C41QDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

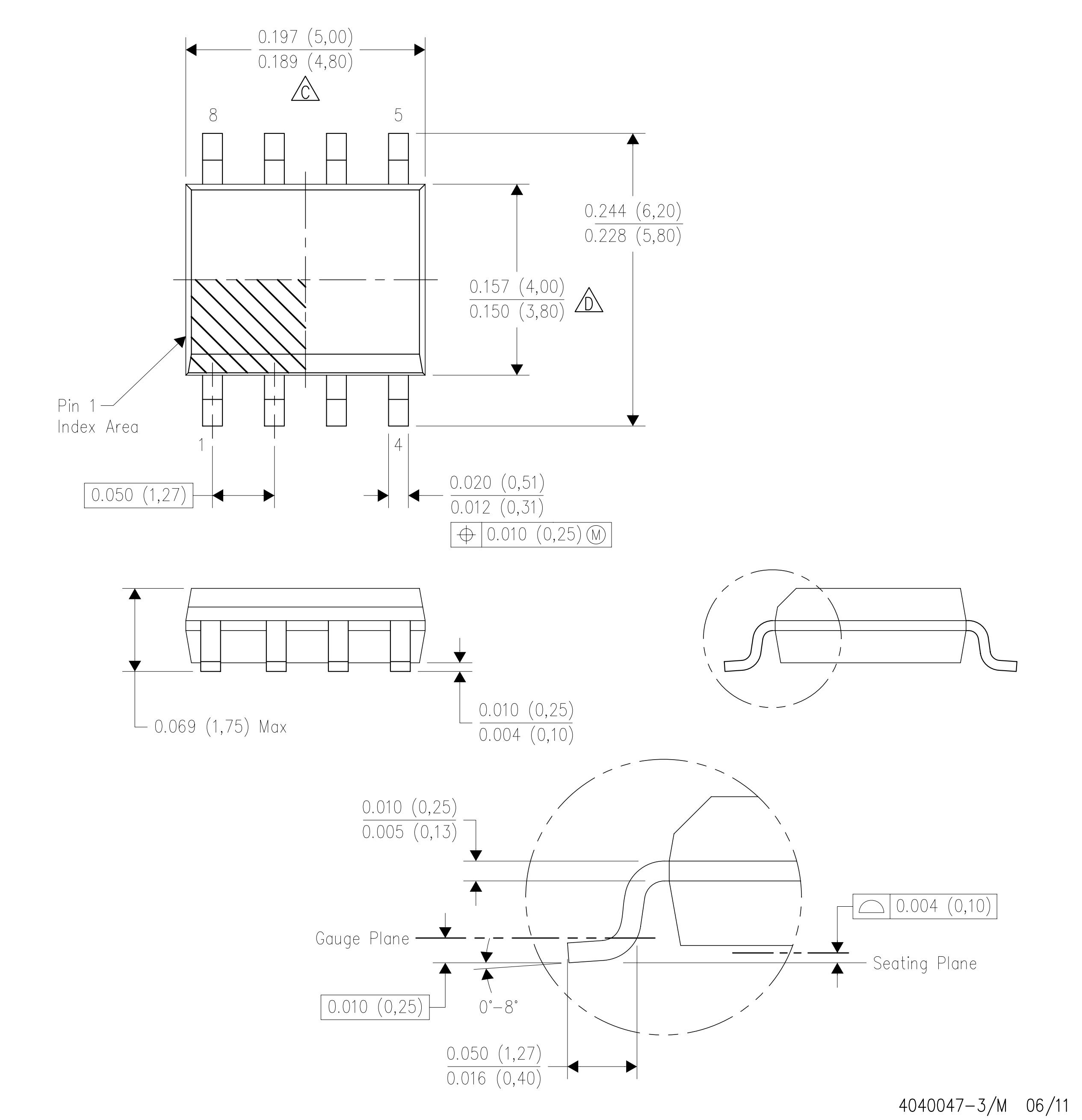
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC28C41QDRQ1	SOIC	D	8	2500	340.5	338.1	20.6

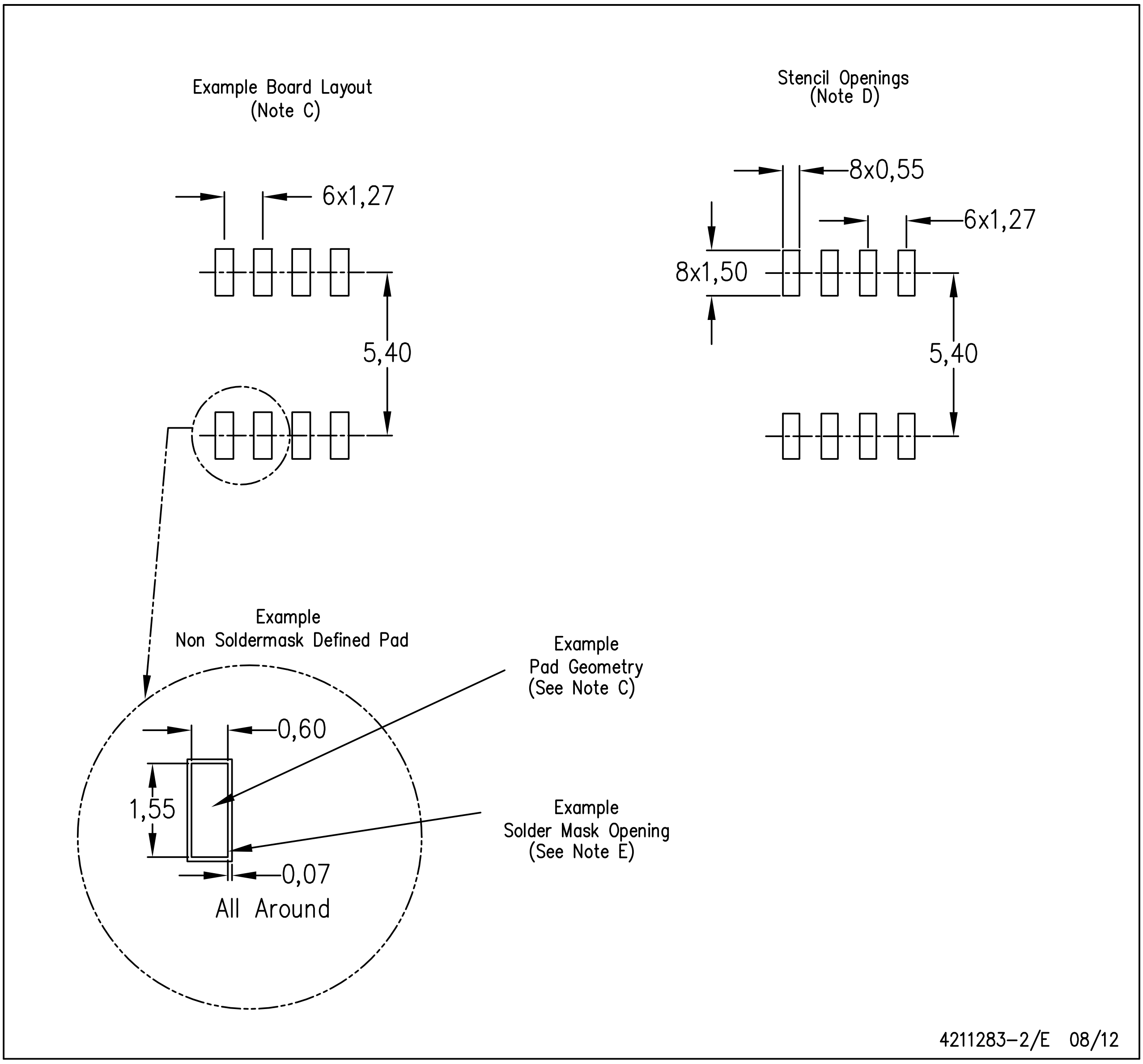
D (R-PDSO-G8) PLASTIC SMALL OUTLINE



4040047-3/M 06/11

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265