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STK30N2LLH5

N-channel 25 V, 0.0024 Ω , 30 A, PolarPAK[®]
STripFET[™]V Power MOSFET

Preliminary Data

Features

Type	V _{DSS}	R _{DS(on)} max	R _{DS(on)} *Q _g
STK30N2LLH5	25 V	< 0.0029 Ω	54 nC*m Ω

- Ultra low top and bottom junction to case thermal resistance
- R_{DS(on)} * Q_g industry benchmark
- Extremely low on-resistance R_{DS(on)}
- Very low switching gate charge
- Fully encapsulated die
- 100% matte tin finish (in compliance with the 2002/95/EC european directive)
- High avalanche ruggedness
- PolarPAK[®] is a trademark of VISHAY

Application

- Switching applications

Description

This product utilizes the 5th generation of design rules of ST's proprietary STripFET[™] technology. The lowest available R_{DS(on)} * Q_g in this chip scale package, makes this device suitable for the most demanding DC-DC converter applications, where high power density is to be achieved.

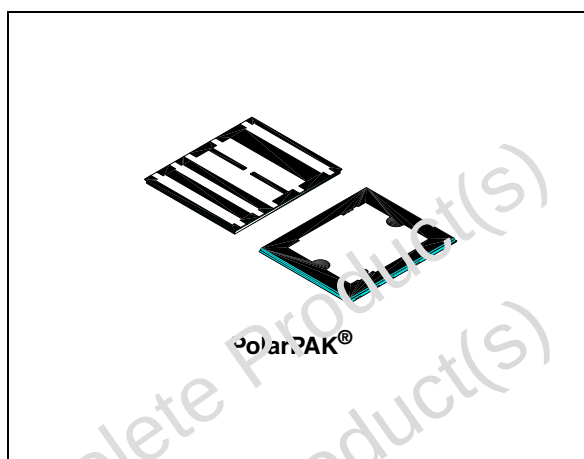


Figure 1. Internal schematic diagram

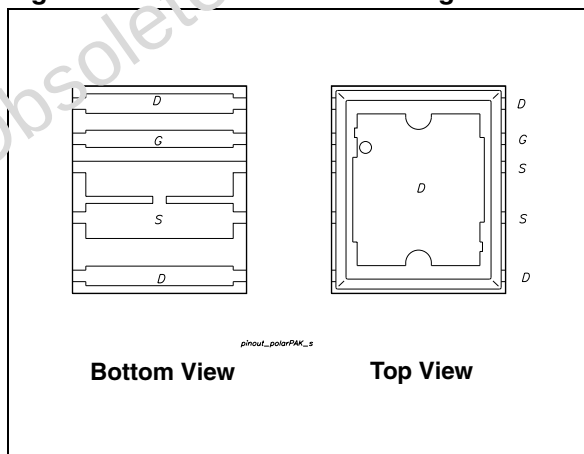


Table 1. Device summary

Order code	Marking	Package	Packaging
STK30N2LLH5	302L5	PolarPAK [®]	Tape and reel

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Electrical ratings

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage ($V_{GS} = 0$)	25	V
V_{GS}	Gate-source voltage	± 20	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25^\circ\text{C}$	30	A
I_D	Drain current (continuous) at $T_C = 100^\circ\text{C}$	18.75	A
$I_{DM}^{(2)}$	Drain current (pulsed)	120	A
$P_{TOT}^{(1)}$	Total dissipation at $T_C = 25^\circ\text{C}$	5.2	W
	Derating factor	0.0416	W/°C
$E_{AS}^{(3)}$	Single pulse avalanche energy	17BD	J
T_j T_{stg}	Operating junction temperature Storage temperature	-55 to 150	°C

1. When mounted on FR-4 board of 1inch², 2 oz Cu and $\leq 10\text{sec}$
2. Pulse width limited by package
3. Starting $T_j = 25^\circ\text{C}$, $I_D = 15\text{ A}$, $V_{DD} = 25\text{ V}$

Table 3. Thermal data

Symbol	Parameter	Typ.	Max.	Unit
$R_{thj-amb}^{(1)}$	Thermal resistance junction-amb	20	24	°C/W
$R_{thj-c}^{(2)}$	Thermal resistance junction-case (top drain)	1	1.2	°C/W
$R_{thj-c}^{(3)}$	Thermal resistance junction-case (source)	2.8	3.4	°C/W

1. When mounted on FR-4 board of 1inch², 2 oz Cu and $\leq 10\text{sec}$
2. Steady state
3. Measured at source pin when the device is mounted on FR-4 board in steady state

Electrical characteristics

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2 Electrical characteristics

(T_{CASE}=25°C unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	I _D = 250 μA, V _{GS} = 0	25			V
I _{DSS}	Zero gate voltage drain current (V _{GS} = 0)	V _{DS} = Max rating, V _{DS} = Max rating, T _C =125°C			1 10	μA μA
I _{GSS}	Gate body leakage current (V _{DS} = 0)	V _{GS} = ±20 V			±100	nA
V _{GS(th)}	Gate threshold voltage	V _{DS} = V _{GS} , I _D = 250 μA	1		2.5	V
R _{DS(on)}	Static drain-source on resistance	V _{GS} = 10 V, I _D = 15 A V _{GS} = 4.5 V, I _D = 15 A		0.0024 0.003	0.0029 0.0036	Ω Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C _{iss}	Input capacitance	V _{DS} = 25 V, f = 1 MHz, V _{GS} = 0		2290		pF
C _{oss}	Output capacitance			555		pF
C _{rss}	Reverse transfer capacitance			90		pF
Q _g	Total gate charge	V _{DD} = 15 V, I _D = 30 A		18		nC
Q _{gs}	Gate-source charge	V _{GS} = 4.5 V		TBD		nC
Q _{gd}	Gate-drain charge	(see Figure 3)		TBD		nC
Q _{gs1}	Pre V _{th} gate-to-source charge	V _{DD} = 15 V, I _D = 30 A		TBD		nC
Q _{gs2}	Post V _{th} gate-to-source charge	V _{GS} = 4.5 V (see Figure 8)		TBD		nC
R _G	Gate input resistance	f = 1 MHz Gate DC Bias = 0 Test signal level = 20 mV open drain		TBD		Ω

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Electrical characteristics

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD}=15\text{ V}$, $I_D=15\text{ A}$, $R_G=4.7\ \Omega$, $V_{GS}=4.5\text{ V}$ (see Figure 2)		TBD		ns
t_r	Rise time			TBD		ns
$t_{d(off)}$	Turn-off delay time	$V_{DD}=15\text{ V}$, $I_D=15\text{ A}$, $R_G=4.7\ \Omega$, $V_{GS}=4.5\text{ V}$ (see Figure 2)		TBD		ns
t_f	Fall time			TBD		ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current				30	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				120	A
$V_{SD}^{(2)}$	Forward on Voltage	$I_{SD}=30\text{ A}$, $V_{GS}=0$			1.1	V
t_{rr}	Reverse recovery time	$I_{SD}=30\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD}=20\text{ V}$, $T_j=150^\circ\text{C}$ (see Figure 7)		TBD		ns
Q_{rr}	Reverse recovery charge			TBD		nC
I_{RRM}	Reverse recovery current			TBD		A

1. Pulse width limited by package

2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

Test circuits

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3 Test circuits

Figure 2. Switching times test circuit for resistive load

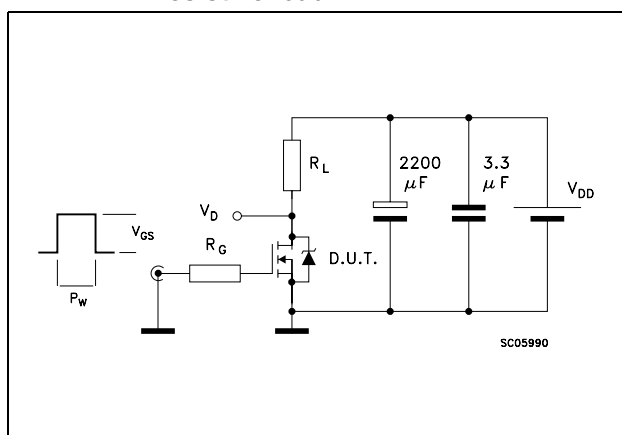


Figure 3. Gate charge test circuit

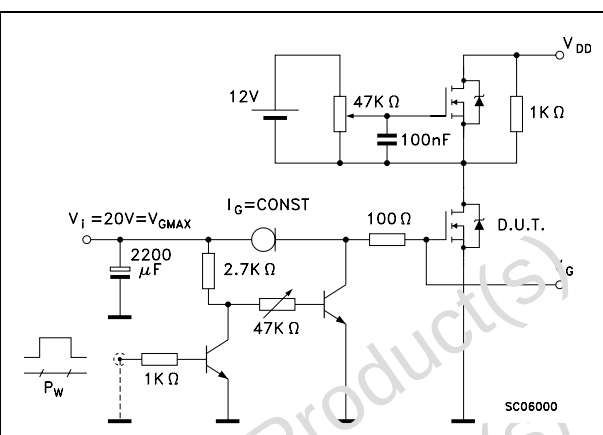


Figure 4. Test circuit for inductive load switching and diode recovery times

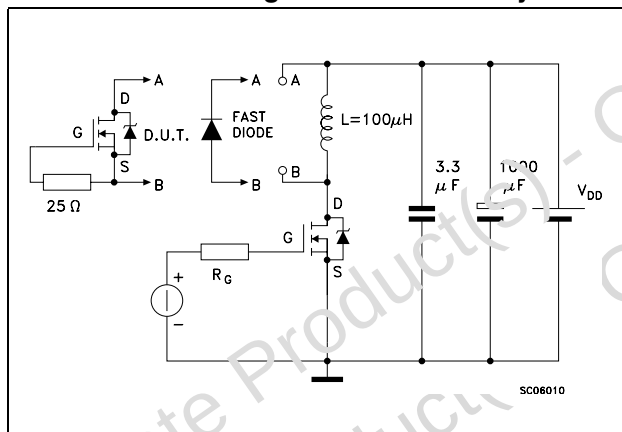


Figure 5. Unclamped inductive load test circuit

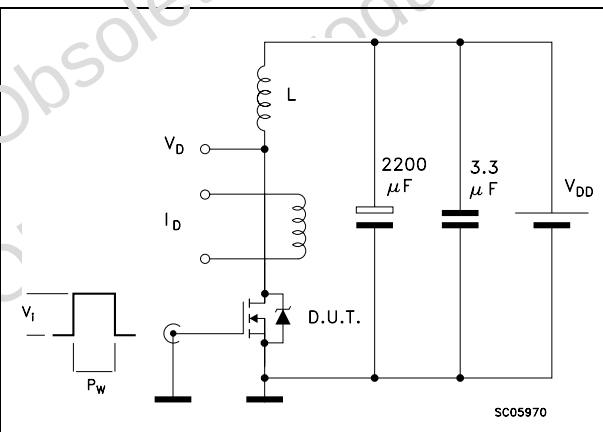


Figure 6. Unclamped inductive waveform

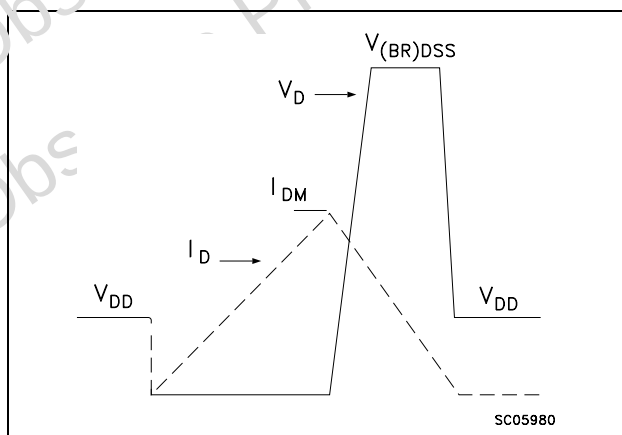
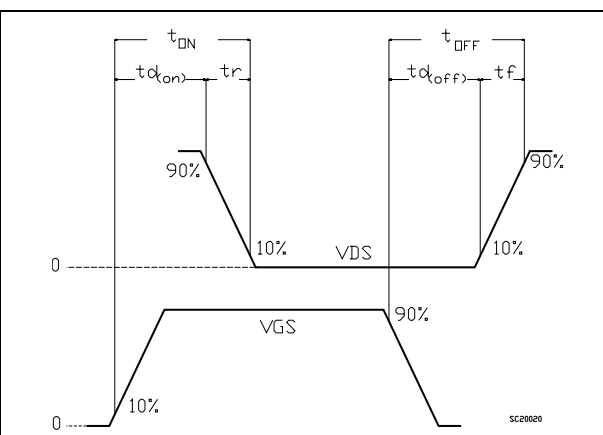


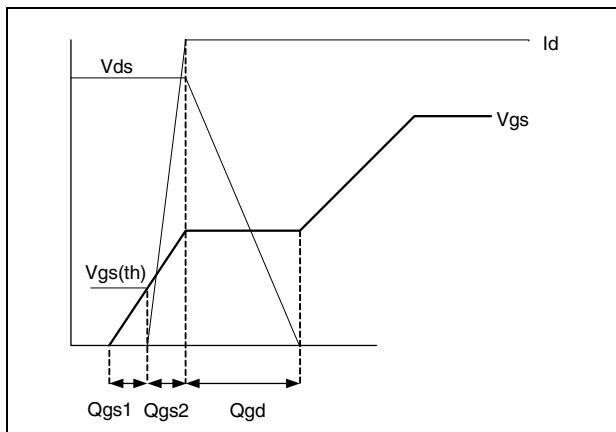
Figure 7. Switching time waveform



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Test circuits

Figure 8. Gate charge waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

Obsolete Product(s) - Obsolete Product(s)
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Package mechanical data

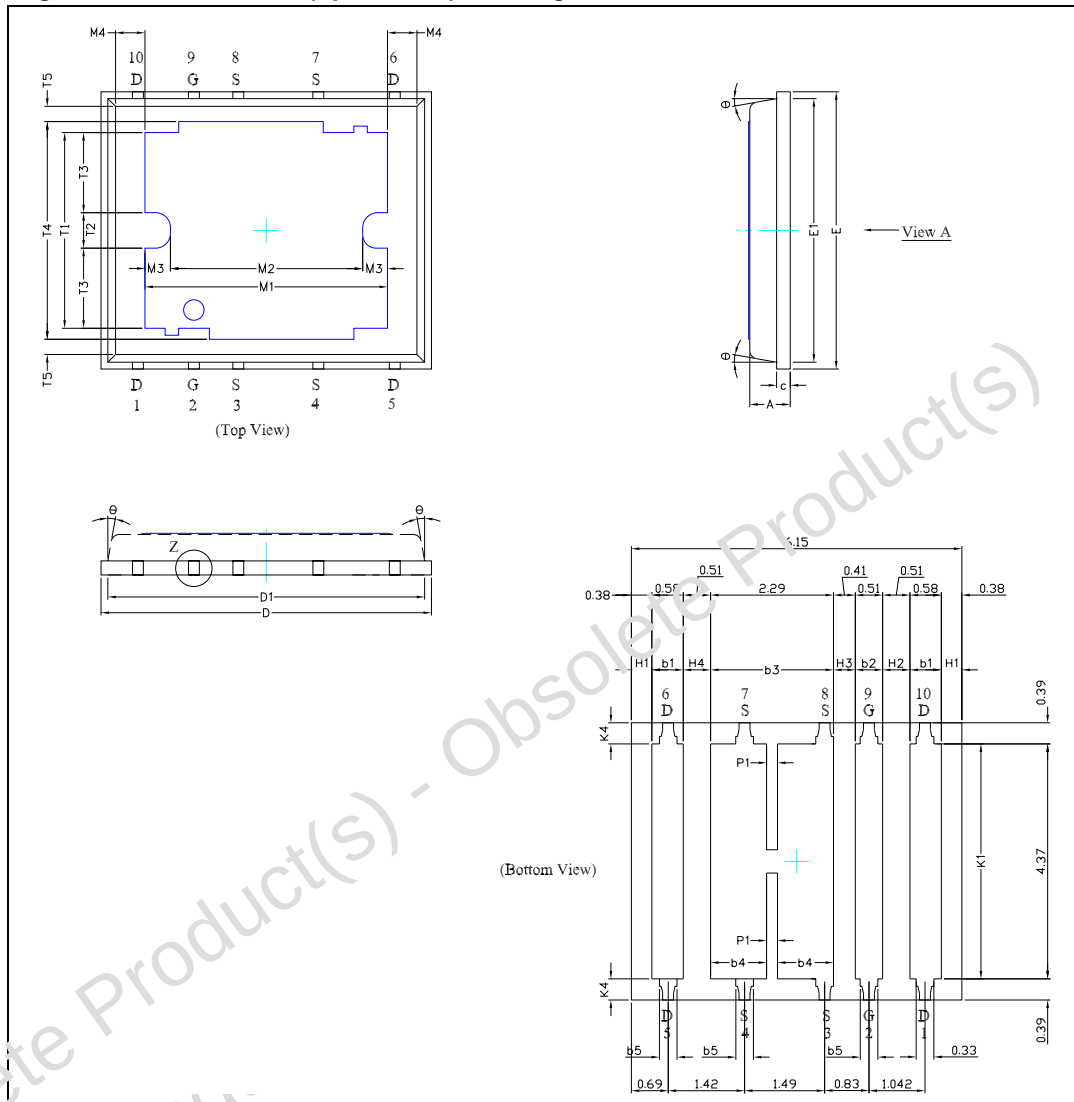
Table 8. PolarPAK® (option "S") mechanical data

Ref.	mm			inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.75	0.80	0.85	0.030	0.031	0.033
A1			0.05			0.002
b1	0.48	0.58	0.68	0.019	0.023	0.027
b2	0.41	0.51	0.61	0.016	0.020	0.024
b3	2.19	2.29	2.39	0.086	0.090	0.094
b4	0.89	1.04	1.19	0.035	0.041	0.047
b5	0.23	0.33	0.43	0.009	0.013	0.017
c	0.20	0.25	0.30	0.008	0.010	0.012
D	6	6.15	6.30	0.236	0.242	0.248
D1	5.74	5.89	6.04	0.226	0.232	0.238
E	5.01	5.16	5.31	0.197	0.203	0.209
E1	4.75	4.90	5.05	0.187	0.193	0.199
H1	0.23			0.009		
H2	0.45		0.56	0.018		0.022
H3	0.31	0.41	0.51	0.012	0.016	0.020
H4	0.45		0.56	0.018		0.022
I1	1.92	1.97	2.02	0.075	0.077	0.079
J1	0.38	0.43	0.48	0.014	0.016	0.018
K1	4.22	4.37	4.52	0.166	0.172	0.178
K4	0.24			0.009		
M1	4.30	4.50	4.70	0.169	0.177	0.185
M2	3.43	3.58	3.73	0.135	0.141	0.147
M3	0.22			0.009		
M4	0.05			0.002		
P1	0.15	0.20	0.25	0.006	0.008	0.010
T1	3.48	3.64	4.10	0.137	0.143	0.161
T2	0.56	0.76	0.95	0.022	0.030	0.037
T3	1.20			0.047		
T4	3.90			0.154		
T5		0.18	0.36		0.007	0.014
<	0°	10°	12°	0°	10°	12°

Package mechanical data

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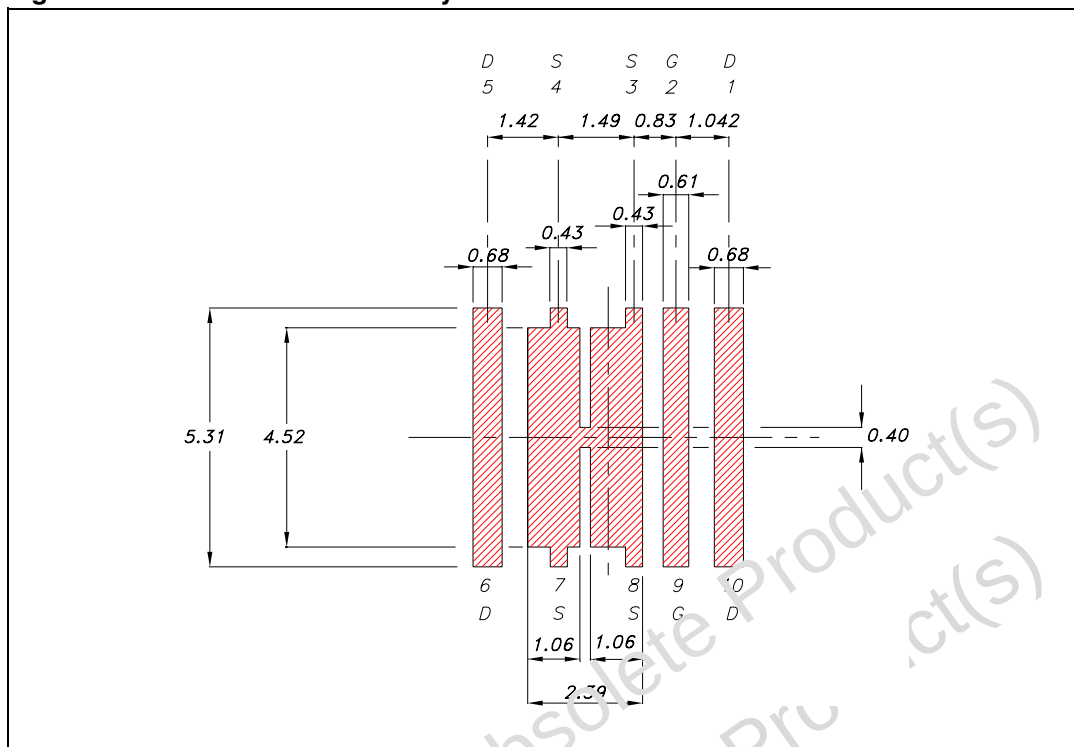
Figure 9. PolarPAK® (option "S") drawings



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Package mechanical data

Figure 10. Recommended PAD layout



Revision history

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5 Revision history

Table 9. Document revision history

Date	Revision	Changes
07-Jul-2008	1	First release

STK30N2LLH5

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