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CSD16340Q3 25-V N-Channel NexFET™ Power MOSFET

1 Features

- Optimized for 5 V Gate Drive
- Resistance Rated at $V_{GS} = 2.5\text{ V}$
- Ultra-Low Q_g and Q_{gd}
- Low Thermal Resistance
- Avalanche Rated
- Pb Free Terminal Plating
- RoHS Compliant
- Halogen Free
- SON 3.3-mm x 3.3-mm Plastic Package

2 Applications

- Point of Load Synchronous Buck Converter for Applications in Networking, Telecom, and Computing Systems
- Optimized for Control or Synchronous FET Applications

3 Description

This 25 V, 3.8 mΩ, 3.3 x 3.3 mm SON NexFET™ power MOSFET is designed to minimize losses in power conversion and optimized for 5 V gate drive applications.

Product Summary

$T_A = 25^\circ\text{C}$		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage	25	V
Q_g	Gate Charge Total (4.5 V)	6.5	nC
Q_{gd}	Gate Charge Gate-to-Drain	1.2	nC
$R_{DS(on)}$	Drain-to-Source On-Resistance	$V_{GS} = 2.5\text{ V}$	6.1 mΩ
		$V_{GS} = 4.5\text{ V}$	4.3 mΩ
		$V_{GS} = 8\text{ V}$	3.8 mΩ
V_{th}	Threshold Voltage	0.85	V

Ordering Information⁽¹⁾

Device	Media	Qty	Package	Ship
CSD16340Q3	13-Inch Reel	2500	SON 3.3 x 3.3 mm Plastic Package	Tape and Reel
CSD16340Q3T	7-Inch Reel	250		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

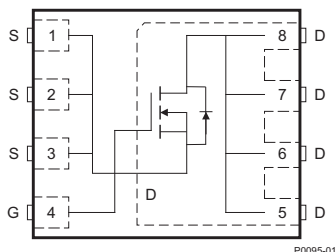
Absolute Maximum Ratings

$T_A = 25^\circ\text{C}$		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage	25	V
V_{GS}	Gate-to-Source Voltage	+10 / -8	V
I_D	Continuous Drain Current, $T_C = 25^\circ\text{C}$	60	A
	Continuous Drain Current ⁽¹⁾	21	A
I_{DM}	Pulsed Drain Current, $T_A = 25^\circ\text{C}$ ⁽²⁾	115	A
P_D	Power Dissipation ⁽¹⁾	3	W
T_J , T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150	$^\circ\text{C}$
E_{AS}	Avalanche Energy, single pulse $I_D = 40\text{ A}$, $L = 0.1\text{ mH}$, $R_G = 25\ \Omega$	80	mJ

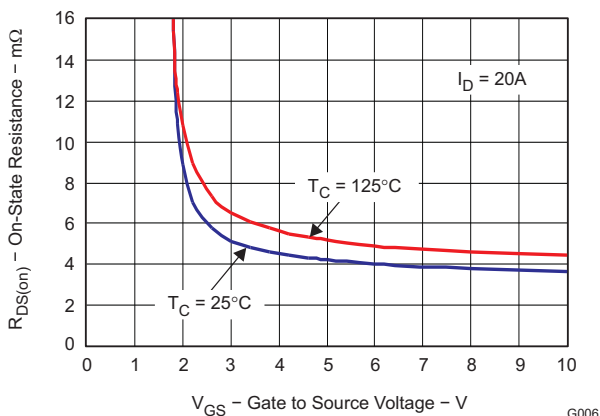
(1) Typical $R_{\theta JA} = 39^\circ\text{C/W}$ on 1in² Cu (2 oz.) on 0.060" thick FR4 PCB.

(2) Pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$

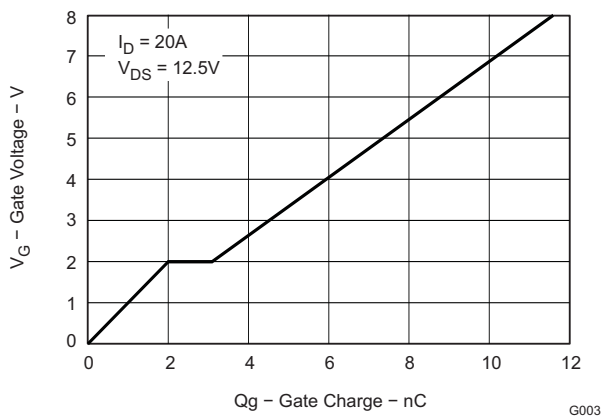
Top View



$R_{DS(on)}$ vs V_{GS}



Gate Charge



CSD16340Q3

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4 Revision History

Changes from Revision D (November 2011) to Revision E **Page**

- Added 7" reel to Ordering Information **1**
- Updated Mechanical Information **9**

Changes from Revision C (June 2011) to Revision D **Page**

- Replaced the THERMAL CHARACTERISTICS table with the new Thermal Information Table..... **4**
- Replaced [Figure 10](#) - Maximum Safe Operating Area **6**

Changes from Revision B (September 2010) to Revision C **Page**

- Deleted the Package Marking Information section **9**

Changes from Revision A (January 2010) to Revision B **Page**

- Changed [Figure 2](#), reversed the order of the V_{GS} labels..... **5**

Changes from Original (December 2009) to Revision A **Page**

- Changed Q_g in the PRODUCT SUMMARY table from: 6.8 To 6.5 nC **1**

5 Specifications

5.1 Electrical Characteristics

($T_A = 25^\circ\text{C}$ unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV_{DSS}	Drain-to-Source Voltage	$V_{GS} = 0\text{ V}, I_{DS} = 250\ \mu\text{A}$	25			V
I_{DSS}	Drain-to-Source Leakage Current	$V_{GS} = 0\text{ V}, V_{DS} = 20\text{ V}$			1	μA
I_{GSS}	Gate-to-Source Leakage Current	$V_{DS} = 0\text{ V}, V_{GS} = +10/-8\text{ V}$			100	nA
$V_{GS(th)}$	Gate-to-Source Threshold Voltage	$V_{DS} = V_{GS}, I_{DS} = 250\ \mu\text{A}$	0.6	0.85	1.1	V
$R_{DS(on)}$	Drain-to-Source On-Resistance	$V_{GS} = 2.5\text{ V}, I_{DS} = 20\text{ A}$		6.1	7.8	m Ω
		$V_{GS} = 4.5\text{ V}, I_{DS} = 20\text{ A}$		4.3	5.5	m Ω
		$V_{GS} = 8\text{ V}, I_{DS} = 20\text{ A}$		3.8	4.5	m Ω
g_{fs}	Transconductance	$V_{DS} = 15\text{ V}, I_{DS} = 20\text{ A}$		121		S
DYNAMIC CHARACTERISTICS						
C_{ISS}	Input Capacitance	$V_{GS} = 0\text{ V}, V_{DS} = 12.5\text{ V}, f = 1\text{ MHz}$		1050	1350	pF
C_{OSS}	Output Capacitance			730	950	pF
C_{RSS}	Reverse Transfer Capacitance			53	69	pF
R_g	Series Gate Resistance			1.5	3	Ω
Q_g	Gate Charge Total (4.5 V)	$V_{DS} = 12.5\text{ V}, I_D = 20\text{ A}$		6.5	9.2	nC
Q_{gd}	Gate Charge Gate-to-Drain			1.2		nC
Q_{gs}	Gate Charge Gate-to-Source			2.1		nC
$Q_g(th)$	Gate Charge at V_{th}			1		nC
Q_{OSS}	Output Charge	$V_{DS} = 13\text{ V}, V_{GS} = 0\text{ V}$		15		nC
$t_{d(on)}$	Turn On Delay Time	$V_{DS} = 12.5\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 20\text{ A}$ $R_G = 2\ \Omega$		4.8		ns
t_r	Rise Time			16.1		ns
$t_{d(off)}$	Turn Off Delay Time			13.8		ns
t_f	Fall Time			5.2		ns
DIODE CHARACTERISTICS						
V_{SD}	Diode Forward Voltage	$I_S = 20\text{ A}, V_{GS} = 0\text{ V}$		0.8	1	V
Q_{rr}	Reverse Recovery Charge	$V_{DD} = 13\text{ V}, I_F = 20\text{ A}, di/dt = 300\text{ A}/\mu\text{s}$		14.5		nC
t_{rr}	Reverse Recovery Time			20		ns

CSD16340Q3

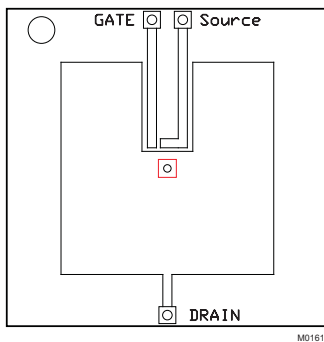
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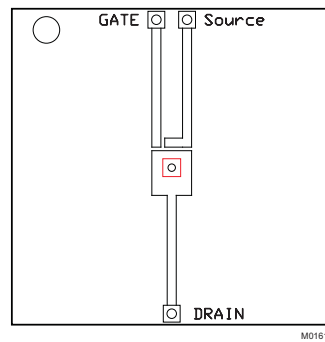
5.2 Thermal Information

THERMAL METRIC ⁽¹⁾⁽²⁾		CSD16340Q3	UNITS
		Q3 (8 PINS)	
θ_{JA}	Junction-to-Ambient Thermal Resistance	42.0	°C/W
θ_{JcTop}	Junction-to-Case (top) Thermal Resistance	20.6	
θ_{JB}	Junction-to-Board Thermal Resistance	8.8	
ψ_{JT}	Junction-to-Top Characterization Parameter	0.3	
ψ_{JB}	Junction-to-Board Characterization Parameter	8.7	
θ_{Jcbot}	Junction-to-Case (bottom) Thermal Resistance	0.1	

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).
- (2) For thermal estimates of this device based on PCB copper area, see the [TI PCB Thermal Calculator](#).



Max $R_{\theta JA}$ = 58°C/W
when mounted on
1 inch² of 2 oz. Cu.



Max $R_{\theta JA}$ = 162°C/W
when mounted on
minimum pad area of
2 oz. Cu.

5.3 Typical MOSFET Characteristics

($T_A = 25^\circ\text{C}$ unless otherwise stated)

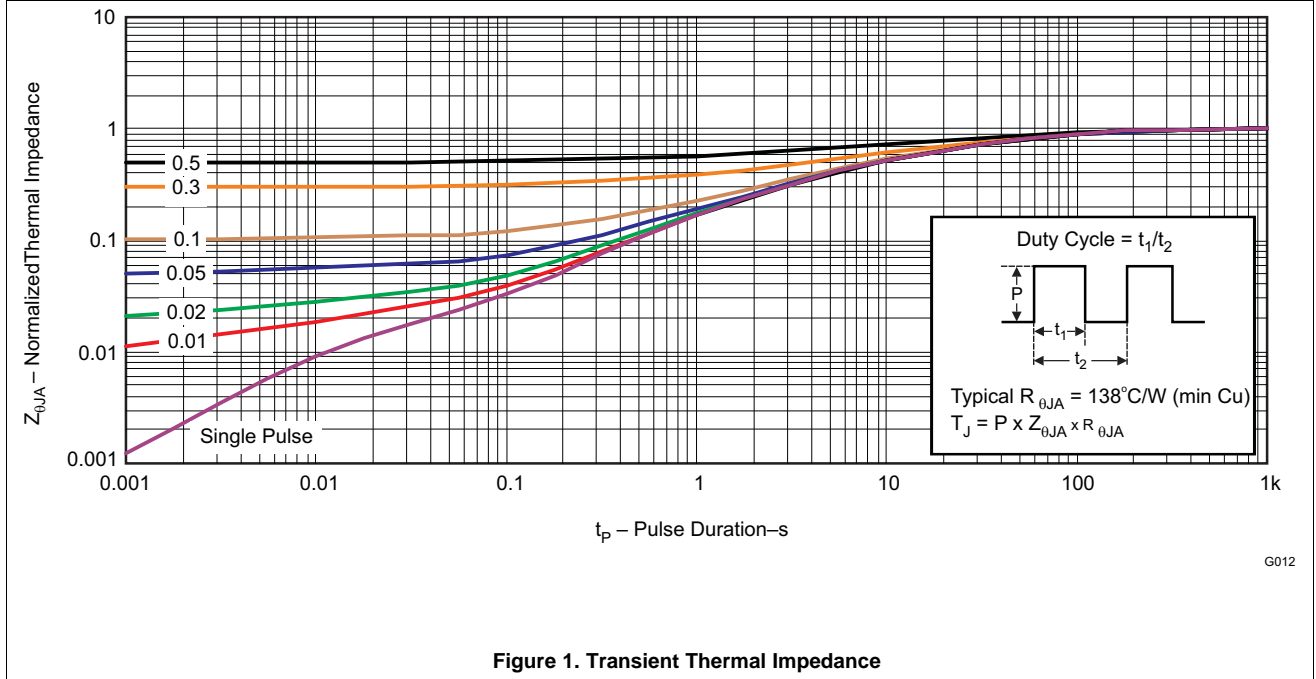


Figure 1. Transient Thermal Impedance

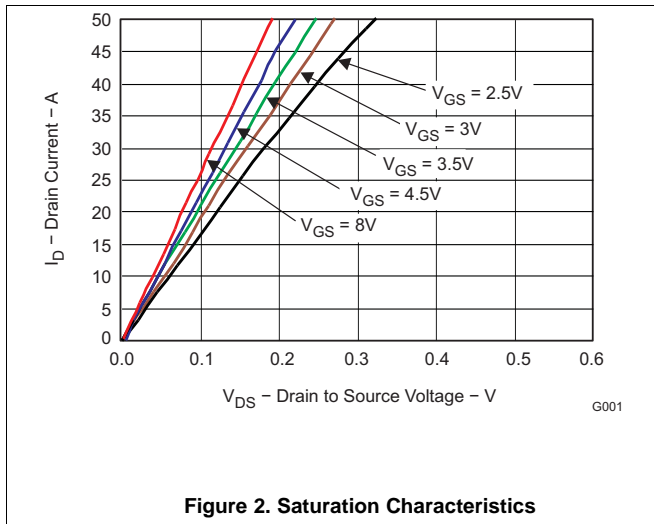


Figure 2. Saturation Characteristics

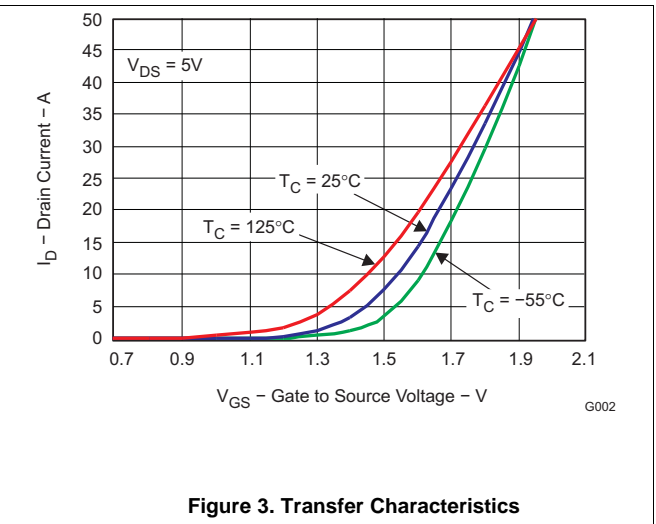


Figure 3. Transfer Characteristics

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Typical MOSFET Characteristics (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)

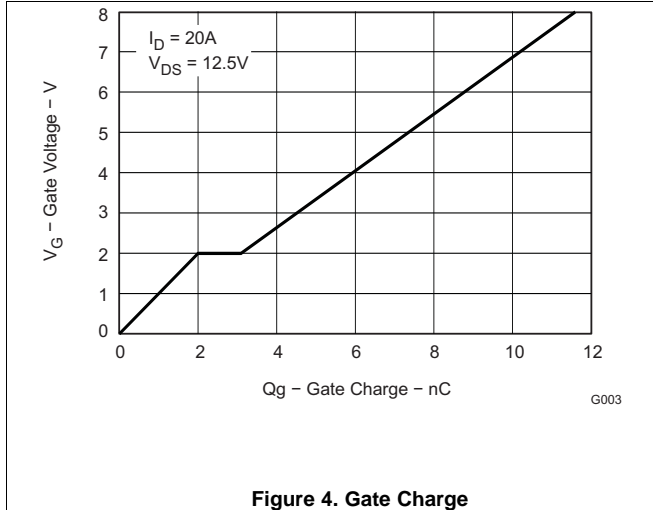


Figure 4. Gate Charge

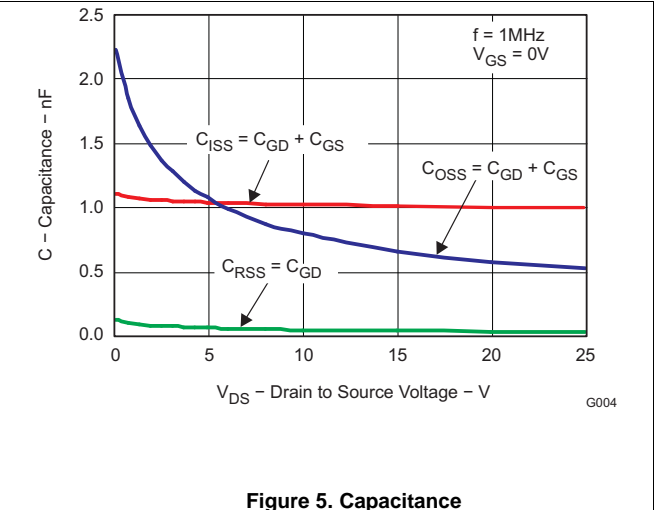


Figure 5. Capacitance

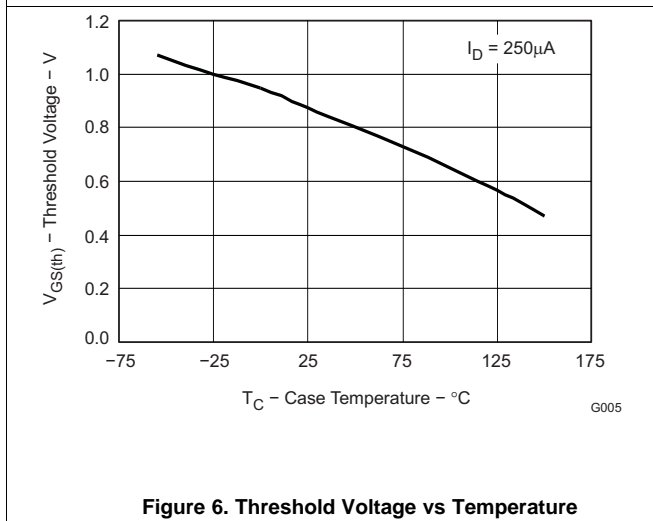


Figure 6. Threshold Voltage vs Temperature

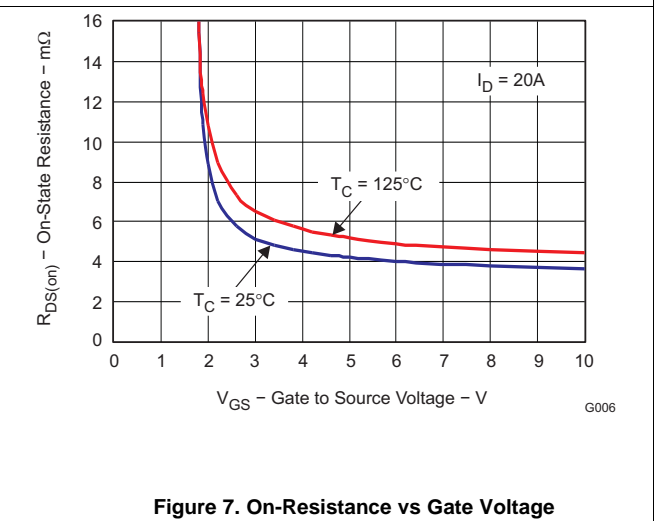


Figure 7. On-Resistance vs Gate Voltage

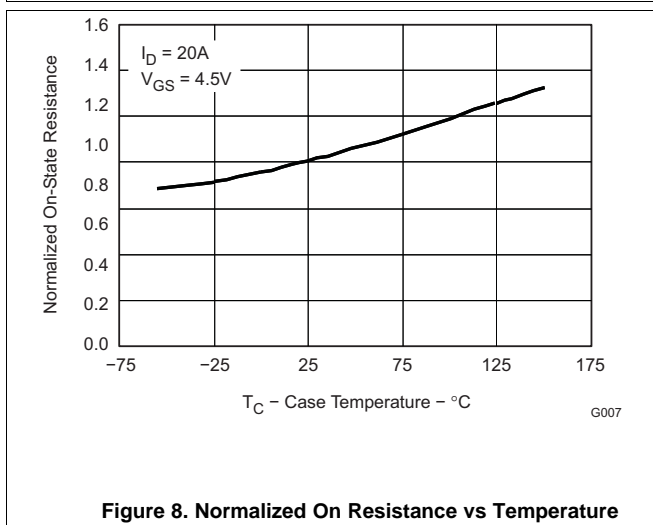


Figure 8. Normalized On Resistance vs Temperature

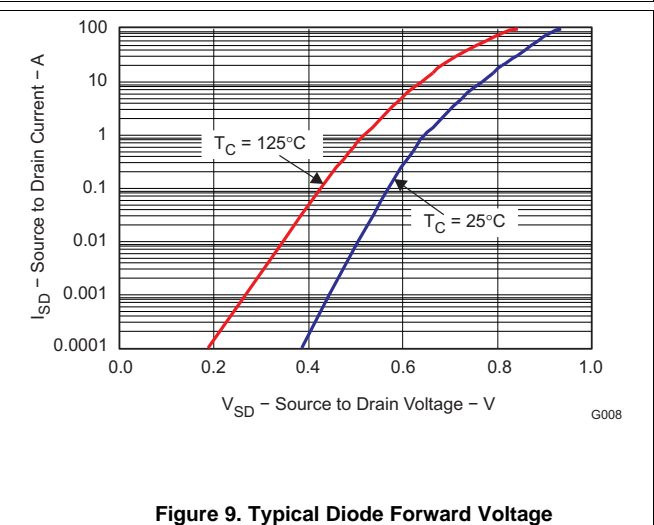


Figure 9. Typical Diode Forward Voltage

Typical MOSFET Characteristics (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)

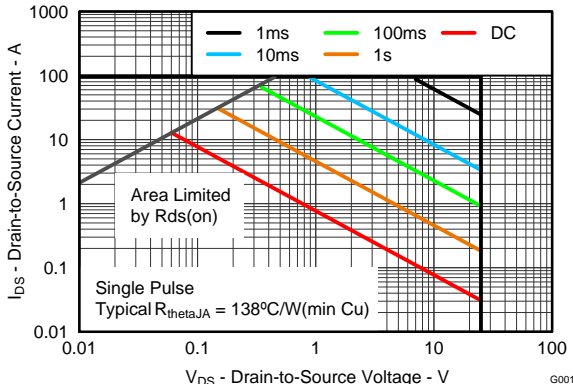


Figure 10. Maximum Safe Operating Area

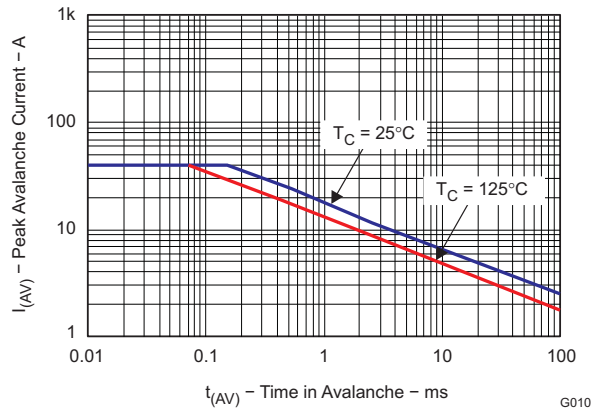


Figure 11. Single Pulse Unclamped Inductive Switching

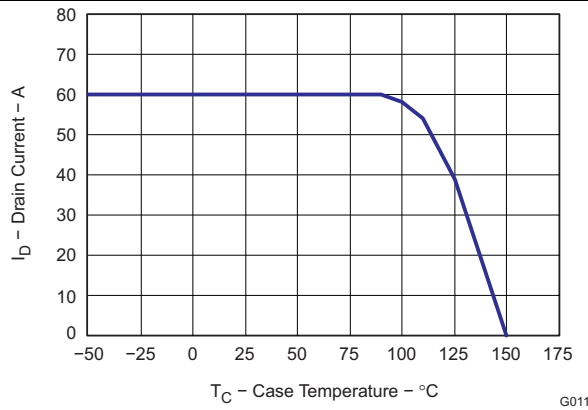


Figure 12. Maximum Drain Current vs Temperature

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6 Device and Documentation Support

6.1 Trademarks

NexFET is a trademark of Texas Instruments.

6.2 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

6.3 Glossary

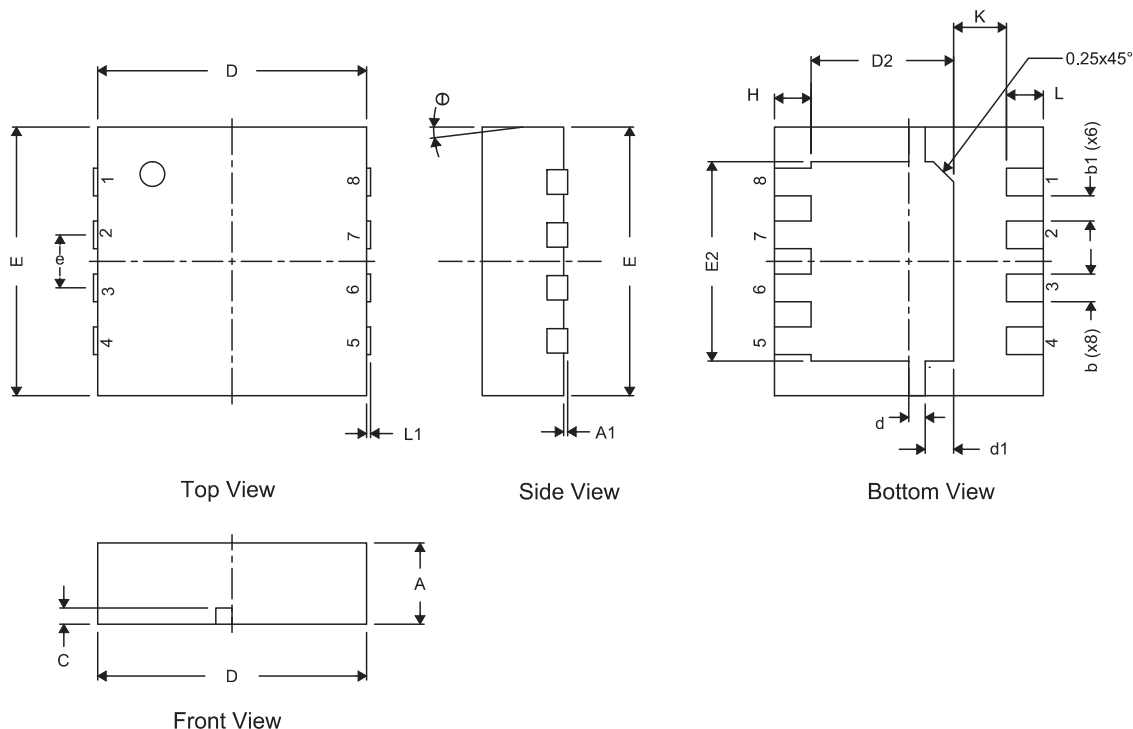
[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

7.1 Q3 Package Dimensions



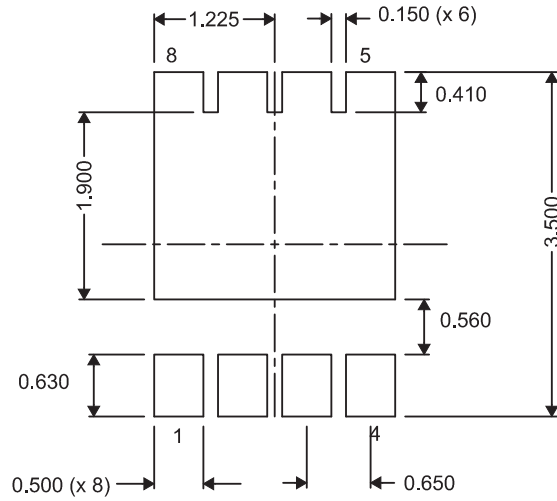
DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.950	1.000	1.100	0.037	0.039	0.043
A1	0.000	0.000	0.050	0.000	0.000	0.002
b	0.280	0.340	0.400	0.011	0.013	0.016
b1	0.310 NOM			0.012 NOM		
c	0.150	0.200	0.250	0.006	0.008	0.010
D	3.200	3.300	3.400	0.126	0.130	0.134
D2	1.650	1.750	1.800	0.065	0.069	0.071
d	0.150	0.200	0.250	0.006	0.008	0.010
d1	0.300	0.350	0.400	0.012	0.014	0.016
E	3.200	3.300	3.400	0.126	0.130	0.134
E2	2.350	2.450	2.550	0.093	0.096	0.100
e	0.650 TYP			0.026		
H	0.35	0.450	0.550	0.014	0.018	0.022
K	0.650 TYP			0.026 TYP		
L	0.35	0.450	0.550	0.014	0.018	0.022
L1	0	—	0	0	—	0
θ	0	—	0	0	—	0

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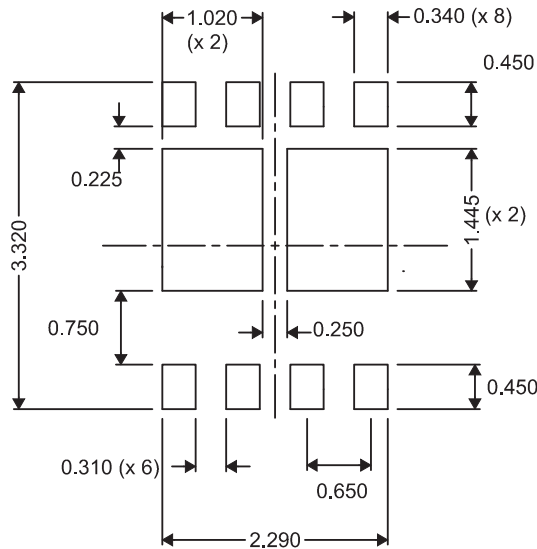
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7.2 Recommended PCB Pattern



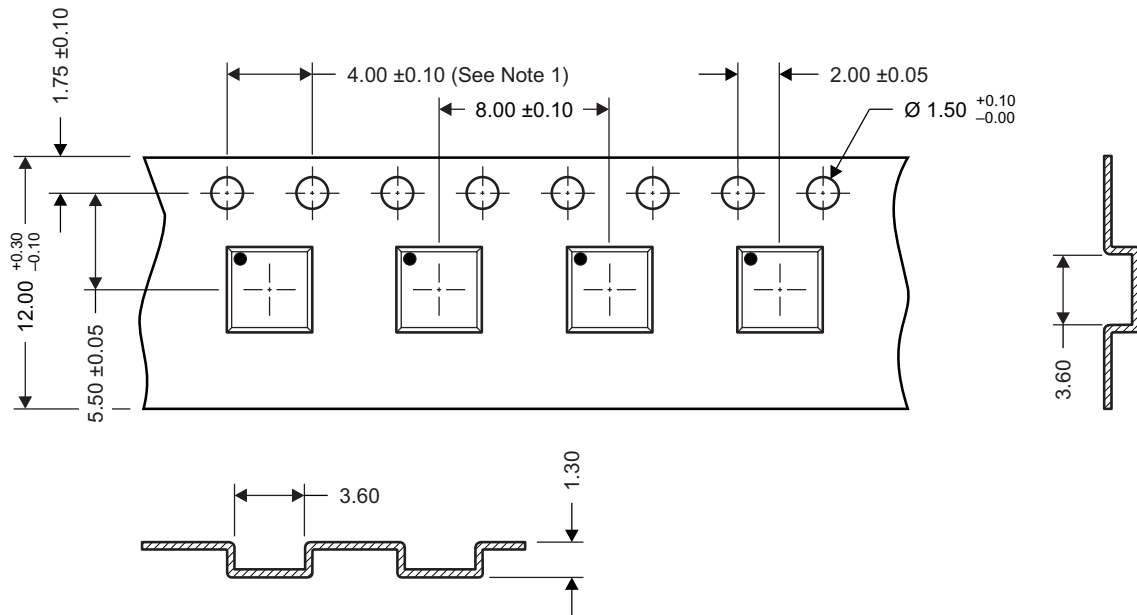
For recommended circuit layout for PCB designs, see application note [SLPA005](#) – *Reducing Ringing Through PCB Layout Techniques*.

7.3 Recommended Stencil Opening



All dimensions are in mm, unless otherwise specified.

7.4 Q3 Tape and Reel Information





M0144-01

Notes:

1. 10 sprocket hole pitch cumulative tolerance ± 0.2
2. Camber not to exceed 1 mm in 100 mm, noncumulative over 250 mm
3. Material: black static dissipative polystyrene
4. All dimensions are in mm (unless otherwise specified).
5. Thickness: 0.30 ± 0.05 mm
6. MSL1 260°C (IR and Convection) PbF-Reflow Compatible

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD16340Q3	ACTIVE	VSON-CLIP	DQG	8	2500	Pb-Free (RoHS Exempt)	CU SN	Level-1-260C-UNLIM	-55 to 150	CSD16340	
CSD16340Q3T	ACTIVE	VSON-CLIP	DQG	8	250	Pb-Free (RoHS Exempt)	CU SN	Level-1-260C-UNLIM	-55 to 150	CSD16340	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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PACKAGE OPTION ADDENDUM



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