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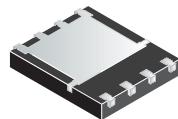
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[CSD17306Q5A](#)

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30V, N-Channel NexFET™ Power MOSFETs

Check for Samples: [CSD17306Q5A](#)

FEATURES

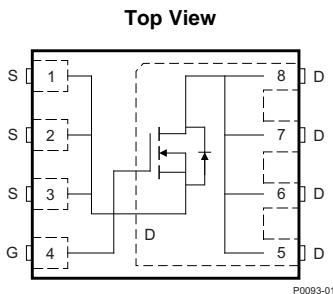
- Optimized for 5V Gate Drive
- Ultralow Q_g and Q_{gd}
- Low Thermal Resistance
- Avalanche Rated
- Pb Free Terminal Plating
- RoHS Compliant
- Halogen Free
- SON 5-mm x 6-mm Plastic Package

APPLICATIONS

- Notebook Point of Load
- Point-of-Load Synchronous Buck in Networking, Telecom and Computing Systems

DESCRIPTION

The NexFET™ power MOSFET has been designed to minimize losses in power conversion applications, and optimized for 5V gate drive applications.



P0093-01

PRODUCT SUMMARY

V_{DS}	Drain to Source Voltage	30	V
Q_g	Gate Charge Total (4.5V)	11.8	nC
Q_{gd}	Gate Charge Gate to Drain	2.4	nC
$R_{DS(on)}$	Drain to Source On Resistance	$V_{GS} = 3V$	4.2 mΩ
		$V_{GS} = 4.5V$	3.3 mΩ
		$V_{GS} = 8V$	2.9 mΩ
$V_{GS(th)}$	Threshold Voltage	1.1	V

ORDERING INFORMATION

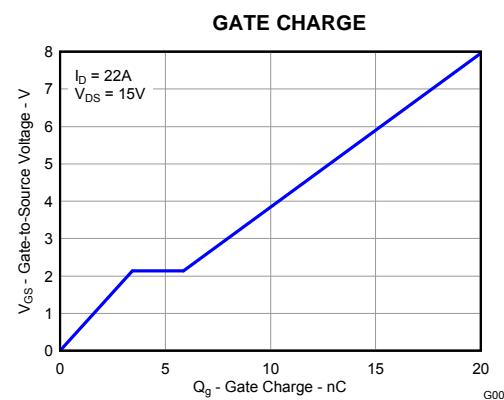
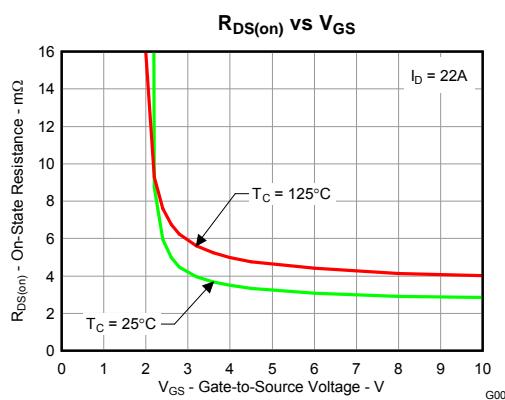
Device	Package	Media	Qty	Ship
CSD17306Q5A	SON 5-mm x 6-mm Plastic Package	13-Inch Reel	2500	Tape and Reel

ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ C$ unless otherwise stated	VALUE	UNIT
V_{DS} Drain to Source Voltage	30	V
V_{GS} Gate to Source Voltage	+10 / -8	V
I_D Continuous Drain Current, $T_C = 25^\circ C$	100	A
I_D Continuous Drain Current ⁽¹⁾	24	A
I_{DM} Pulsed Drain Current, $T_A = 25^\circ C$ ⁽²⁾	155	A
P_D Power Dissipation ⁽¹⁾	3.2	W
T_J, T_{STG} Operating Junction and Storage Temperature Range	-55 to 150	°C
E_{AS} Avalanche Energy, Single Pulse $I_D = 74A, L = 0.1mH, R_G = 25\Omega$	274	mJ

(1) Typical $R_{QJA} = 39^\circ C/W$ on a 1-inch² (6.45-cm²), 2-oz. (0.071-mm thick) Cu pad on a 0.06-inch (1.52-mm) thick FR4 PCB.

(2) Pulse duration $\leq 300\mu s$, duty cycle $\leq 2\%$



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CSD17306Q5A

SLPS253A – FEBRUARY 2010 – REVISED JULY 2010

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ELECTRICAL CHARACTERISTICS

 ($T_A = 25^\circ\text{C}$ unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Static Characteristics						
BV_{DSS}	Drain to Source Voltage	$V_{\text{GS}} = 0\text{V}$, $I_{\text{D}} = 250\mu\text{A}$		30		V
I_{DSS}	Drain to Source Leakage Current	$V_{\text{GS}} = 0\text{V}$, $V_{\text{DS}} = 24\text{V}$		1		μA
I_{GSS}	Gate to Source Leakage Current	$V_{\text{DS}} = 0\text{V}$, $V_{\text{GS}} = +10 / -8\text{V}$		100		nA
$V_{\text{GS}(\text{th})}$	Gate to Source Threshold Voltage	$V_{\text{DS}} = V_{\text{GS}}$, $I_{\text{D}} = 250\mu\text{A}$	0.9	1.1	1.6	V
$R_{\text{DS}(\text{on})}$	Drain to Source On Resistance	$V_{\text{GS}} = 3\text{V}$, $I_{\text{D}} = 22\text{A}$		4.2	5.4	$\text{m}\Omega$
		$V_{\text{GS}} = 4.5\text{V}$, $I_{\text{D}} = 22\text{A}$		3.3	4.2	$\text{m}\Omega$
		$V_{\text{GS}} = 8\text{V}$, $I_{\text{D}} = 22\text{A}$		2.9	3.7	$\text{m}\Omega$
g_{fs}	Transconductance	$V_{\text{DS}} = 15\text{V}$, $I_{\text{D}} = 22\text{A}$		105		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{\text{GS}} = 0\text{V}$, $V_{\text{DS}} = 15\text{V}$, $f = 1\text{MHz}$		1670	2170	pF
C_{oss}	Output Capacitance			890	1160	pF
C_{rss}	Reverse Transfer Capacitance			56	73	pF
R_{G}	Series Gate Resistance			1	2	Ω
Q_{g}	Gate Charge Total (4.5V)	$V_{\text{DS}} = 15\text{V}$, $I_{\text{D}} = 22\text{A}$		11.8	15.3	nC
Q_{gd}	Gate Charge Gate to Drain			2.4		nC
Q_{gs}	Gate Charge Gate to Source			3.5		nC
$Q_{\text{g}(\text{th})}$	Gate Charge at V_{th}			1.8		nC
Q_{oss}	Output Charge	$V_{\text{DS}} = 13.4\text{V}$, $V_{\text{GS}} = 0\text{V}$		23		nC
$t_{\text{d}(\text{on})}$	Turn On Delay Time	$V_{\text{DS}} = 15\text{V}$, $V_{\text{GS}} = 4.5\text{V}$, $I_{\text{DS}} = 22\text{A}$, $R_{\text{G}} = 2\Omega$		7.8		ns
t_{r}	Rise Time			13.1		ns
$t_{\text{d}(\text{off})}$	Turn Off Delay Time			18.4		ns
t_{f}	Fall Time			6.4		ns
Diode Characteristics						
V_{SD}	Diode Forward Voltage	$I_{\text{DS}} = 22\text{A}$, $V_{\text{GS}} = 0\text{V}$		0.85	1	V
Q_{rr}	Reverse Recovery Charge	$V_{\text{DD}} = 14\text{V}$, $I_{\text{F}} = 25\text{A}$, $\text{di/dt} = 300\text{A}/\mu\text{s}$		27		nC
t_{rr}	Reverse Recovery Time			25		ns

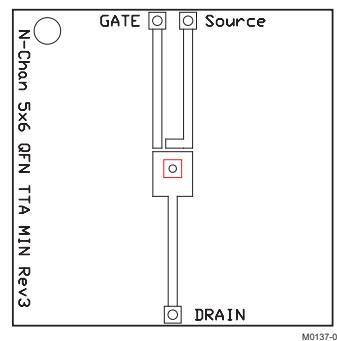
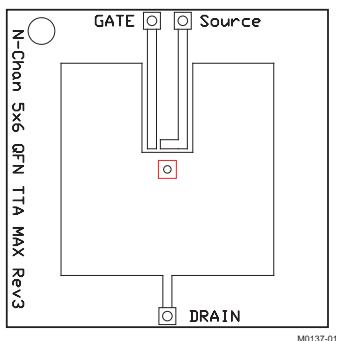
THERMAL CHARACTERISTICS

 ($T_A = 25^\circ\text{C}$ unless otherwise stated)

PARAMETER		MIN	TYP	MAX	UNIT
R_{0JC}	Thermal Resistance Junction to Case ⁽¹⁾			0.9	$^\circ\text{C}/\text{W}$
R_{0JA}	Thermal Resistance Junction to Ambient ⁽¹⁾⁽²⁾			49	$^\circ\text{C}/\text{W}$

 (1) R_{0JC} is determined with the device mounted on a 1-inch² (6.45-cm²), 2-oz. (0.071-mm thick) Cu pad on a 1.5-inch \times 1.5-inch (3.81-cm \times 3.81-cm), 0.06-inch (1.52-mm) thick FR4 PCB. R_{0JC} is specified by design, whereas R_{0JA} is determined by the user's board design.

 (2) Device mounted on FR4 material with 1-inch² (6.45-cm²), 2-oz. (0.071-mm thick) Cu.



TYPICAL MOSFET CHARACTERISTICS

($T_A = 25^{\circ}\text{C}$ unless otherwise stated)

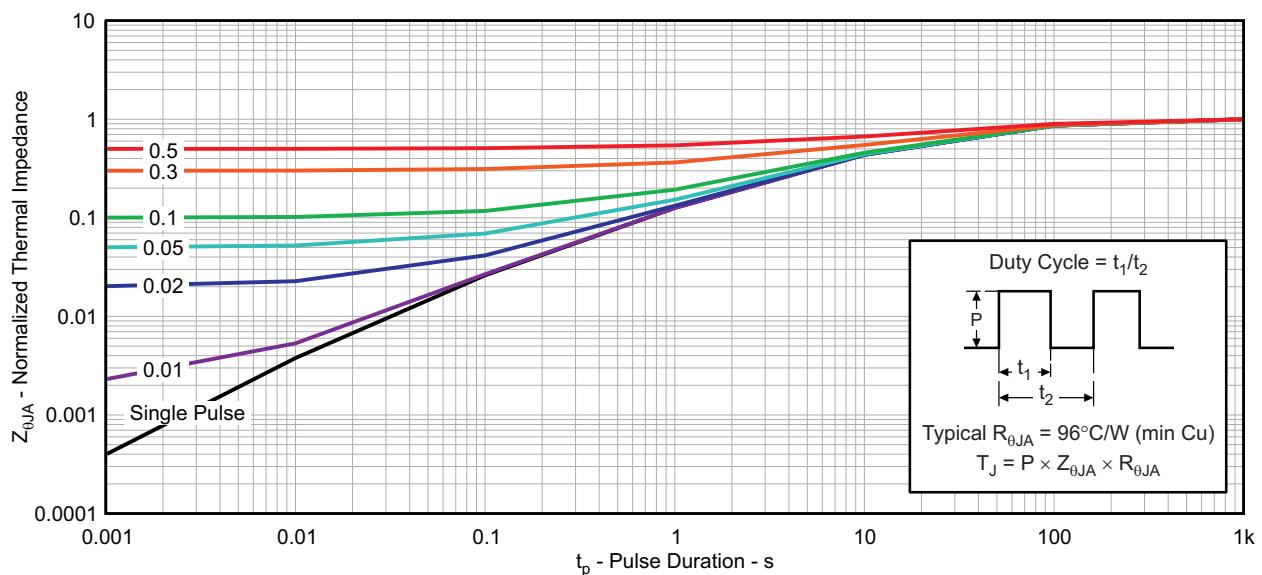


Figure 1. Transient Thermal Impedance

TYPICAL MOSFET CHARACTERISTICS (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)

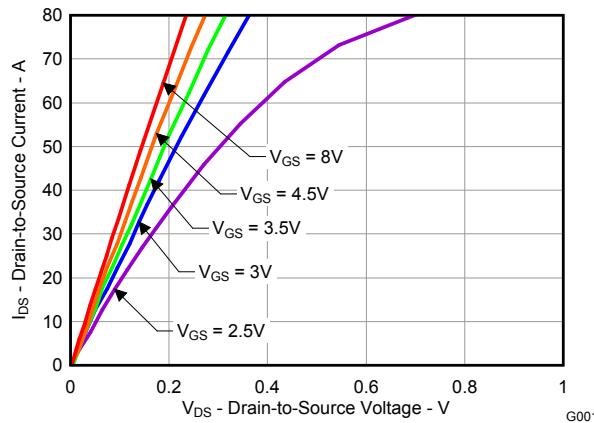


Figure 2. Saturation Characteristics

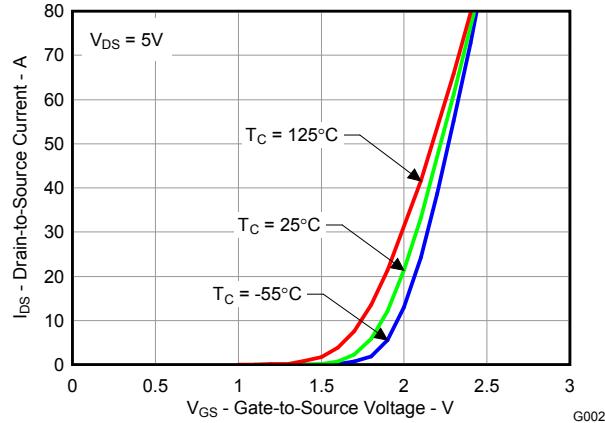


Figure 3. Transfer Characteristics

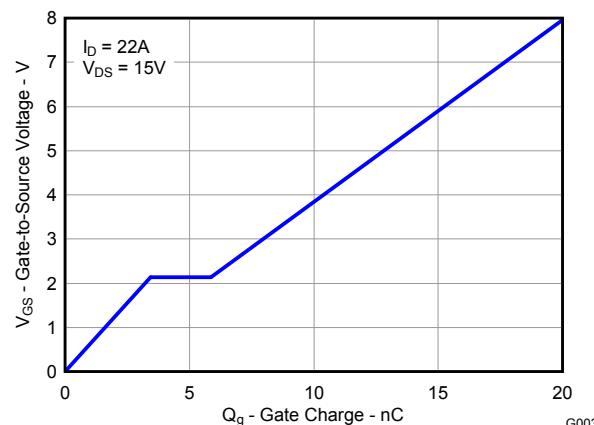


Figure 4. Gate Charge

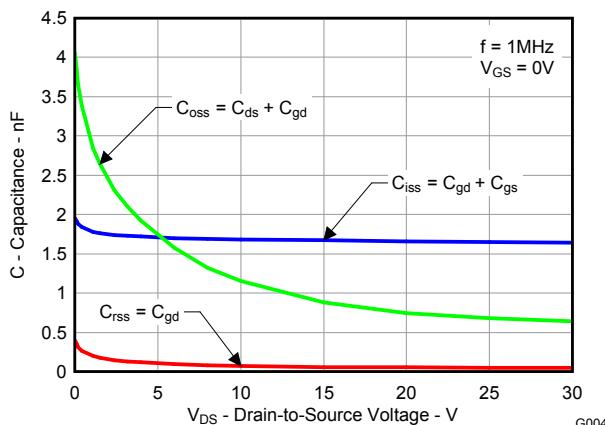


Figure 5. Capacitance

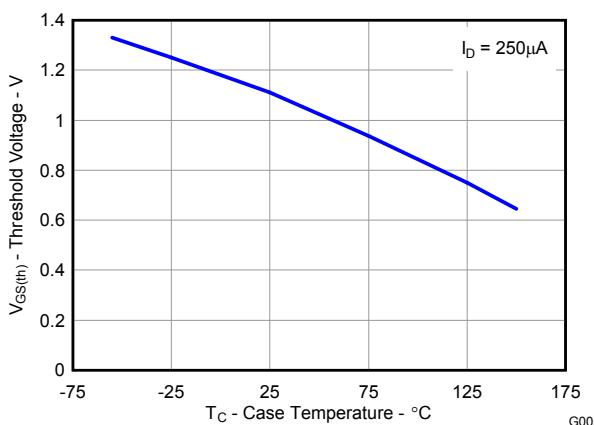


Figure 6. Threshold Voltage vs. Temperature

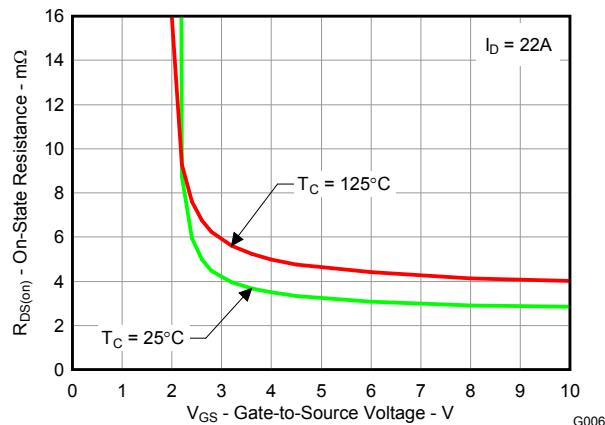


Figure 7. On-State Resistance vs. Gate-to-Source Voltage

TYPICAL MOSFET CHARACTERISTICS (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)

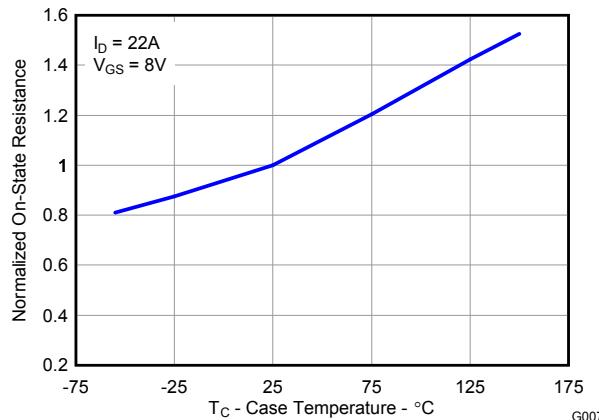


Figure 8. Normalized On-State Resistance vs. Temperature

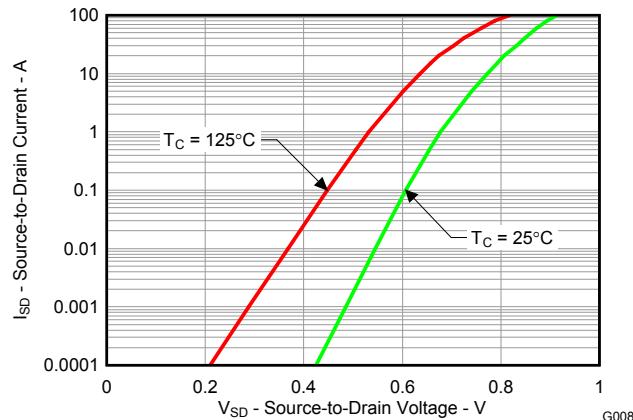


Figure 9. Typical Diode Forward Voltage

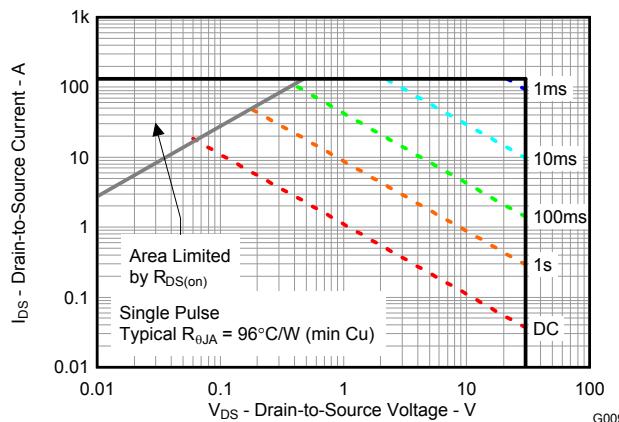


Figure 10. Maximum Safe Operating Area

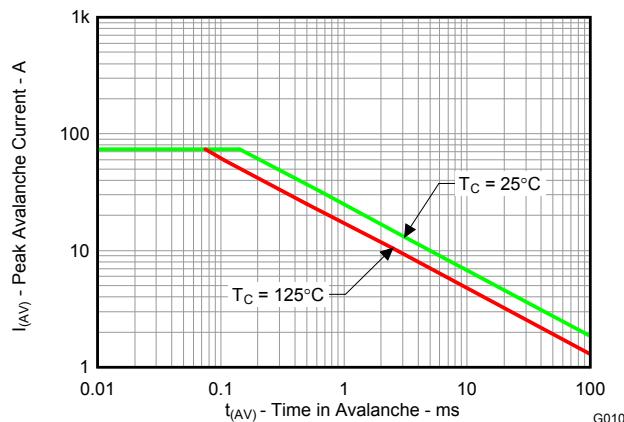


Figure 11. Single Pulse Unclamped Inductive Switching

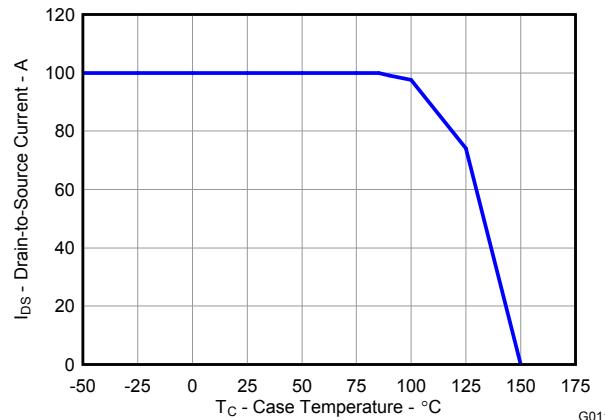
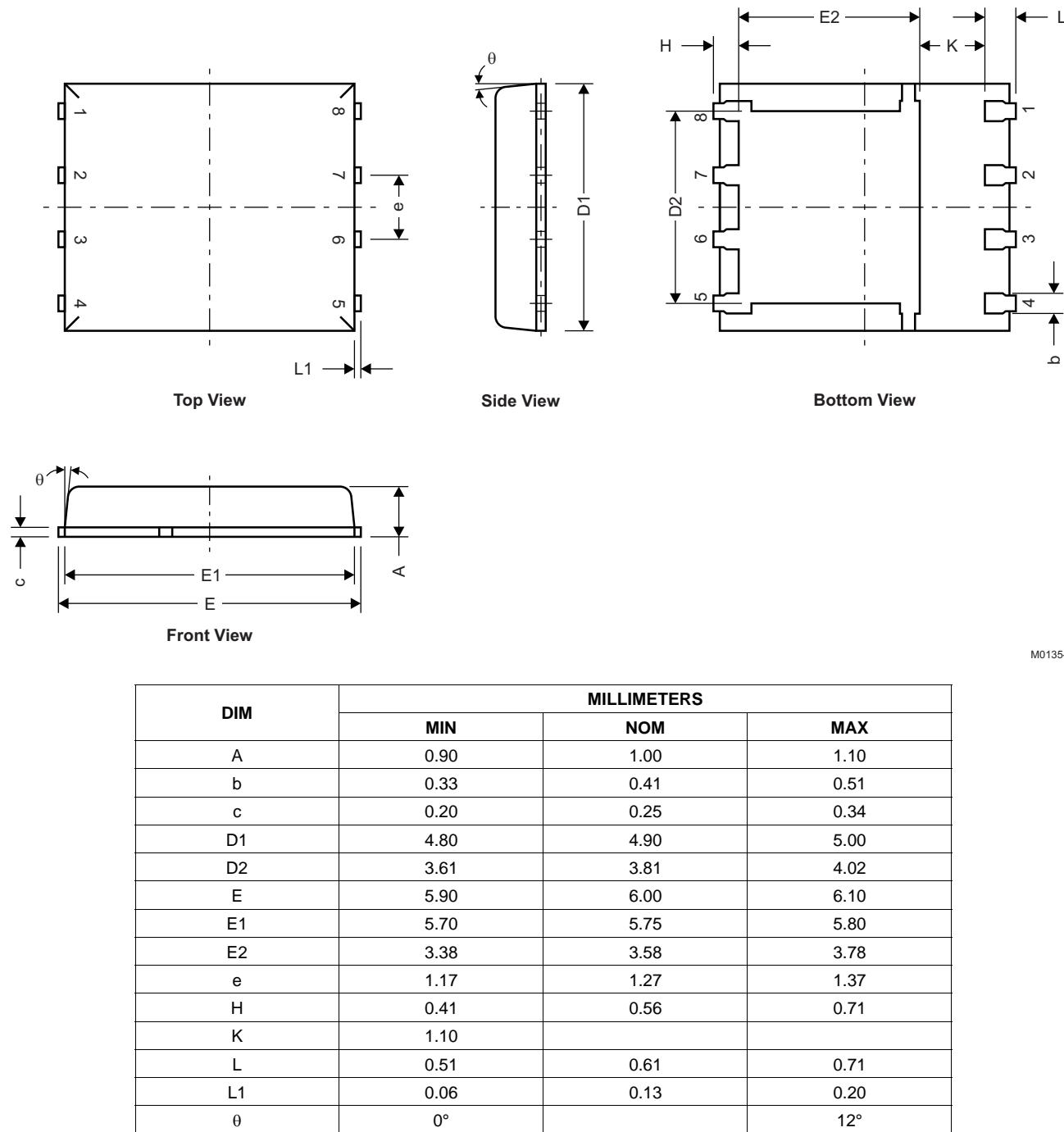


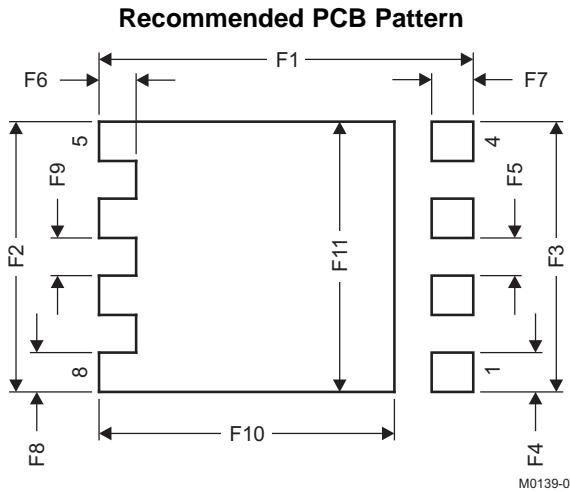
Figure 12. Maximum Drain Current vs. Temperature

MECHANICAL DATA

Q5A Package Dimensions



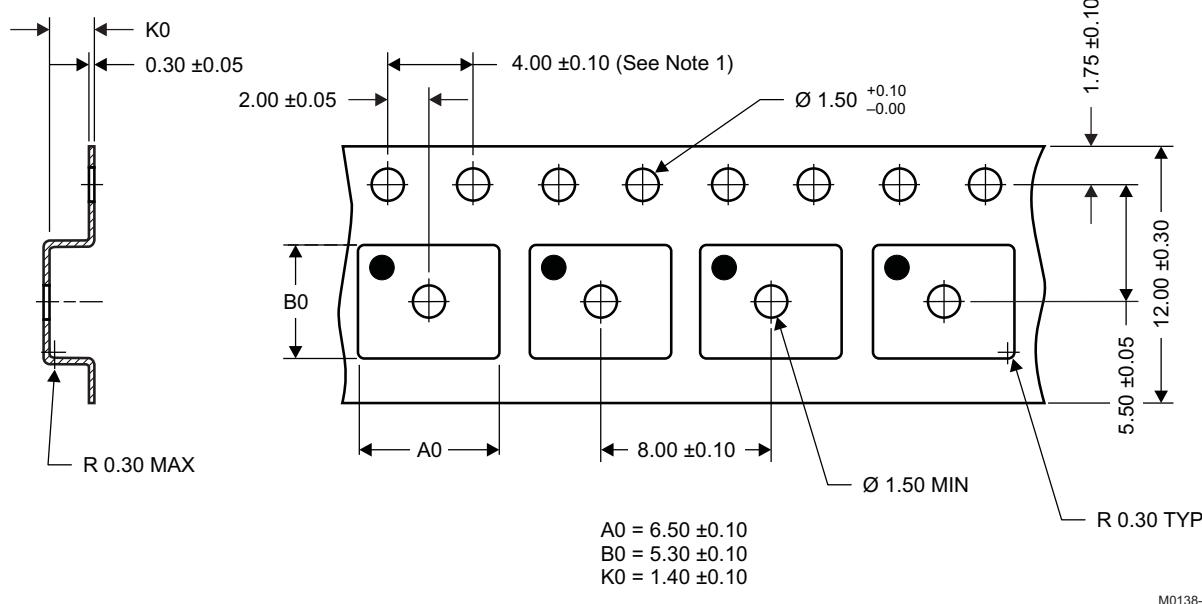
M0135-01



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
F1	6.205	6.305	0.244	0.248
F2	4.46	4.56	0.176	0.18
F3	4.46	4.56	0.176	0.18
F4	0.65	0.7	0.026	0.028
F5	0.62	0.67	0.024	0.026
F6	0.63	0.68	0.025	0.027
F7	0.7	0.8	0.028	0.031
F8	0.65	0.7	0.026	0.028
F9	0.62	0.67	0.024	0.026
F10	4.9	5	0.193	0.197
F11	4.46	4.56	0.176	0.18

For recommended circuit layout for PCB designs, see application note [SLPA005 – Reducing Ringing Through PCB Layout Techniques](#).

Q5A Tape and Reel Information



Notes:

1. 10-sprocket hole-pitch cumulative tolerance ± 0.2
2. Camber not to exceed 1mm in 100mm, noncumulative over 250mm
3. Material: black static-dissipative polystyrene
4. All dimensions are in mm (unless otherwise specified)
5. A0 and B0 measured on a plane 0.3mm above the bottom of the pocket

REVISION HISTORY

Changes from Original (February 2010) to Revision A	Page
• Updated the Q5A Package Dimensions table. DIM c MAX was 0.30, DIM D2 MAX was 3.96, DIM e MIN was blank MAX was blank, DIM H NOM was 0.51 MAX was 0.61	6
• Deleted Note 6 from the Q5A Tape and Reel Information - "MSL1 260°C (IR and convection) PbF reflow compatible"	7
• Deleted the Package Marking Information section	7

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD17306Q5A	ACTIVE	VSONP	DQJ	8	2500	Pb-Free (RoHS Exempt)	CU SN	Level-1-260C-UNLIM	-55 to 150	CSD17306	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.**OBSOLETE:** TI has discontinued the production of the device.(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.**TBD:** The Pb-Free/Green conversion plan has not been defined.**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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