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CY2VC521ZXC-2T

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CY2VC521-2

Low Noise LVDS Clock Generator with VCXO

Features

- Output: 216 MHz Output Clock
- Input: External 27 MHz Crystal
- Differential LVDS Output with 2x Drive to Drive Two Loads
- VCXO gives 230 ppm Minimum Pull Range
- Low RMS Phase Jitter (12 kHz–20 MHz): 1.3 ps Typical
- Low Phase Noise
- Fully Integrated Low Noise Phase Locked Loop (PLL)
- Excellent Voltage-to-Frequency Linearity
- Supply Voltage: 3.3V
- Pb-free 16-Pin TSSOP Package

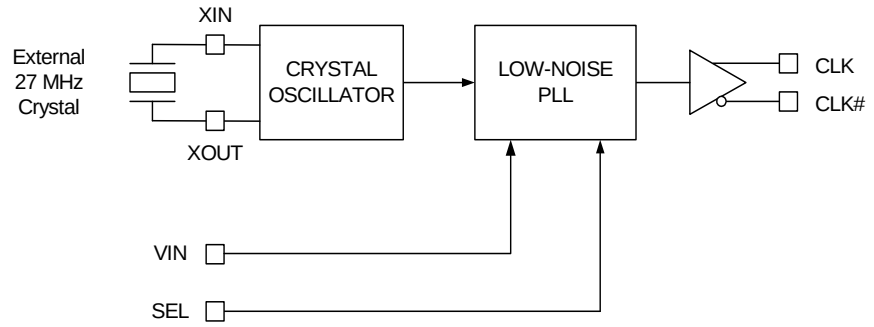
Description

The CY2VC521-2 is a PLL-based clock generator with VCXO control and very low output jitter. When the user connects a fundamental mode 27 MHz crystal, this device generates a 216 MHz output clock. The CY2VC521-2 has one LVDS output pair tuned to drive two standard LVDS loads and operates from a single 3.3V power supply.

The VIN pin is an analog input that enables the user to pull the output frequency. The pullability range is at least 230 ppm (±115 ppm).

Unlike conventional VCXO designs, the output frequency adjustment is not achieved by adjusting capacitance at the pins of the crystal. Instead, a proprietary PLL design is used. This permits the use of a standard 27 MHz crystal. A special “pullable” crystal is neither required nore recommended.

Logic Block Diagram



Pinout

Figure 1. Pin Diagram - 16-Pin TSSOP

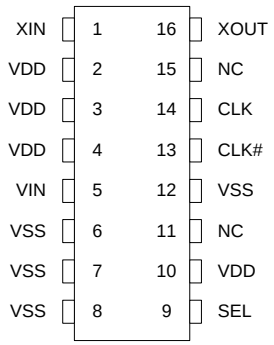


Table 1. Pin Definitions - 16-Pin TSSOP

Pin	Name	Type	Description
1	XIN	Crystal	Oscillator Input: Connect a 27 MHz crystal between XIN and XOUT
16	XOUT	Crystal	Oscillator Output: Connect a 27 MHz crystal between XIN and XOUT
5	VIN	Analog Input	VCXO Control Voltage: VIN has a positive control slope, meaning that increasing the voltage on VIN causes the output frequency to increase. The nominal output frequency is determined when VIN = 1.65V
13, 14	CLK#, CLK	LVDS Output	Differential output clock
9	SEL	CMOS Input	Select: Hold this pin LOW for normal operation
11, 15	NC	–	No Connect: NC pins are not connected to the die
2, 3, 4, 10	VDD	–	3.3V power supply
6, 7, 8, 12	VSS	–	Ground

Frequency Table

Inputs		Output Frequency (MHz)
Xtal Frequency (MHz)	PLL Multiplier Value	
27	8	216

VCXO and VIN

The output frequency of the device is adjusted over a limited range by use of the VCXO feature. This feature is typically used to phase and frequency lock to a separate reference clock. The frequency is controlled by the analog voltage on the VIN pin. The nominal output frequency is generated when VIN = 1.65V. As the voltage on VIN is increased, the output frequency increases. The voltage range for VIN is from 0V (V_{SS}) to V_{DD}.

Application Information

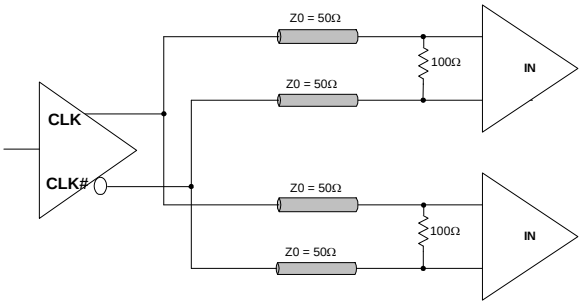
Power Supply Filtering Techniques

As in any high speed analog circuitry, noise on the power supply pins degrade device performance. For general power plane decoupling, make certain there is at least one tantalum capacitor (~5 to 10 µF) in the general vicinity of this device. Additionally, ensure one or two multi-layer ceramic chip capacitors (0.01 or 0.1 µF) is located as close as possible to the power and ground pins of the device. Make certain to optimize the layout to minimize power and ground inductance and to locate the capacitor as close to the device pins as possible.

Termination for LVDS Output

Use a 100Ω terminating resistor to terminate CLK and CLK# with two parallel differential traces split near the driver; connect the resistors between each pair near the receiver. This is shown in the following figure.

Figure 2. LVDS Output Termination



Crystal Input Interface

The CY2VC521-2 is designed for use with a 14 pF parallel resonant crystal. This assumes 2 pF of board capacitance on each crystal signal traces, plus 26 pF internally on both the XIN and XOUT pins. The crystal is required to meet the parameters shown in "Crystal Characteristics" on page 4. Because the frequency pulling function is implemented inside the PLL, there are no additional requirements placed on the crystal for pullability.

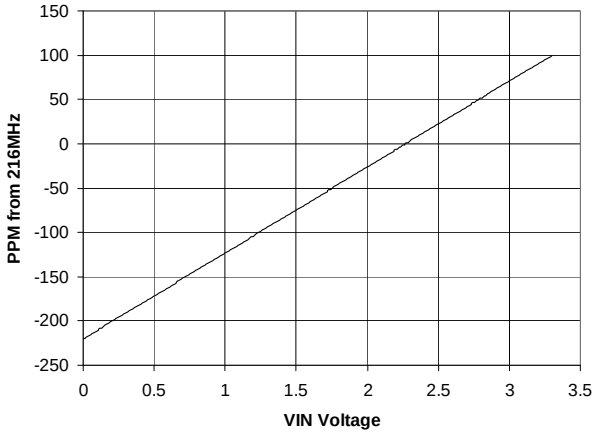
The design may require external trimming capacitors if the crystal has C_L greater than 14 pF, depending on the layout.

VIN Control

Figure 3 shows a typical VCXO control curve for the CY2VC521-2. The conditions are 25°C, V_{DD}=3.3V, crystal C_L=13 pF, and board capacitance on XIN and XOUT traces of 3.5 pF each. Note that the internal capacitance measured on the XIN and XOUT pins is approximately 26 pF.

In this case the curve is not centered (0 ppm at VIN=V_{DD}/2) because the capacitive loading on the crystal is too high, which causes it to oscillate slower than its nominal frequency. When the crystal is capacitively loaded as specified (C_L), it oscillates at its specified frequency, and the VCXO control curve is nominally centered. Such changes in the crystal oscillation frequency result in a vertical shift of the curve. The slope and linearity of the curve are independent of the crystal characteristics.

Figure 3. Typical VCXO Control Curve



Absolute Maximum Conditions

Parameter	Description	Condition	Min	Max	Unit
V_{DD}	Supply Voltage		–0.5	4.4	V
V_{IN}[1]	Input Voltage, DC	Relative to V_{SS}	–0.5	V_{DD}+0.5	V
T_S	Temperature, Storage	Non Operating	–65	150	°C
T_J	Temperature, Junction		–	135	°C
ESD_{HBM}	ESD Protection (Human Body Model)	JEDEC STD 22-A114-B	2000	–	V
UL–94	Flammability Rating	At 1/8 in.	V–0		
Θ_{JA}[5]	Thermal Resistance, Junction to Ambient	0 m/s airflow	84		°C/W
		1 m/s airflow	79		
		2.5 m/s airflow	76		

Operating Conditions

Parameter	Description	Min	Typ	Max	Unit
V_{DD}	Supply Voltage Range	3.15	3.3	3.45	V
T_{PU}	Power up time for V_{DD} to reach V_{DD}(min). (Ensure power ramp is monotonic.)	0.05	–	500	ms
T_A	Ambient Temperature	0	–	70	°C

Crystal Characteristics

Parameter	Description	Min	Typ	Max	Unit
	Mode of Oscillation		Fundamental		
F	Frequency	–	27	–	MHz
C_L	Load Capacitance	–	14	–	pF
ESR	Equivalent Series Resistance	–	–	50	Ω
C_S	Shunt Capacitance	–	–	7	pF

DC Electrical Characteristics

Parameter	Description	Condition	Min	Typ	Max	Unit
I_{DD}[3]	Power Supply Current	Outputs on and terminated	–	–	120	mA
V_{OD}	LVDS Differential Output Voltage		247	350	454	mV
ΔV_{OD}	LVDS V_{OD} Magnitude Change		–50	–	50	mV
V_{OS}	LVDS Offset Output Voltage		1.125	1.25	1.375	mV
ΔV_{OS}	LVDS V_{OS} Magnitude Change		–25	–	25	mV
V_{IH}	Input High Voltage, SEL		0.7*V_{DD}	–	–	V
V_{IL}	Input Low Voltage, SEL		–	–	0.3*V_{DD}	V
I_{IH}	Input High Current, SEL	SEL = V_{DD}	–	–	10	µA
I_{IL}	Input Low Current, SEL	SEL = V_{SS}	–	–	20	µA
C_{IN}[5]	Input Capacitance, SEL		–	4	–	pF
V_{VIN}	VIN Input Voltage		0	–	V_{DD}	V
I_{VIN}	VIN Input Current	$V_{SS} \le VIN \le V_{DD}$	–10	–	60	µA
INL_{VIN}[4, 5]	VIN to F_{OUT} Integral Nonlinearity	$V_{SS} \le VIN \le V_{DD}$	–	1	–	%

Notes
1. The voltage on any input or output pin cannot exceed the power pin during power up.
2. Simulated using Apache Sentinel TI software. The board is derived from the JEDEC multilayer standard. It measures 76 x 114 x 1.6 mm and has 4-layers of copper (2/1/1/2 oz.). The internal layers are 100% copper planes, while the top and bottom layers have 50% metalization. No vias are included in the model
3. I_{DD} includes ~8 mA of current that is dissipated externally in the output termination resistors.
4. Not 100% tested, guaranteed by design and characterization.
5. Integral nonlinearity is defined in IEEE Standard 1241-2000.

AC Electrical Characteristics[4, 6]

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
F_{OUT}	Output Frequency		–	216	–	MHz
PR	Pull Range	VIN = V_{DD} to V_{SS}, relative to frequency at VIN = 1.65V, across operating temperature and voltage range	±115	–	–	ppm
T_R, T_F[7]	Output Rise and Fall Times	20% and 80% of swing between steady state levels	–	–	0.5	ns
T_J	Period Jitter, RMS		–	7	–	ps
$T_{Jitter(\phi)}$	RMS Phase Jitter (Random)	216 MHz carrier, integrated 12 kHz–20 MHz	–	1.3	–	ps
PN	Phase Noise	1 kHz offset from 216 MHz carrier	–	–95	–	dBc/Hz
		10 kHz offset from 216 MHz carrier	–	–120	–	dBc/Hz
		100 kHz offset from 216 MHz carrier	–	–127	–	dBc/Hz
		1 MHz offset from 216 MHz carrier	–	–123	–	dBc/Hz
		10 MHz offset from 216 MHz carrier	–	–130	–	dBc/Hz
T_{DC}[8]	Duty Cycle	Measured at zero crossing point	45	50	55	%
T_{LOCK}	Start-up Time	Time for CLK to reach valid frequency measured from the time V_{DD} = V_{DD} (min.)	–	–	5	ms

Notes
6. Outputs are terminated with 50Ω between CLK and CLK#. Refer to Figure 2 on page 3.
7. Refer to Figure 6 on page 6.
8. Refer to Figure 7 on page 6.

Parameter Measurements

Figure 4. Output Voltage Swing

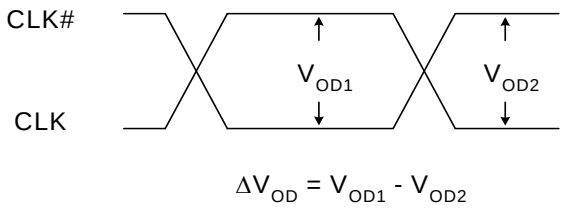


Figure 5. Output Offset Voltage

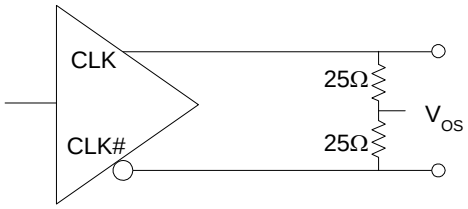


Figure 6. Output Rise and Fall Time

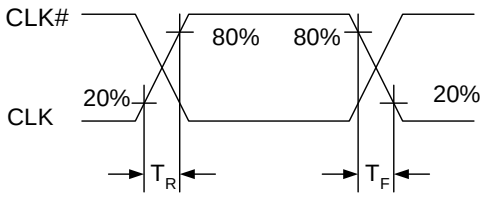
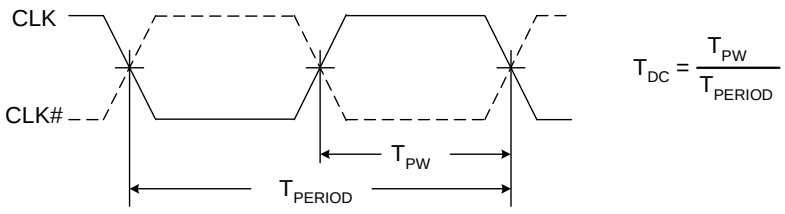


Figure 7. Output Duty Cycle/Pulse Width/Period

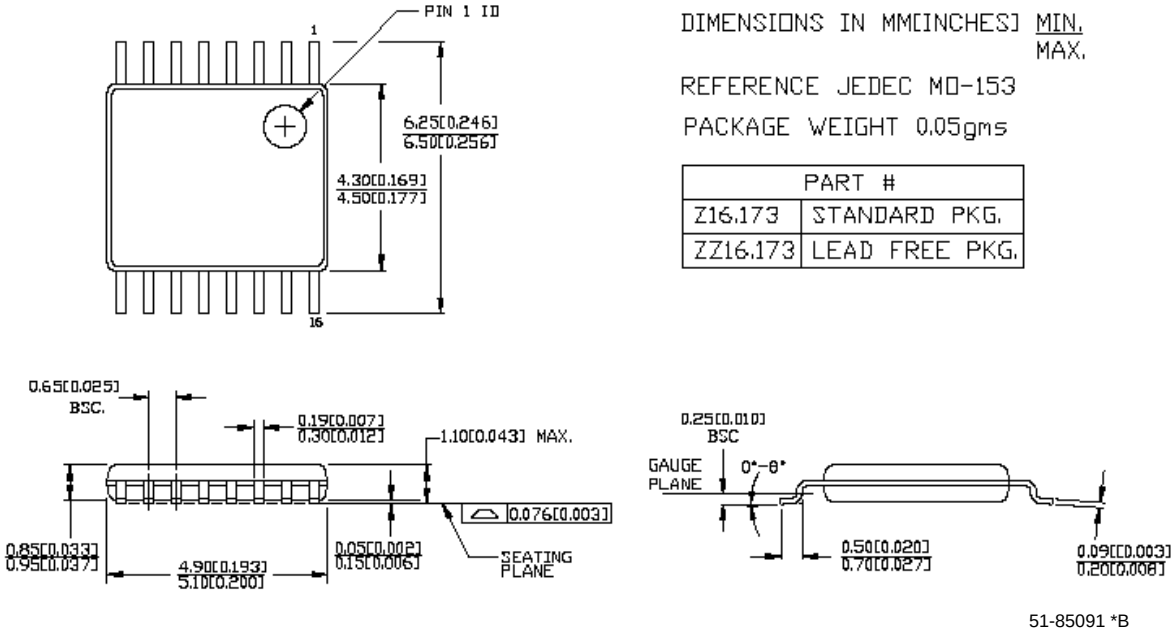


Ordering Information

Part Number	Package Description	Product Flow
Pb-Free		
CY2VC521ZXC-2	16-Pin TSSOP	Commercial, 0° to 70°C
CY2VC521ZXC-2T	16-Pin TSSOP - Tape and Reel	Commercial, 0° to 70°C

Package Drawings and Dimensions

Figure 8. 16-Pin TSSOP 4.40 MM Body



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Document History Page

Document Title: CY2VC521-2 Low Noise LVDS Clock Generator with VCXO Document Number: 001-15599				
REV.	**ECN NO.**	**Submission Date**	**Orig. of Change**	**Description of Change**
**	1285703	See ECN	JWK/ARI	New datasheet Created from 001-06436 Edited data sheet for template compliance
*A	2669117	3/5/2009	KVM/AESA	Removed MSL spec IIL changed from 100 µA to 20 µA Changed phase noise values Replaced jitter with phase jitter in Features list Changes to VOD specs Change I_{IVIN} max from 50uA to 60uA; added min value Changed junction temp from 125°C to 135°C Changed Data Sheet Status to Final
*B	2697706	04/20/2009	KVM/PYRS	Added VCXO Control Curve figure and text
*C	2705609	05/15/2009	KVM/AESA	Corrected part numbers in Ordering Information table Added phase jitter spec to AC Electrical table, and added conditions to the phase jitter claim in the features section of page 1 Formatting improvements Corrected conditions for ESD
*D	2768029	09/18/2009	KVM	Change parameter name I_{IVIN} to I_{VIN} Change parameter LIN to INL_{VIN}, add note to definition INL_{VIN} & C_{IN} reference note: not 100% tested Change T_{LOCK} max from 10 ms to 5 ms Change part number CY2VC521ZXCT-2 to CY2VC521ZXC-2T
*E	2905106	05/14/10	KVM	Updated package diagram.

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