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NCP1581DR2G

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NCP1581

High Frequency Synchronous Step Down PWM Controller for Tracking Applications

The NCP1581 controller IC is designed to provide a simple synchronous buck regulator for on−board DC to DC applications in a 14−pin SOIC. The NCP1581 is designed specifically for tracking applications by providing the track input.

The NCP1581 operates at a fixed internal 400 kHz switching frequency allowing the use of small external components. The device features a programmable soft start set by an external capacitor, under−voltage lockout and output under−voltage detection that latches off the device when an output short is detected.

Features

- Power up Sequencing / Tracking
- Enable Input
- Internal 400 kHz Oscillator
- Programmable Soft−Start
- Fixed Frequency Voltage Mode
- Voltage Mode Adaptive Deadtime
- This is a Pb−Free Device

Applications

- Tracking Applications
- Game Consoles
- Computing Peripheral Voltage Regulators
- Graphics Cards
- General DC to DC Converters

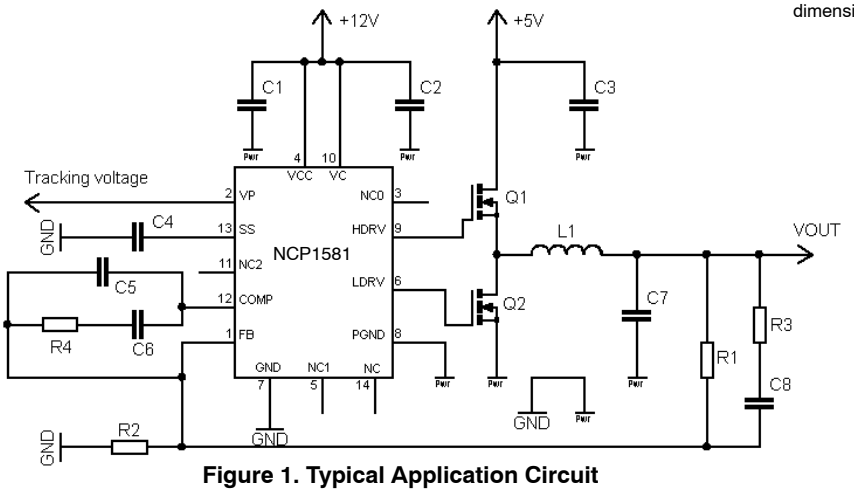

Figure 1. Typical Application Circuit

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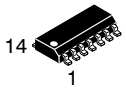
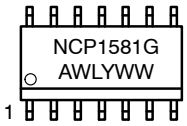


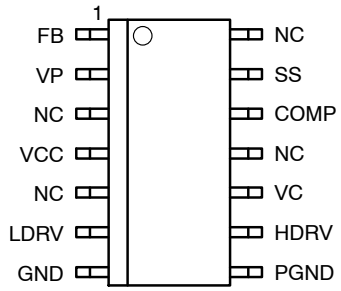
SOIC−14
D SUFFIX
CASE 751A

MARKING DIAGRAM



A	= Assembly Location
WL	= Wafer Lot
Y	= Year
WW	= Work Week
G	= Pb−Free Package

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 13 of this data sheet.

Circuit Description:

Block Diagram

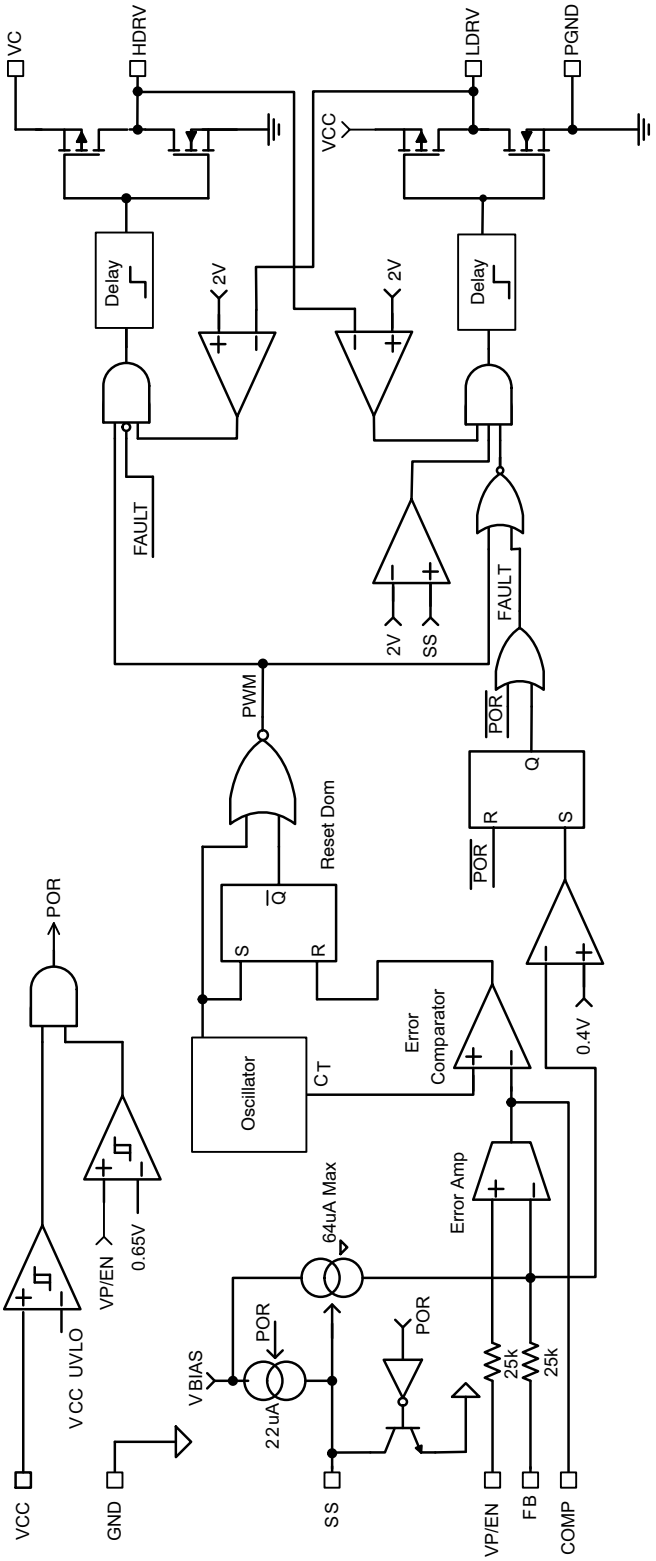


Figure 2. Simplified Block Diagram

Table 1. PIN FUNCTION DESCRIPTION

Pin	Name	Description
1	FB	Inverting input to the error amplifier. This pin is connected to the output of the regulator via resistor divider to set the output voltage and provide feedback to the error amplifier.
2	VP/EN	Dual function pin. Non inverting input to the error amplifier. Enable input.
3	NC	No Connect
4	VCC	This pin provides power for the internal blocks of the IC as well as powers the low side driver. A minimum of 0.1 μF, high frequency capacitor must be connected from this pin to power ground.
5	NC	No Connect
6	LDRV	Output driver for low side MOSFET.
7	GND	IC ground for internal control circuitry.
8	PGND	Power Ground. This pin serves as a separate ground for the MOSFET drivers and should be connected to the system's power ground plane.
9	HDRV	Output driver for high side MOSFET. The negative voltage at this pin may cause instability for the gate drive circuit. To prevent this, a low forward voltage drop diode (e.g. BAT54 or 1N4148) is required between this pin and Power Ground.
10	VC	This pin powers the high side driver.
11	NC	No Connect
12	COMP	Output of error amplifier. An external resistor and capacitor network is typically connected from this pin to ground to provide loop compensation.
13	SS	Soft start. This pin provides user programmable soft−start function. Connect an external capacitor from this pin to ground to set the start up time of the output voltage.
14	NC	No Connect

Table 2. ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	min	max	Unit
Main Supply Voltage Input	V_{CC}	−0.3	20	V
Main Supply Voltage Input 200 ns wide spikes, 400 kHz	V_{CC_SPK}	−0.3	22	V
Supply Voltage for the High side driver	V_C	−0.3	20	V
Supply Voltage for the High side driver 200 ns wide spikes, 400 kHz	V_{C_SPK}	−0.3	22	V
VP/EN pin Voltage	$V_{P/EN}$	−0.3	10 or V_{CC} (Note 1)	V
FB pin Voltage	V_{FB}	−0.3	10 or V_{CC} (Note 1)	V
Rating	**Symbol**	**Value**		**Unit**
Thermal Resistance, Junction−to−Ambient (Note 2)	R_{thja}	90		K/W
Storage Temperature Range	T_{stg}	−65 to 150		°C
Junction Operating Temperature	T_J	0 to 150		°C
ESD Withstand Voltage (Note 3) Human Body Model Machine Model	V_{ESD}	 2.0 200		 kV V
Moisture Sensitivity Level	MSL	JEDEC Level 1 @ 260°C		

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

NOTE: All voltages are referenced to GND pin unless otherwise stated.

1. Maximum = 10 V or V_{CC}, whichever is lower.
2. JEDEC High−K model
3. This device series contains ESD protection and exceeds the following tests:
   Human Body Model (HBM) ±2.0 kV per JEDEC standard: JESD22−A114
   Machine Model (MM) ±200 V per JEDEC standard: JESD22−A115

Table 3. RECOMMENDED OPERATING CONDITIONS

Symbol	Definition	Min	Max	Units
V_{CC}	Supply Voltage	7	20	V
V_C	Supply Voltage	Converter Voltage + 5 V, (Note 4)	20	V
T_J	Junction Temperature	0	125	°C

NOTE: All voltages are referenced to GND pin.
4. Depend on high side MOSFET V_{GS}

Table 4. ELECTRICAL SPECIFICATIONS Unless otherwise specified, $V_{CC} = V_C = 12$ V, $0°C < T_J < 125°C$

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
SUPPLY CURRENT						
V_{CC} Supply Current (Static)	$I_{CC(Static)}$	$V_{P/EN} = 0$ V, No Switching		1.5	3	mA
V_{CC} Supply Current (Dynamic)	$I_{CC(Dynamic)}$	$f_{SW} = 400$ kHz, $C_L = 1.5$ nF		10	15	mA
V_C Supply Current (Static)	$I_{C(Static)}$	$V_{P/EN} = 0$ V, No Switching		0.05	0.1	mA
V_C Supply Current (Dynamic)	$I_{C(Dynamic)}$	$f_{SW} = 400$ kHz, $C_L = 1.5$ nF		9	15	mA
UNDER VOLTAGE LOCKOUT						
V_{CC}–Start–Threshold	V_{CC} UVLO (R)	Supply voltage Rising	6.3	6.6	7.0	V
V_{CC}–Stop–Threshold	V_{CC} UVLO (F)	Supply voltage Falling	6.0	6.3	6.6	V
V_{CC}–Hysteresis	V_{CC} (Hyst)	Supply ramping up and down	0.2	0.3	0.4	V
Enable–Start–Threshold	$V_{P/EN}$ UVLO (R)	Supply voltage Rising	0.6	0.65	0.7	V
Enable–Stop–Threshold	$V_{P/EN}$ UVLO (F)	Supply voltage Falling	0.56	0.6	0.66	V
Enable–Hysteresis	$V_{P/EN}$ (Hyst)	Supply ramping up and down		40		mV
FB UVLO	V_{FB} UVLO	FB ramping down	0.3	0.4	0.5	V
OSCILLATOR						
Frequency	f_{SW}		370	400	430	kHz
Ramp Amplitude	V_{RAMP}	(Note 5)		1.25		V
Min Duty Cycle	D_{MIN}	V_{FB} =1V, $V_{P/EN} = 0.8$ V			0	%
Max Duty Cycle	D_{MAX}	$f_{SW} = 400$ kHz, $V_{FB} = 0.6$ V, $V_{P/EN} = 0.8$ V	83	85	95	%
ERROR AMPLIFIER						
FB Input Bias Current	I_{FB1}	$V_{SS} = 3$ V		–0.1	–0.5	μA
FB Input Bias current	I_{FB2}	$V_{SS} = 0$ V		64		μA
VP/EN Input Bias Current	$I_{VP/EN}$	$V_{SS} = 3$ V		–0.1	–0.5	μA
Transconductance	gm		440		1300	μmho
Input Offset Voltage	V_{OS}	$V_{P/EN} = 0.8$ V, $V_{COMP} = 2.0$ V	–6	0	+6	mV
VP/EN Common Mode Range	V_{COMN}	(Note 5)	0.6		1.5	V
ERROR AMPLIFIER DESIGN SPECIFICATIONS						
OTA output current	$I_{OTA\ (SINK)}$	$V_{FB} = 1.2$ V, $V_{P/EN} = 1.0$ V, $V_{COMP} = 2.0$ V, (Note 5)		100		μA
OTA output current	$I_{OTA\ (SOURCE)}$	$V_{FB} = 0.8$ V, $V_{P/EN} = 1.0$ V, $V_{COMP} = 2.0$ V, (Note 5)		100		μA

5. Guaranteed by Design but not tested in production.

Table 5. ELECTRICAL SPECIFICATIONS Unless otherwise specified, V_{CC} = V_C = 12 V, 0°C < T_J < 125°C

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
SOFT START						
Soft Start Current	I_{SS}	V_{SS} = 0 V	12	22	32	μA
Soft Start Turn On	SS (on)		1.8	2	2.2	V
OUTPUT DRIVERS						
LO Drive Rise Time	tr(Lo)	C_L = 1.5 nF (See Figure 3)		20	50	ns
HI Drive Rise Time	tr(Hi)	C_L = 1.5 nF (See Figure 3)		30	60	ns
LO Drive Fall Time	tf(Lo)	C_L = 1.5 nF (See Figure 3)		20	50	ns
HI Drive Fall Time	tf(Hi)	C_L = 1.5 nF (See Figure 3)		30	60	ns
Dead Band Time	t_{DEAD}	(See Figure 3)	35	45	90	ns
Adaptive DBT Level	V_{ADT}			2.0		V

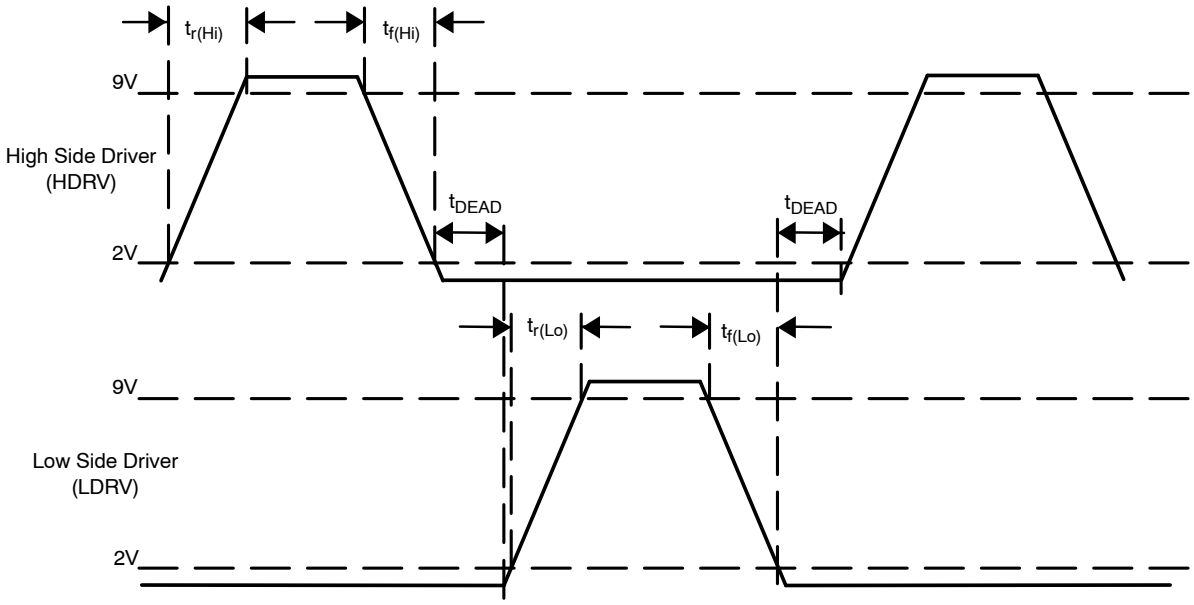


Figure 3. Definition of Rise/Fall Time and Deadband Time

TYPICAL CHARACTERISTICS

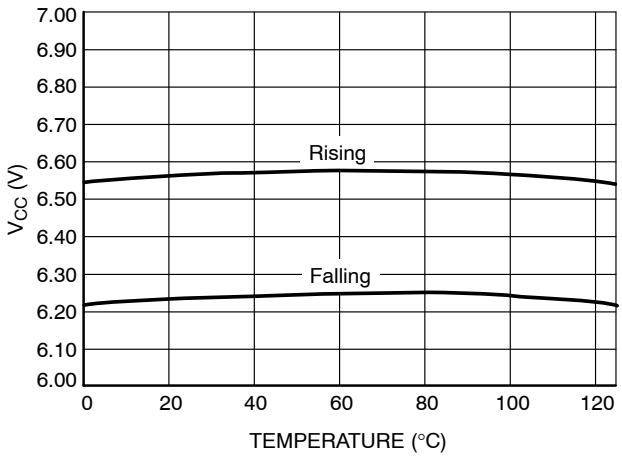


Figure 4. V_{CC} UVLO

TYPICAL CHARACTERISTICS

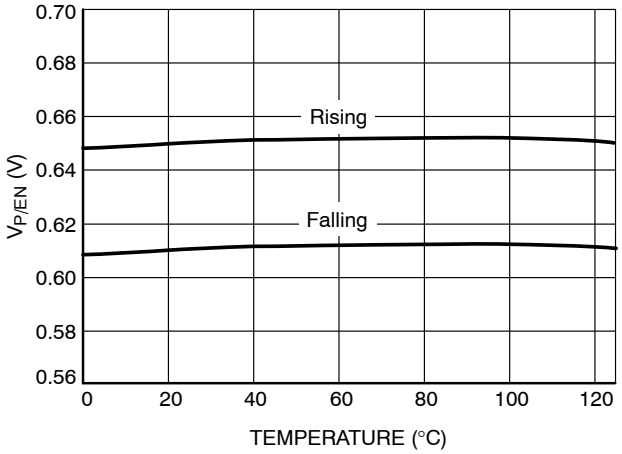


Figure 5. $V_{P/EN}$ UVLO

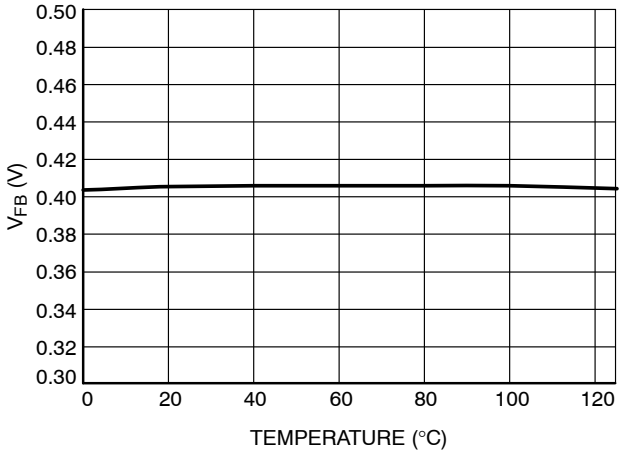


Figure 6. FB UVLO

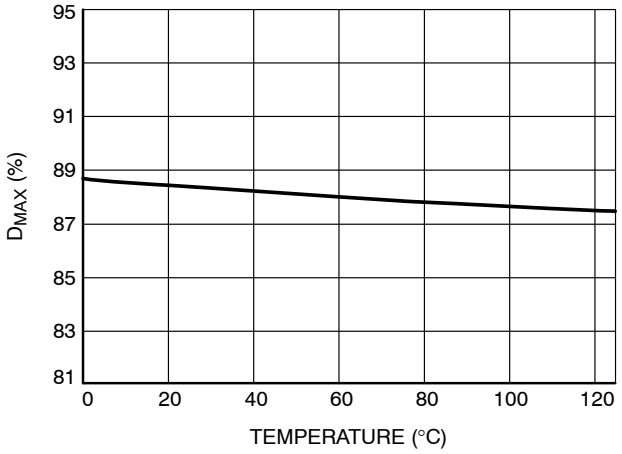


Figure 7. Maximum Duty Cycle

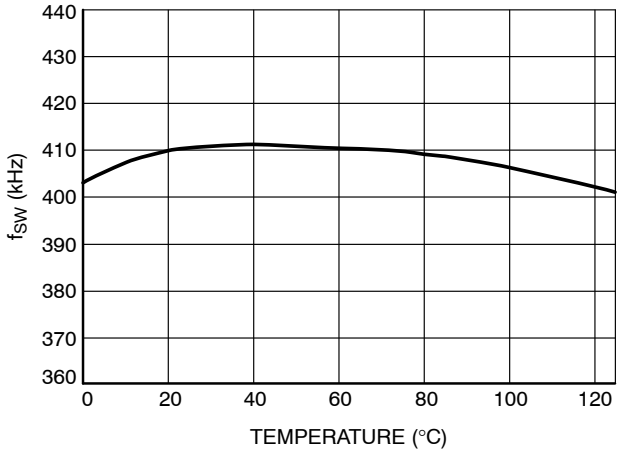


Figure 8. Switching Frequency

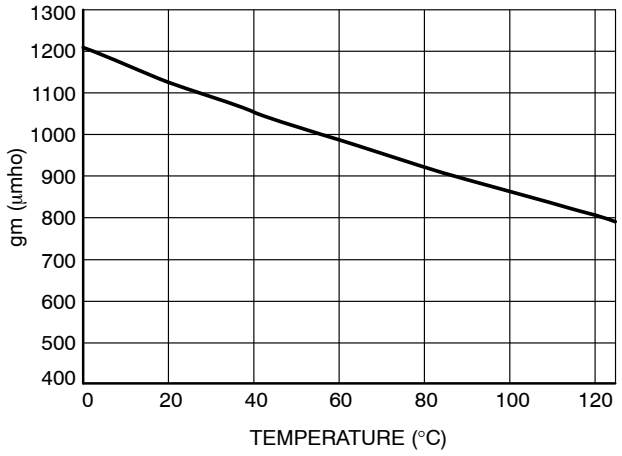


Figure 9. Error Amplifier Transconductance

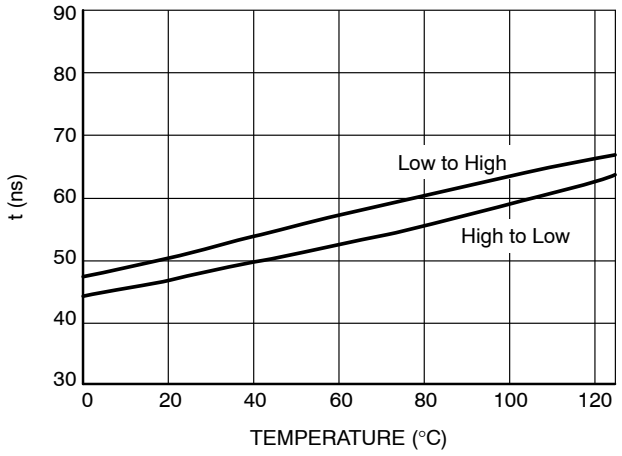


Figure 10. Deadtime

Detailed Description

Introduction

The NCP1581 is voltage mode PWM synchronous controller designated to drive two external N-channel MOSFETs. Switching frequency is fixed at 400 kHz. Output voltage is determined by feedback resistor divider and external reference voltage. Reference voltage input can be used to enabling and disabling operation and for tracking function.

Under-Voltage Lockout

The undervoltage lockout circuit ensures that the IC does not start and work until V_{CC} and $V_{P/EN}$ are over set thresholds. If these conditions are not fulfilled output drivers are in the off state.

Disable Function

The output voltage can be disabled by pulling the VP/EN pin below 0.6 V. At this time are output drivers in the off state.

Output Voltage

Output voltage can be set by an external resistor divider and external reference voltage at VP/EN pin according to Equation (1):

$$V_{OUT} = V_{P/EN} \cdot \left(1 + \frac{R1}{R2}\right) \quad \text{(eq. 1)}$$

where $V_{P/EN}$ is the external reference voltage at VP/EN pin that is connected to noninverting input of error amplifier. R1 and R2 resistors create voltage divider from output to FB pin that is connected to inverting input of error amplifier. Absolute values of resistors R1 and R2 depend on the compensation network type. See discussion of compensation description for details.

Inductor Selection

The inductor selection is based on the output power, frequency, input and output voltages, and efficiency requirements. High inductor values cause low current ripple, slower transient response, higher efficiency and increased size. Inductor design can be reduced to desired maximum current ripple in the inductor. It is good to have current ripple (ΔI_{Lmax}) between 20% and 50% of the output current.

For a buck converter, the inductor should be chosen according to Equation (2).

$$L = \left(\frac{V_{OUT}}{f_{SW} \cdot \Delta I_{Lmax}}\right)\left(1 - \frac{V_{OUT}}{V_{INmax}}\right) \quad \text{(eq. 2)}$$

Output Capacitor Selection

The output voltage ripple and transient requirements determine the output capacitor type and value. The important parameter for the selection of the output capacitor is equivalent serial resistance (ESR). If the capacitor has low ESR, it often has sufficient capacity for filtering as well as an adequate RMS current rating.

The value of the output capacitor should be calculated using the following equation:

$$C_{OUT} \geq \frac{\Delta I_L}{8 \cdot f_{SW} \cdot (\Delta V_{OUT} - \Delta I_L \cdot ESR)} \quad \text{(eq. 3)}$$

For a higher switching frequency, it is suitable to use a multilayer ceramic capacitor (MLCC) with very low ESR. The advantages are small size, low output voltage ripple and fast transient response. The disadvantage of the MLCC type is the requirement to use a Type III compensation network.

Input Capacitor Selection

The input capacitor is used to supply current pulses while the high side MOSFET is on. When the MOSFET is off, the input capacitor is being charged. The value of this capacitor can be selected with the Equation (4):

$$C_{IN} \geq \frac{I_{OUT} \cdot \frac{V_{OUT}}{V_{IN}} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}{f_{SW} \cdot \Delta V_{IN}} \quad \text{(eq. 4)}$$

where ΔV_{IN} is the input voltage ripple and the recommended value is about 2–5% of V_{IN}. The input capacitor must be able to handle the input ripple current. Its value should be calculated using Equation (5):

$$I_{RMS} = I_{OUT} \cdot \sqrt{\frac{V_{OUT} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}{V_{IN}}} \quad \text{(eq. 5)}$$

Power MOSFET Selection

The NCP1581 uses two N-channel MOSFETs. They can be primarily selected according to $R_{DS(ON)}$, maximum drain to source voltage, and gate charge. $R_{DS(ON)}$ impacts conductive losses and gate charge impacts switching losses. The low side MOSFET is selected primarily for conduction losses, and the high side MOSFET is selected to reduce switching losses especially when the output voltage is less than 30% of the input voltage. The drain to source breakdown voltage must be higher than the maximum input voltage. Conductive power losses can be calculated using the following Equations (6) and (7):

$$P_{COND-HIGHFET} = I_{OUT}^2 \cdot R_{DS(ON)} \cdot \frac{V_{OUT}}{V_{IN}} \quad \text{(eq. 6)}$$

$$P_{COND-LOWFET} = I_{OUT}^2 \cdot R_{DS(ON)} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad \text{(eq. 7)}$$

Switching losses are dependent on the drain to source voltage at turn-off state, output current, and switch-on and switch-off times, as is shown by Equation (8).

$$P_{SW} = \frac{V_{DS(OFF)}}{2} \cdot (t_{ON} + t_{OFF}) \cdot f_{SW} \cdot I_{OUT} \quad \text{(eq. 8)}$$

t_{ON} and t_{OFF} times are dependent on the transistor gate charge.

The MOSFET output capacitance loss is caused by the charging and discharging during the switching process and can be computed using Equation (9).

$$P_{COSS} = \frac{C_{OSS} \cdot V_{IN}^2 \cdot f_{SW}}{2} \quad \text{(eq. 9)}$$

where $C_{OSS} = C_{DS} + C_{GS}$.

Some power dissipation is caused by the reverse recovery charge in the low side MOSFET body diode, which conducts at dead time. This charge is needed to close the diode. The current from the input power supply flows through the high side MOSFET to the low side MOSFET body diode. This power dissipation can be calculated using the following Equation (10):

$$P_{QRR} = Q_{RR} \cdot V_{IN} \cdot f_{SW} \quad \text{(eq. 10)}$$

Q_{RR} is the diode recovery charge as given in the manufacturer's datasheet. For some types of MOSFETs, this dissipation may be dominant at high input voltages. It is necessary to take care when selecting a MOSFET. An external Schottky diode across the low side MOSFET can be used to eliminate the reverse recovery charge power loss. The Schottky diode's forward voltage should be lower than that of the body diode, and reverse recovery time (t_{rr}) should be lower then that of the body diode. The Schottky diode's capacitance loss can be calculated as shown in Equation (11).

$$P_{C(schottky)} = \frac{C_{schottky} \cdot V_{IN}^2 \cdot f_{SW}}{2} \quad \text{(eq. 11)}$$

Adaptive Deadtime

The NCP1581 includes voltage mode adaptive dead time feature. This block waits for full turn off of the one of MOSFETs before the second one can be turned on. Detection is based on driver voltage, when this voltage drops below V_{ADT} second driver can be turned on. There is fixed time t_{DEAD} between turn off detection and internal logical turn on signal that increase safety. There can't be used additional gate resistors due to voltage base detection, because these resistors would create voltage divider with driver's pull down transistor and correct turn off detection is impossible. Gate resistors may be used only if MOSFETs turn off time is at all operation conditions shorter than t_{DEAD}. MOSFETs' timing diagram can be seen at Figure 11.

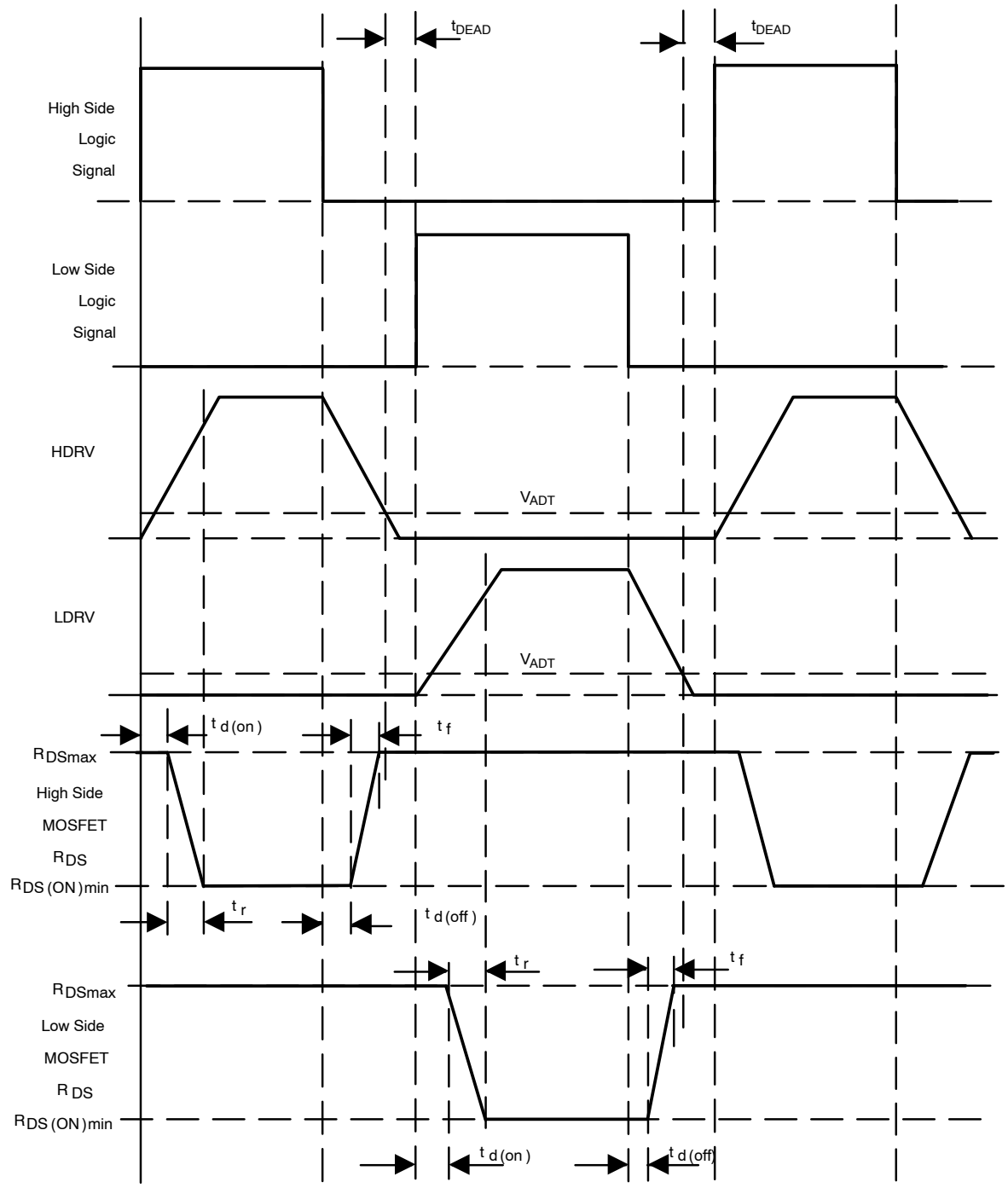


Figure 11. MOSFETs Timing Diagram

Soft Start

The soft start time is set by a capacitor connected between the SS pin and ground. This function is used for controlling the output voltage slope and limiting start-up currents. The start-up sequence initiates when the Power On Ready (POR) internal signal rises to logic level high. That means the supply voltage and $V_{P/EN}$ voltage are over the set thresholds. The soft start capacitor is charged by a 22 μA current source. If POR is low, the SS pin is internally pulled to GND, which means that the NCP1581 is in a shutdown state. The SS pin voltage (0 V to 2 V) controls the internal current source (64 μA to 0 μA) with a negative linear characteristic. This current source injects current into the resistor (25 kΩ) connected between the FB pin and the negative input of the error amplifier and into the external feedback resistor network. Voltage drop on these resistors is over 1.6 V, which is enough to force the error amplifier into a negative saturation state and to block switching.

When the soft start pin reaches around 1.2 V (exact value depends on feedback and compensation network and on the soft start capacitor; a larger soft start capacitor and a lower compensation capacity decrease this level), the IC starts switching. The impact of the controlled current source decreases and the output voltage starts to rise. When the soft start capacitor voltage reaches 2 V, the output voltage is at nominal value.

The soft start time must be at least 10 times longer than the time needed to charge the compensation network from the output of the error amplifier. If the soft start time is not long enough, the soft start sequence would be faster than the charging compensation network and the IC would start without slowly increasing the output voltage. The soft start capacitance can be calculated using Equation 12:

$$C_{SS} = 22 \cdot 10^{-6} \cdot T_{SS} \quad \text{(eq. 12)}$$

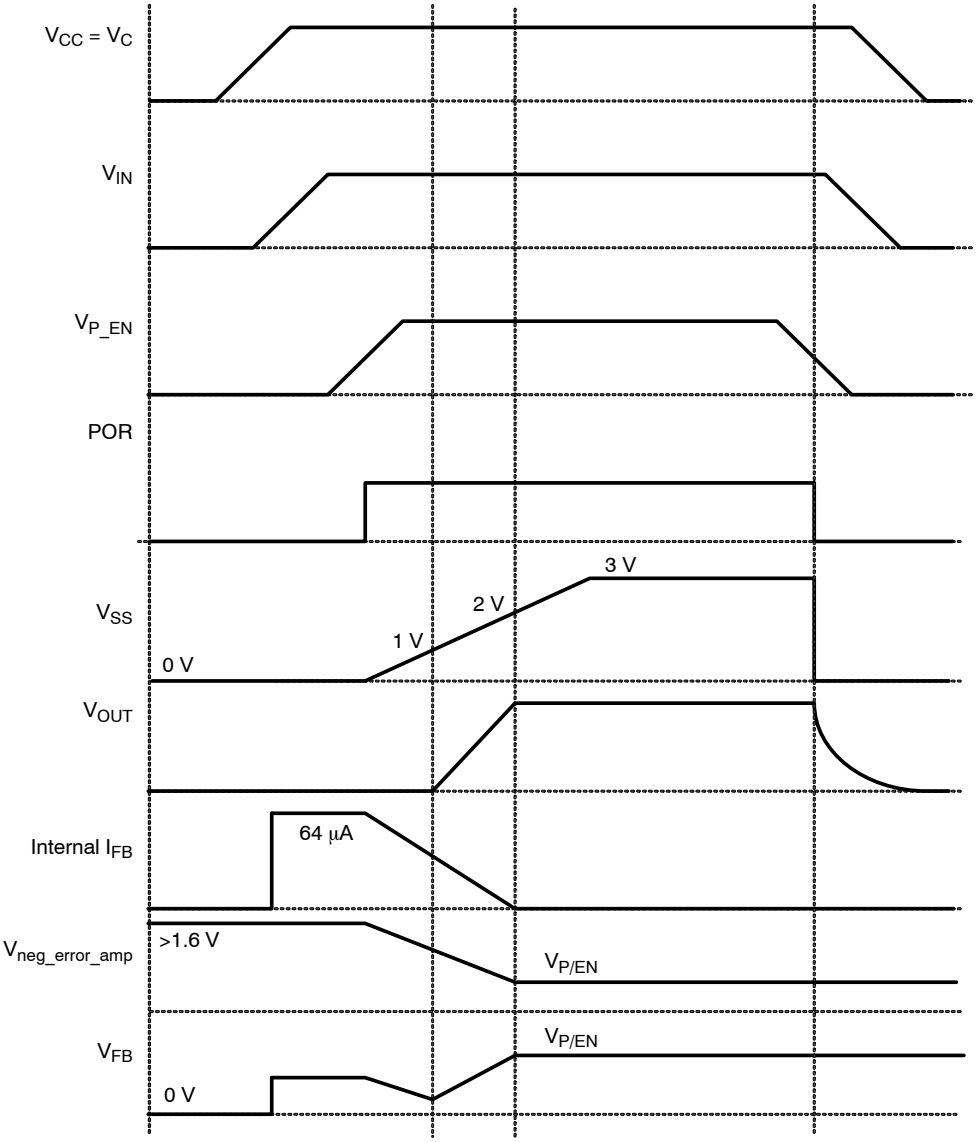


Figure 12. Start-up Sequence

Start to Pre-biased Output

The NCP1581 is able to start up into a pre-biased output capacitor. The low side MOSFET does not turn on before the output voltage is at set value. During this time, the energy is not discharged by the low side MOSFET (current flows through low side MOSFET body diode) until the soft start sequence ends.

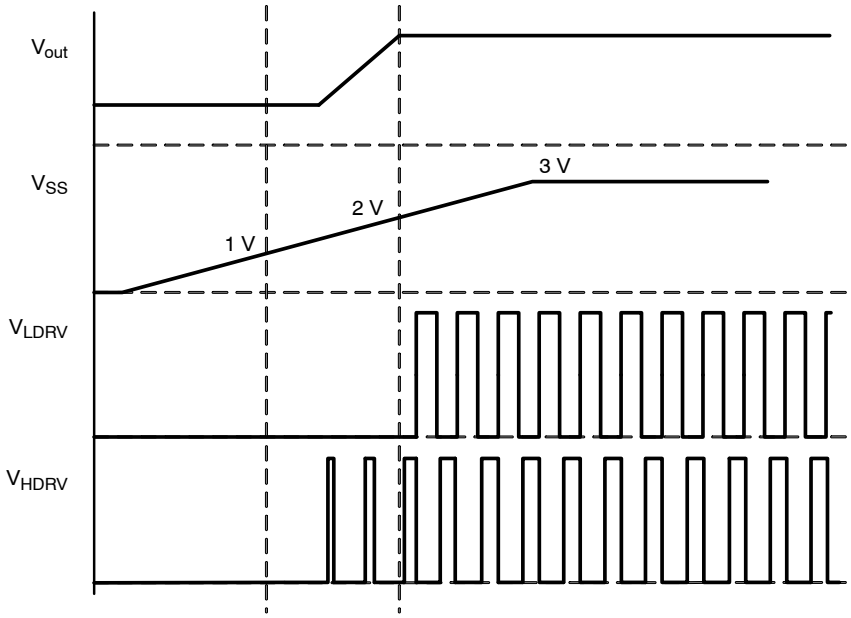


Figure 13. Start-up to Pre-biased Output

Short Circuit Protection

The output of convertor with NCP1581 is protected against short circuit conditions. This protection is sensing output voltage through feedback divider on FB pin. On this pin is comparator that compares FB voltage to 0.4 V. If FB voltage is below 0.4 V then IC goes to latch state and switch output drivers to off state. Latch state can be released by decrease V_{CC} or $V_{P/EN}$ voltage below threshold.

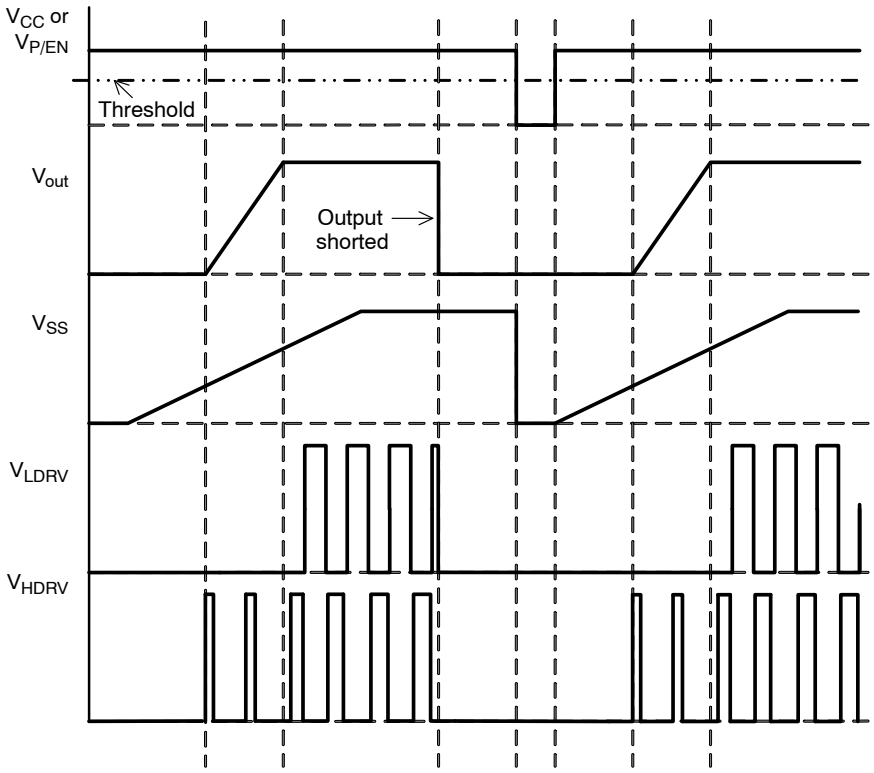


Figure 14. Short Circuit Protection (Start Up, Short, Latch, Latch Release and New Start-up)

Compensation Circuit

The NCP1581 is a voltage mode buck converter with a transconductance error amplifier compensated by an external compensation network. Compensation is needed to achieve accurate output voltage regulation and fast transient response. The goal of the compensation circuit is to provide a loop gain function with the highest crossing frequency and adequate phase margin (minimally 45°).

The transfer function of the power stage (the output LC filter) is a double pole system. The resonance frequency of this filter is expressed as follows:

$$f_{PO} = \frac{1}{2 \cdot \pi \cdot \sqrt{L \cdot C_{OUT}}} \quad \text{(eq. 13)}$$

One zero of this LC filter is given by the output capacitance and output capacitor ESR. Its value can be calculated using the following equation:

$$f_{Z0} = \frac{1}{2 \cdot \pi \cdot C_{OUT} \cdot ESR} \quad \text{(eq. 14)}$$

The next parameter that must be chosen is the zero crossover frequency f_0. It can be chosen to be 1/10–1/5 of the switching frequency. These three parameters show the necessary type of compensation that can be selected from Table 6.

Table 6. COMPENSATION TYPES

Zero Crossover Frequency Condition	Compensation Type	Typical Output Capacitor Type
$f_{P0} < f_{Z0} < f_0 < f_{SW}/2$	Type II (PI)	Electrolytic, Tantalum
$f_{P0} < f_0 < f_{Z0} < f_{SW}/2$	Type III (PID) Method I	Tantalum, Ceramic
$f_{P0} < f_0 < f_{SW}/2 < f_{Z0}$	Type III (PID) Method II	Ceramic

Compensation Type II (PI)

This compensation is suitable for low-cost electrolytic capacitors. The zero created by the capacitor's ESR is a few kHz, and the zero crossover frequency is chosen to be 1/10 of the switching frequency. Components of the PI compensation (Figure 15) network can be specified by the following equations:

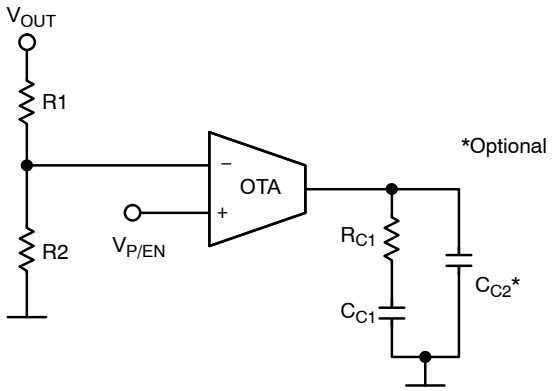


Figure 15. PI compensation (Type II)

$$R_{C1} = \frac{2 \cdot \pi \cdot f_0 \cdot L \cdot V_{RAMP} \cdot V_{OUT}}{ESR \cdot V_{IN} \cdot V_{P/EN} \cdot gm}$$

$$C_{C1} = \frac{1}{0.75 \cdot 2 \cdot \pi \cdot f_{P0} \cdot R_{C1}} \quad \text{(eq. 15)}$$

$$C_{C2} = \frac{1}{\pi \cdot R_{C1} \cdot f_{SW}}$$

$$R1 = \frac{V_{OUT} - V_{P/EN}}{V_{P/EN}} \cdot R2$$

V_{RAMP} is the peak-to-peak voltage of the oscillator ramp, and gm is the transconductance error amplifier gain. Capacitor C_{C2} is optional.

Compensation Type III (PID)

Tantalum and ceramic capacitors have lower ESR than electrolytic capacitors, so the zero of the output LC filter goes to a higher frequency above the zero crossover frequency. This situation needs to be compensated by the PID compensation network that is shown in Figure 16.

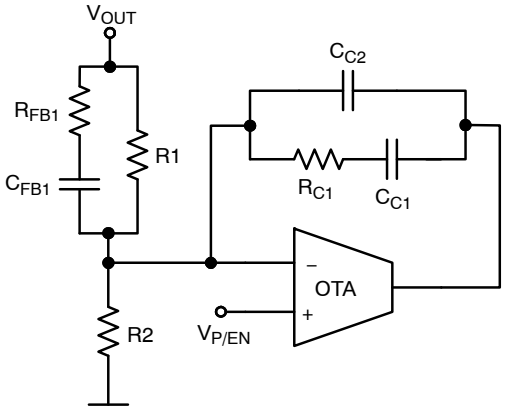


Figure 16. PID Compensation (Type III)

There are two methods to select the zeros and poles of the compensation network. The first one (method I) is usable for tantalum output capacitors, which have a higher ESR than ceramics, and its zeros and poles can be calculated as shown below:

$$f_{Z1} = 0.75 \cdot f_{P0}$$

$$f_{Z2} = f_{P0}$$

$$f_{P2} = f_{Z0} \quad \text{(eq. 16)}$$

$$f_{P3} = \frac{f_{SW}}{2}$$

The second one (method II) is for ceramic capacitors:

$$f_{Z2} = f_0 \cdot \sqrt{\frac{1 - \sin\theta_{max}}{1 + \sin\theta_{max}}}$$
$$f_{P2} = f_0 \cdot \sqrt{\frac{1 + \sin\theta_{max}}{1 - \sin\theta_{max}}} \quad \text{(eq. 17)}$$
$$f_{Z1} = 0.5 \cdot f_{Z2}$$
$$f_{P3} = 0.5 \cdot f_{SW}$$

The remaining calculations are the same for both methods.

$$R_{C1} >> \frac{2}{gm}$$
$$C_{C1} = \frac{1}{2 \cdot \pi \cdot f_{Z1} \cdot R_{C1}}$$
$$C_{C2} = \frac{1}{2 \cdot \pi \cdot f_{P3} \cdot R_{C1}} \quad \text{(eq. 18)}$$
$$C_{FB1} = \frac{2 \cdot \pi \cdot f_0 \cdot L \cdot V_{RAMP} \cdot C_{OUT}}{V_{IN} \cdot R_{C1}}$$
$$R_{FB1} = \frac{1}{2 \cdot \pi \cdot C_{FB1} \cdot f_{P2}}$$
$$R1 = \frac{1}{2 \cdot \pi \cdot C_{FB1} \cdot f_{Z2}} - R_{FB1}$$
$$R2 = \frac{V_{P/EN}}{V_{OUT} - V_{P/EN}} \cdot R1$$

To check the design of this compensation network, the following equation must be true:

$$\frac{R1 \cdot R2 \cdot R_{FB1}}{R1 \cdot R_{FB1} + R2 \cdot R_{FB1} + R1 \cdot R2} > \frac{1}{gm} \quad \text{(eq. 19)}$$

If it is not true, then a higher value of R_{C1} must be selected.

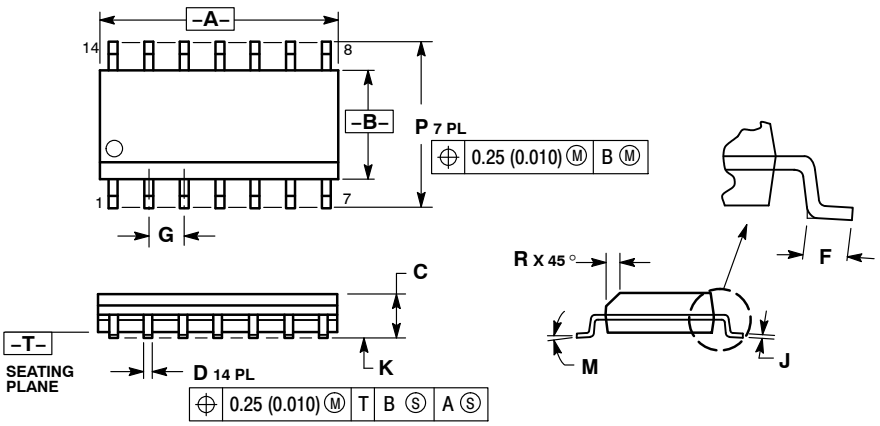
ORDERING INFORMATION

Device	Package	Shipping†
NCP1581DR2G	SOIC−14 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

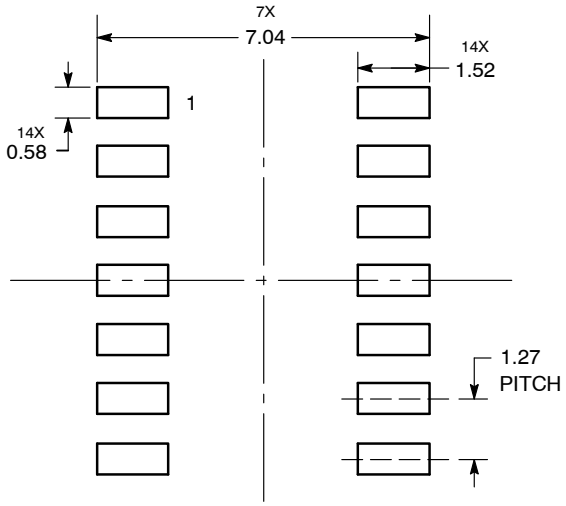
SOIC−14
CASE 751A−03
ISSUE J



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0 °	7 °	0 °	7 °
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

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