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Alpha & Omega Semiconductor Inc.
AON7448

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ALPHA & OMEGA SEMICONDUCTOR

AON7448

80V N-Channel MOSFET

SDMOS™

General Description

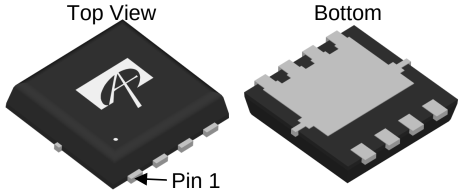
The AON7448 is fabricated with SDMOS™ trench technology that combines excellent $R_{DS(ON)}$ with low gate charge and low Qrr.The result is outstanding efficiency with controlled switching behavior. This universal technology is well suited for PWM, load switching and general purpose applications.

Product Summary

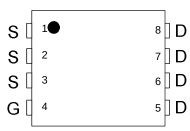
V_{DS}	80V
I_D (at V_{GS}=10V)	24A
$R_{DS(ON)}$ (at V_{GS}=10V)	< 30mΩ
$R_{DS(ON)}$ (at V_{GS} = 8V)	< 37mΩ

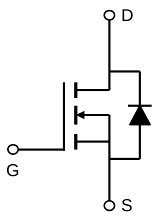
100% UIS Tested
100% R_g Tested

DFN 3x3 EP



Top View





Absolute Maximum Ratings T_A=25℃ unless otherwise noted

Parameter		Symbol	Maximum	Units
Drain-Source Voltage		V_{DS}	80	V
Gate-Source Voltage		V_{GS}	±25	V
Continuous Drain Current	T_C=25℃	I_D	24	A
	T_C=100℃		15	
Pulsed Drain Current [C]		I_{DM}	76	
Continuous Drain Current	T_A=25℃	I_{DSM}	7.1	A
	T_A=70℃		5.7	
Avalanche Current [C]		I_{AS}, I_{AR}	25	A
Avalanche energy L=0.1mH [C]		E_{AS}, E_{AR}	31	mJ
Power Dissipation [B]	T_C=25℃	P_D	36	W
	T_C=100℃		15	
Power Dissipation [A]	T_A=25℃	P_{DSM}	3.1	W
	T_A=70℃		2	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150	℃

Thermal Characteristics

Parameter		Symbol	Typ	Max	Units
Maximum Junction-to-Ambient [A]	t ≤ 10s	$R_{\theta JA}$	30	40	℃/W
Maximum Junction-to-Ambient [A D]	Steady-State		60	75	℃/W
Maximum Junction-to-Case	Steady-State	$R_{\theta JC}$	2.8	3.4	℃/W

Electrical Characteristics (T_J=25℃ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=250µA, V_{GS}=0V	80			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=80V, V_{GS}=0V			10	µA
		T_J=55℃			50	
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}= ±25V			100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS} I_D=250µA	2.9	3.5	4.1	V
$I_{D(ON)}$	On state drain current	V_{GS}=10V, V_{DS}=5V	78			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=10V, I_D=10A		25	30	mΩ
		T_J=125℃		44	53	
		V_{GS}=8V, I_D=10A		29	37	mΩ
g_{FS}	Forward Transconductance	V_{DS}=5V, I_D=10A		16		S
V_{SD}	Diode Forward Voltage	I_S=1A,V_{GS}=0V		0.7	1	V
I_S	Maximum Body-Diode Continuous Current [G]				40	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=40V, f=1MHz	720	900	1100	pF
C_{oss}	Output Capacitance		75	110	150	pF
C_{rss}	Reverse Transfer Capacitance		25	40	60	pF
R_g	Gate resistance	V_{GS}=0V, V_{DS}=0V, f=1MHz	0.4	0.8	1.2	Ω
SWITCHING PARAMETERS						
Q_g(10V)	Total Gate Charge	V_{GS}=10V, V_{DS}=40V, I_D=10A	11.5	14.5	17.5	nC
Q_{gs}	Gate Source Charge		4.5	5.5	6.5	nC
Q_{gd}	Gate Drain Charge		2.8	4.6	6.5	nC
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=10V, V_{DS}=40V, R_L=4Ω, R_{GEN}=3Ω		16		ns
t_r	Turn-On Rise Time			7.5		ns
$t_{D(off)}$	Turn-Off DelayTime			36		ns
t_f	Turn-Off Fall Time			7.5		ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=10A, dI/dt=500A/µs	10	15	20	ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=10A, dI/dt=500A/µs	30	43	56	nC

A. The value of $R_{\theta JA}$ is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A =25℃. The Power dissipation P_{DSM} is based on R $_{\theta JA}$ t ≤ 10s value and the maximum allowed junction temperature of 150℃. The value in any given application depends on the user's specific board design, and the maximum temperature of 150℃ may be u sed if the PCB allows it.
B. The power dissipation P_D is based on $T_{J(MAX)}$=150℃, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.
C. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=150℃. Ratings are based on low frequency and duty cycles to keep initial T_J =25℃.
D. The $R_{\theta JA}$ is the sum of the thermal impedence from junction to case $R_{\theta JC}$ and case to ambient.
E. The static characteristics in Figures 1 to 6 are obtained using <300µs pulses, duty cycle 0.5% max.
F. These curves are based on the junction-to-case thermal impedence which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}$=150℃. The SOA curve provides a single pulse ratin g.
G. The maximum current rating is package limited.
H. These tests are performed with the device mounted on 1 in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25℃.

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

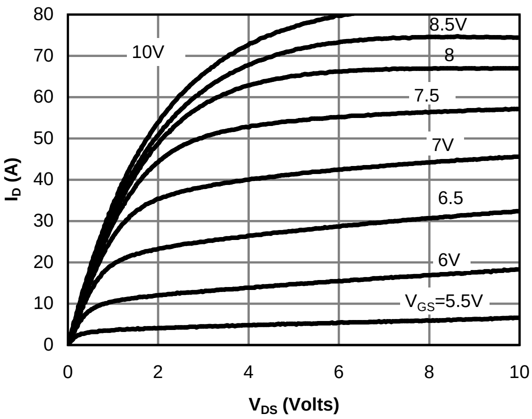


Fig 1: On-Region Characteristics (Note E)

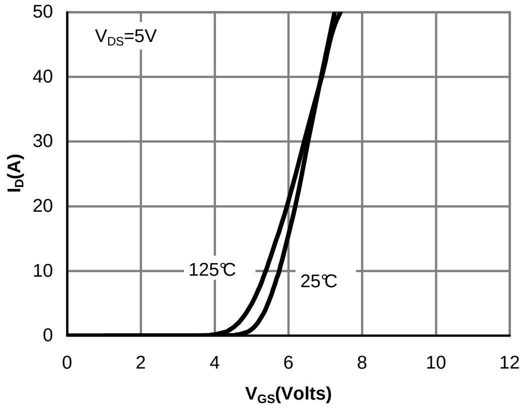


Figure 2: Transfer Characteristics (Note E)

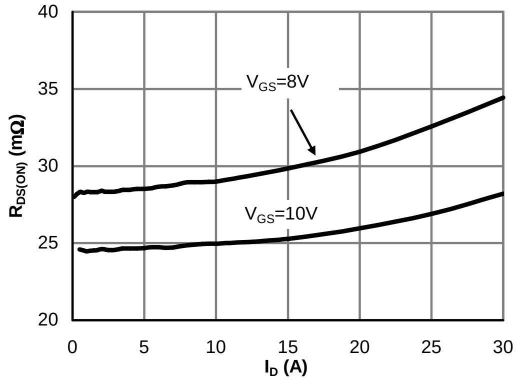


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

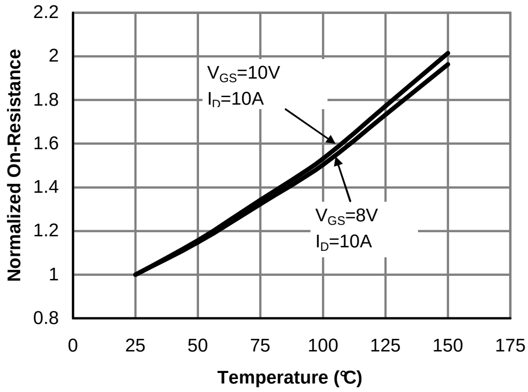


Figure 4: On-Resistance vs. Junction Temperature (Note E)

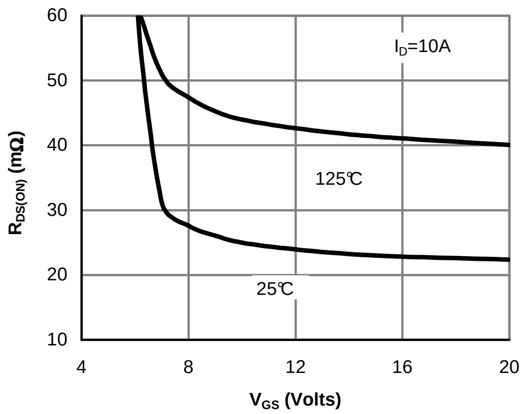


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

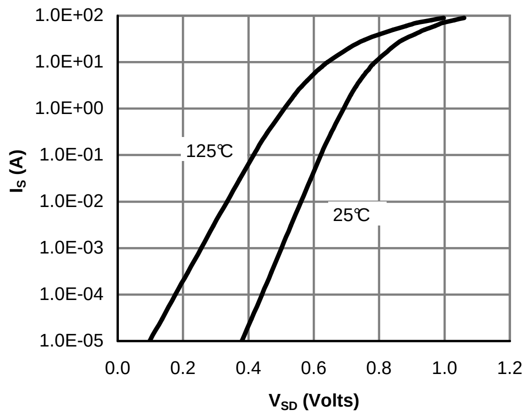


Figure 6: Body-Diode Characteristics (Note E)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

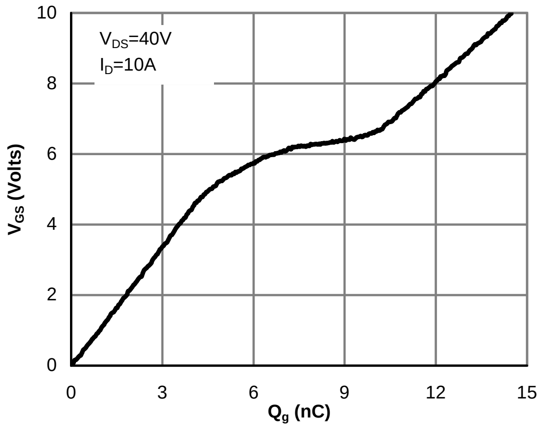


Figure 7: Gate-Charge Characteristics

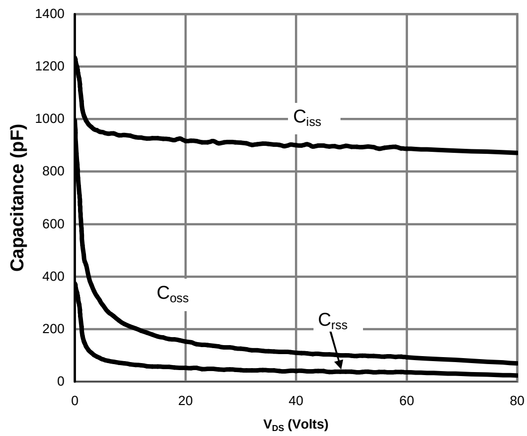


Figure 8: Capacitance Characteristics

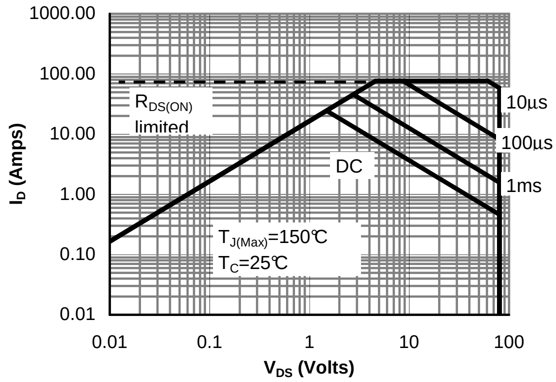


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

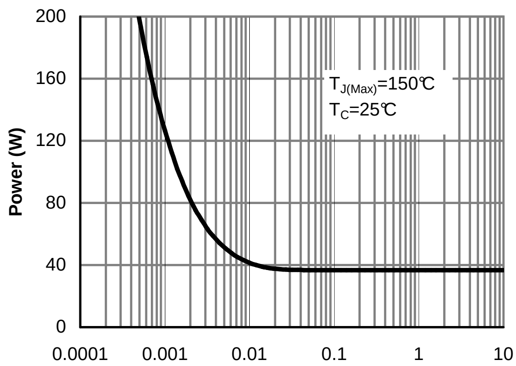


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

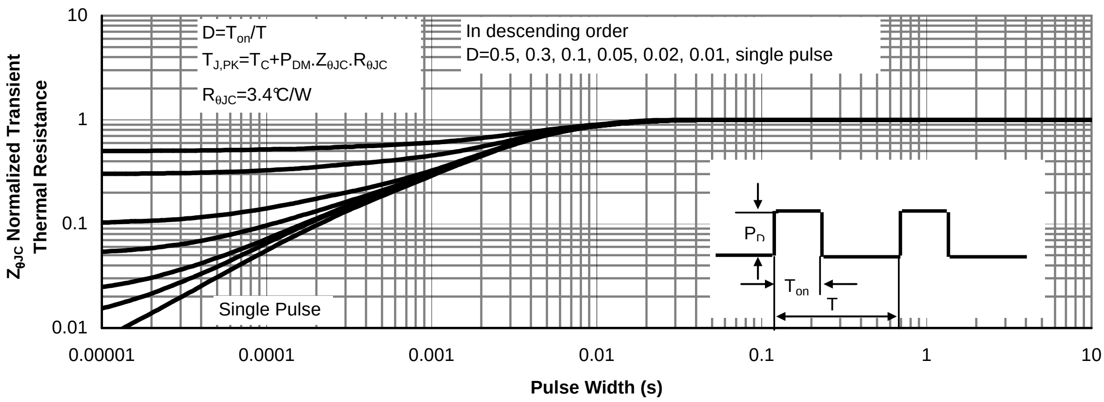


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

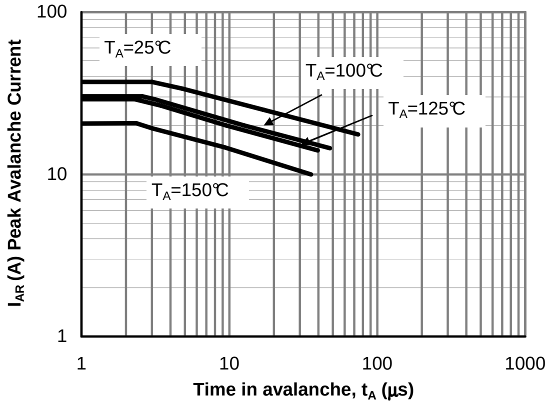


Figure 12: Single Pulse Avalanche capability (Note C)

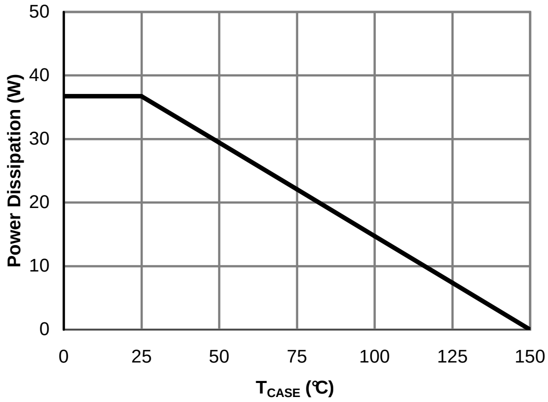


Figure 13: Power De-rating (Note F)

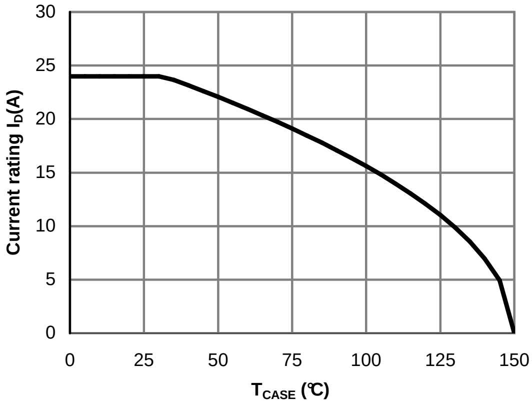
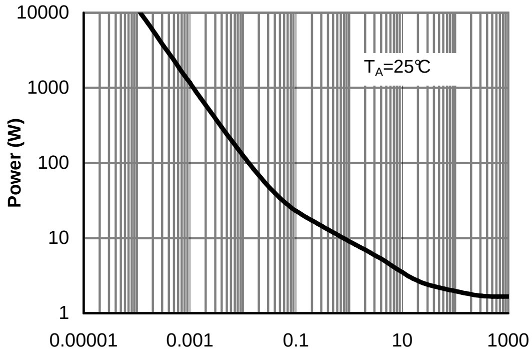
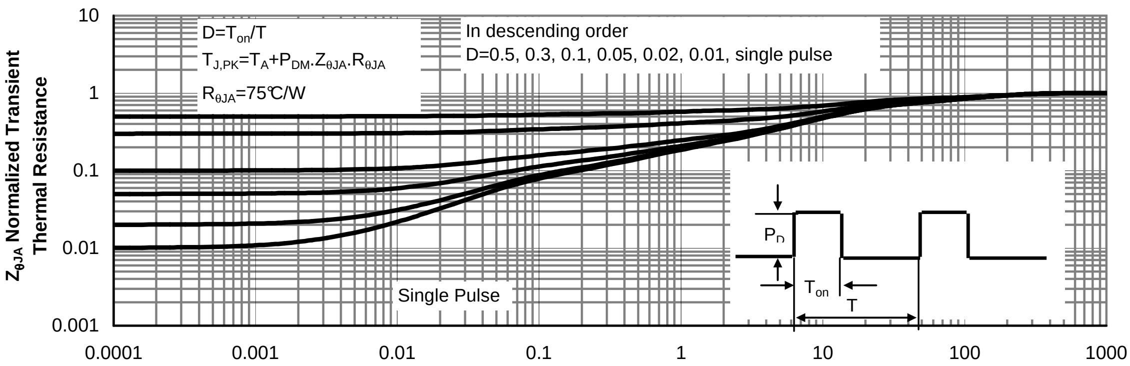


Figure 14: Current De-rating (Note F)



Pulse Width (s)

Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)



Pulse Width (s)

Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

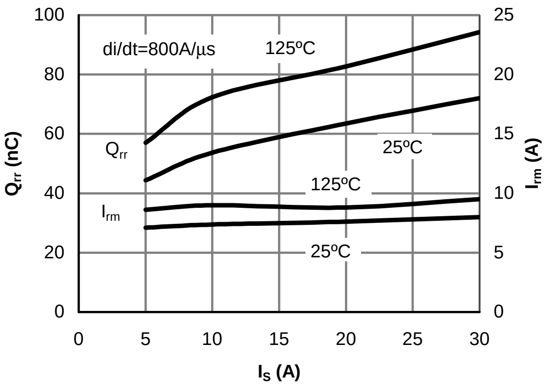


Figure 17: Diode Reverse Recovery Charge and Peak Current vs. Conduction Current

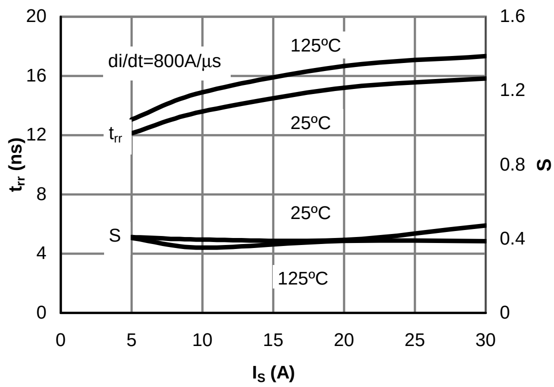


Figure 18: Diode Reverse Recovery Time and Softness Factor vs. Conduction Current

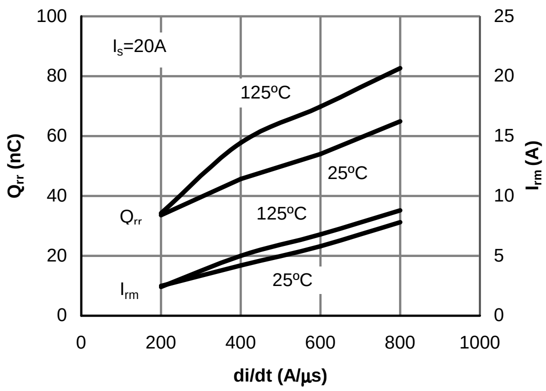


Figure 19: Diode Reverse Recovery Charge and Peak Current vs. di/dt

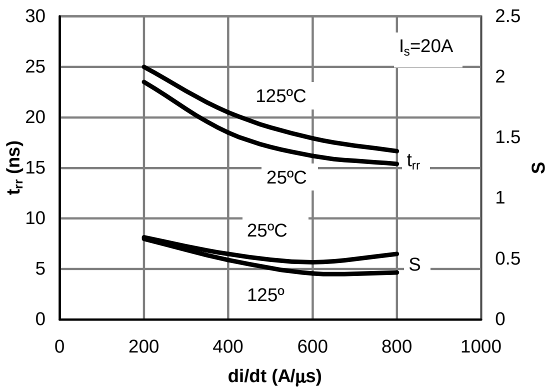
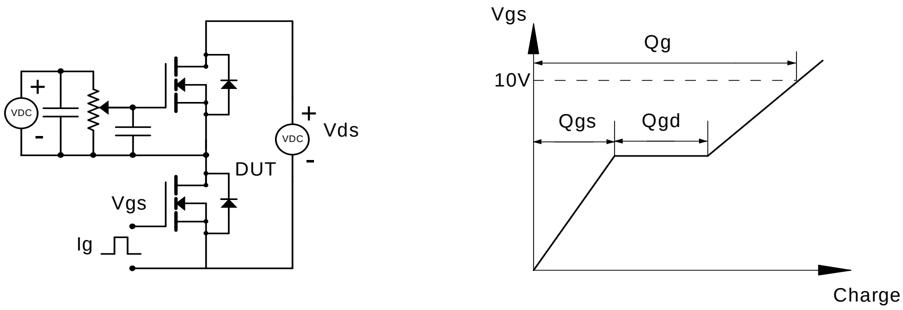
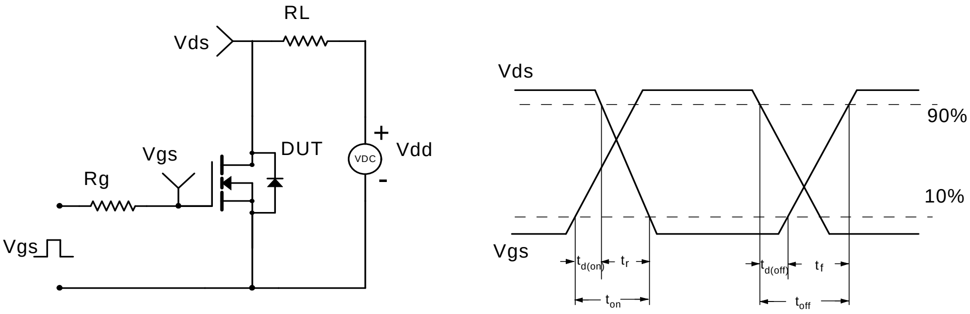


Figure 20: Diode Reverse Recovery Time and Softness Factor vs. di/dt

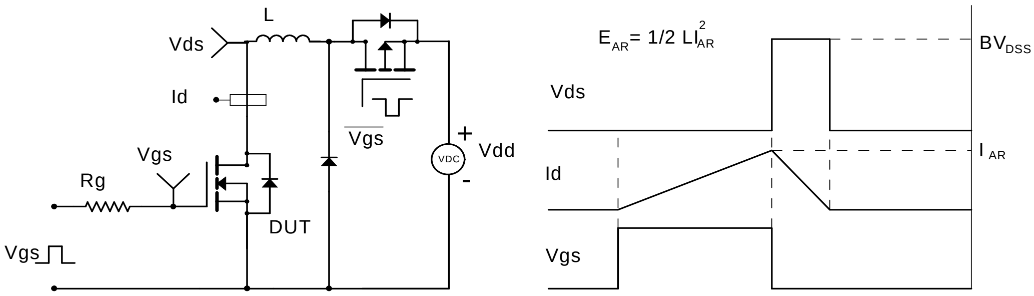
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms