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ADVANCED
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ALD1721/ALD1721G

PRECISION MICROPOWER CMOS OPERATIONAL AMPLIFIER

GENERAL DESCRIPTION

The ALD1721/ALD1721G is a monolithic CMOS micropower high slew rate operational amplifier intended for a broad range of precision applications requiring extremely low input signal power. Input signal power is the product of input offset voltage and input bias current, which represents the minimum required power draw from the signal source in order to drive the input of the operational amplifier. Input signal power is also a figure of merit in source loading and its associated error, and is a measure of the basic signal resolution possible through the operational amplifier for a given signal source. For certain types of signal sources, signal loading directly translates into a significant distortion or "interface noise equivalent" term.

The ALD1721/ALD1721G is designed to set a new standard in low input signal power requirements. The typical input loading at its input is 0.05 mV offset voltage and 0.01 pA input bias current at 25°C, resulting in 0.0005 fW input signal power draw. This input characteristic virtually eliminates any loading effects on most types of signal sources, offering unparalleled accuracy and signal integrity and fidelity. Obviously, for capacitive and high sensitivity, high impedance signal sources, the ALD1721/ALD1721G is ideally suited. It is readily suited for +5V single supply (or ±1V to ±5V) systems, with low operating power dissipation, a traditional strength of CMOS technology. It is offered with industry standard pin configuration of μ A741 and ICL7611 types.

The ALD1721/ALD1721G can operate with rail to rail large signal input and output voltages with relatively high slew rate. The input voltage can be equal to or exceed the positive and negative supply voltages while the output voltage can swing close to these supply voltage rails. This feature significantly reduces the supply overhead voltage required to operate the operational amplifier and allows numerous analog serial stages to operate in a low power supply environment. In addition, the device can accommodate mixed applications where digital and analog circuits may operate off the same power supply or battery. Finally, the output stage can typically drive up to 50pF capacitive and 10K Ω resistive loads.

These features make the ALD1721/ALD1721G a versatile, micropower high precision operational amplifier that is user friendly and easy to use with virtually no source loading and zero input-loading induced source errors. Additionally, robust design and rigorous screening make this device especially suitable for operation in temperature-extreme environments and rugged conditions.

FEATURES & BENEFITS

- Lead Free - RoHS compatible
- Robust high-temperature operation
- Guaranteed extremely low input signal power of 1.5 fW
- Input offset voltage of 0.05 mV typical (0.15 mV max.)
- Low input bias currents of 0.01pA typical (10pA max.)
- Rail to rail input and output voltage ranges
- All parameters specified for +5V single supply or \pm 2.5V dual supplies
- Unity gain stable, no compensation needed
- High voltage gain -- typically 100V/mV @ \pm 2.5V(100dB)
- Drive as low as 10K Ω load
- Output short circuit protected
- Unity gain bandwidth of 0.7MHz
- Slew rate of 0.7V/ μ s
- Micro power dissipation
- Suitable for rugged, temperature-extreme environments

APPLICATIONS

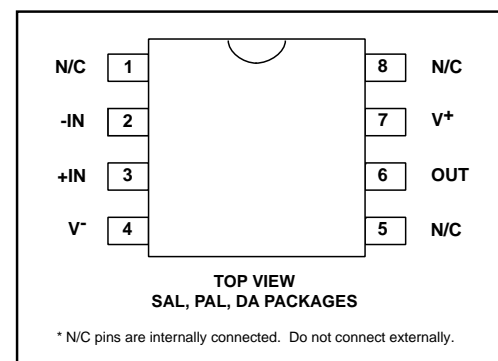
- Voltage amplifier
- Voltage follower/buffer
- Charge integrator
- Photodiode amplifier
- Data acquisition systems
- High performance portable instruments
- Signal conditioning circuits
- Sensor and transducer amplifiers
- Low leakage amplifiers
- Active filters
- Sample/Hold amplifier
- Picoammeter
- Current to voltage converter

ORDERING INFORMATION ("L" suffix denotes lead-free (RoHS))

Operating Temperature Range		
0°C to +70°C	0°C to +70°C	-55°C to +125°C
8-Pin Small Outline Package (SOIC)	8-Pin Plastic Dip Package	8-Pin CERDIP Package
ALD1721SAL ALD1721GSAL	ALD1721PAL ALD1721GPAL	ALD1721DA ALD1721GDA

* Contact factory for leaded (non-RoHS) or high temperature versions.

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{+} _____ 10.6V
Differential input voltage range _____ -0.3V to $V_{+} + 0.3V$
Power dissipation _____ 600 mW
Operating temperature range SAL, PAL packages _____ 0°C to +70°C
DA package _____ -55°C to +125°C
Storage temperature range _____ -65°C to +150°C
Lead temperature, 10 seconds _____ +260°C

CAUTION: ESD Sensitive Device. Use static control procedures in ESD controlled environment.

OPERATING ELECTRICAL CHARACTERISTICS

$T_A = 25^{\circ}\text{C}$ $V_S = \pm 2.5V$ unless otherwise specified

Parameter	Symbol	1721			1721G			Unit	Test Conditions
		Min	Typ	Max	Min	Typ	Max		
Supply Voltage	V_S V_{+}	± 1.0 2.0		± 5.0 10.0	± 1.0 2.0		± 5.0 10.0	V	Dual Supply Single Supply
Input Offset Voltage	V_{OS}		0.05	0.15 0.6		0.15	0.35 1.0	mV mV	$R_S \leq 100K\Omega$ $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$
Input Offset Current	I_{OS}		0.01	10 240		0.01	10 240	pA pA	$T_A = 25^{\circ}\text{C}$ $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$
Input Bias Current	I_B		0.01	10 240		0.01	10 240	pA pA	$T_A = 25^{\circ}\text{C}$ $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$
Input Voltage Range	V_{IR}	-0.3 -2.8		5.3 2.8	-0.3 -2.8		5.3 2.8	V V	$V_{+} = +5V$ $V_S = \pm 2.5V$
Input Resistance	R_{IN}		10^{14}			10^{14}		Ω	
Input Offset Voltage Drift	TCV_{OS}		5			7		$\mu V/^{\circ}\text{C}$	$R_S \leq 100K\Omega$
Power Supply Rejection Ratio	PSRR	65 65	80 80		65 65	80 80		dB dB	$R_S \leq 100K\Omega$ $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$
Common Mode Rejection Ratio	CMRR	65 65	83 83		65 65	83 83		dB dB	$R_S \leq 100K\Omega$ $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$
Large Signal Voltage Gain	A_V	32 20	100 1000		32 20	100 1000		V/mV V/mV V/mV	$R_L = 100K\Omega$ $R_L \geq 1M\Omega$ $R_L = 100K\Omega$ $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$
Output Voltage Range	$V_{O\text{ low}}$ $V_{O\text{ high}}$	4.99	0.001 4.999	0.01	4.99	0.001 4.999	0.01	V V	$R_L = 1M\Omega$ $V_{+} = +5V$ $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$
	$V_{O\text{ low}}$ $V_{O\text{ high}}$	2.40	-2.48 2.48	-2.40	2.40	-2.48 2.48	-2.40	V V	$R_L = 100K\Omega$ $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$
Output Short Circuit Current	I_{SC}		1			1		mA	
Supply Current	I_S		110	200		110	200	μA	$V_{IN} = 0V$ No Load
Power Dissipation	P_D		0.6	1.0		0.6	1.0	mW	$V_S = \pm 2.5V$

OPERATING ELECTRICAL CHARACTERISTICS (cont'd)

$T_A = 25^{\circ}\text{C}$ $V_S = \pm 2.5\text{V}$ unless otherwise specified (cont'd)

Parameter	Symbol	1721			1721G			Unit	Test Conditions
		Min	Typ	Max	Min	Typ	Max		
Input Capacitance	C_{IN}		1			1		pF	
Bandwidth	B_W	400	700		400	700		KHz	
Slew Rate	S_R	0.33	0.7		0.33	0.7		V/ μs	$A_V = +1$ $R_L = 100\text{K}\Omega$
Rise time	t_r		0.2			0.2		μs	$R_L = 100\text{K}\Omega$
Overshoot Factor			20			20		%	$R_L = 100\text{K}\Omega$ $C_L = 50\text{pF}$
Settling Time	t_s		10.0			10.0		μs	0.1% $A_V = -1$ $R_L = 100\text{K}\Omega$ $C_L = 50\text{pF}$

$T_A = 25^{\circ}\text{C}$ $V_S = \pm 5.0\text{V}$ unless otherwise specified

Parameter	Symbol	1721			1721G			Unit	Test Conditions
		Min	Typ	Max	Min	Typ	Max		
Power Supply Rejection Ratio	PSRR		83			83		dB	$R_S \leq 100\text{K}\Omega$
Common Mode Rejection Ratio	CMRR		83			83		dB	$R_S \leq 100\text{K}\Omega$
Large Signal Voltage Gain	A_V		250			250		V/mV	$R_L = 100\text{K}\Omega$
Output Voltage Range	$V_{O \text{ low}}$ $V_{O \text{ high}}$	4.90	-4.98 4.98	-4.90	4.90	-4.98 4.98	-4.90	V V	$R_L = 100\text{K}\Omega$
Bandwidth	B_W		1.0			1.0		MHz	
Slew Rate	S_R		1.0			1.0		V/ μs	$A_V = +1$ $C_L = 50\text{pF}$

$V_S = \pm 2.5\text{V}$ $-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ unless otherwise specified

Parameter	Symbol	1721			1721G			Unit	Test Conditions
		Min	Typ	Max	Min	Typ	Max		
Input Offset Voltage	V_{OS}			1.0			2.0	mV	$R_S \leq 100\text{K}\Omega$
Input Offset Current	I_{OS}			2.0			2.0	nA	
Input Bias Current	I_B			2.0			2.0	nA	
Power Supply Rejection Ratio	PSRR	60	75		60	75		dB	$R_S \leq 100\text{K}\Omega$
Common Mode Rejection Ratio	CMRR	60	83		60	83		dB	$R_S \leq 100\text{K}\Omega$
Large Signal Voltage Gain	A_V	15	50		15	50		V/ mV	$R_L = 100\text{K}\Omega$
Output Voltage Range	$V_{O \text{ low}}$ $V_{O \text{ high}}$	2.35	-2.47 2.45	-2.40	2.35	-2.47 2.45	-2.40	V V	$R_L = 100\text{K}\Omega$

Design & Operating Notes:

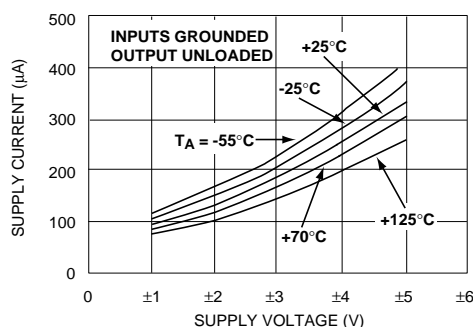
1. The ALD1721/ALD1721G CMOS operational amplifier uses a 3 gain stage architecture and an improved frequency compensation scheme to achieve large voltage gain, high output driving capability, and better frequency stability. The ALD1721/ALD1721G is internally compensated for unity gain stability. This compensation produces a clean single pole roll off in the gain characteristics while providing for more than 70 degrees of phase margin at the unity gain frequency, reducing or eliminating low levels of oscillation or ringing with many types of loading conditions.
2. The ALD1721/ALD1721G has complementary p-channel and n-channel input differential stages connected in parallel to accomplish rail to rail input common mode voltage range. With different ranges of common mode input voltage, one or both of the two differential stages is active. The transition between the two input stages takes place at about 1.5V below the positive supply voltage. Input offset voltage trimming on the ALD1721/ALD1721G is made when the input voltage is symmetrical to the supply voltages, this internal transition switching does not affect a variety of applications such as an inverting amplifier or non-inverting amplifier with a gain larger than 2.5 (5V operation), where the common mode voltage does not make excursions above this switching point. If the operational amplifier is connected as a unity gain buffer, and full input and/or output rail to rail range is used, then provision should be made to allow for slight input offset voltage variations. Likewise the output has push-pull(source-sink) output stages working in tandem to provide full (see note 4) rail to rail output. In addition, the source and sink currents are designed to provide symmetrical drives to the load.
3. The input bias and offset currents are essentially input protection diode reverse bias leakage currents, and are typically less than 0.01pA at room temperature. This low input bias current assures that the analog signal from the source will not be distorted by input bias currents. Normally, this extremely high input impedance of greater than $10^{14}\Omega$ would be limited by the source impedance which

would limit the node impedance. However, for applications where source impedance is also very high, it may be necessary to limit noise and hum pickup through proper ground shielding.

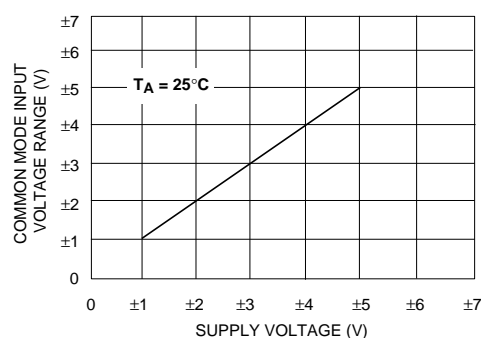
4. The output stage consists of class AB complementary output drivers, capable of driving a low resistance load to either supply rail. The output voltage swing is limited by the drain to source on-resistance of the output transistors as determined by the bias circuitry, and the value of the load resistor. When connected in the voltage follower configuration, the oscillation resistant feature, combined with the rail to rail input and output feature, makes an effective analog signal buffer for medium to high source impedance sensors, transducers, and other circuit networks.
5. The ALD1721/ALD1721G operational amplifier has been designed to provide static discharge protection. Internally, the design has been carefully implemented to minimize latch up. However, care must be exercised when handling the device to avoid strong static fields that may degrade a diode junction, causing increased input leakage currents. The user is advised to power up the circuit before, or simultaneously with any input voltages applied, and to limit input voltages not to exceed 0.3V of the power supply voltage levels at all times, including during power up and power down cycles.
6. The ALD1721/ALD1721G, with its micropower operation, offers benefits in reduced power supply requirements, less noise coupling and current spikes, less thermally induced drift, better overall reliability due to lower self heating, and lower input bias current. It requires practically no warm up time as the chip junction heats up to 0.1°C or less above ambient temperature under most operating conditions.
7. The ALD1721/ALD1721G has an internal design architecture that provides robust high temperature operation. Contact factory for custom screening versions.

TYPICAL PERFORMANCE CHARACTERISTICS

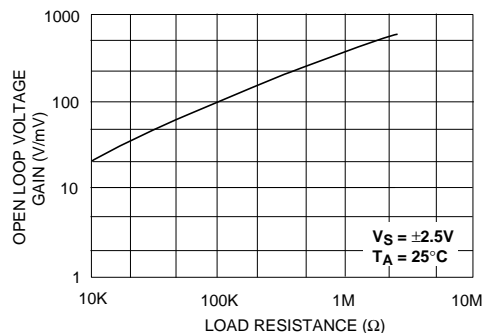
SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



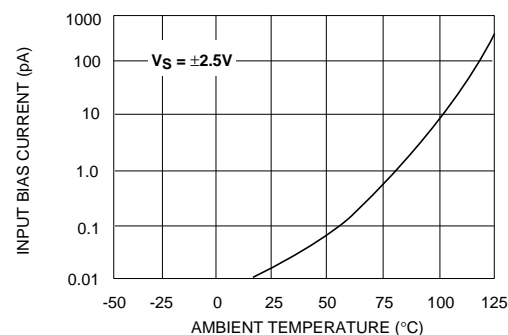
COMMON MODE INPUT VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF LOAD RESISTANCE

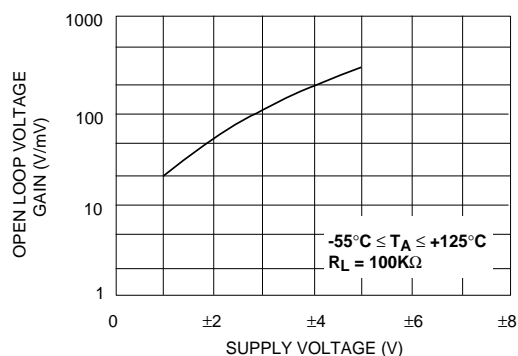


INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

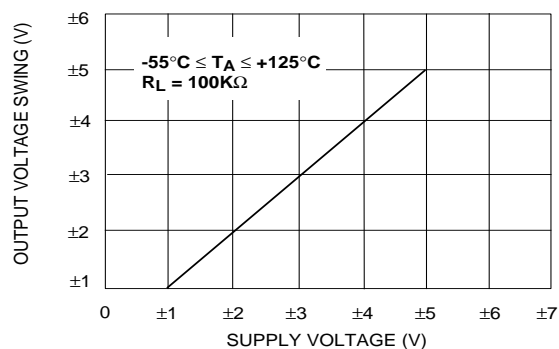


TYPICAL PERFORMANCE CHARACTERISTICS (cont'd)

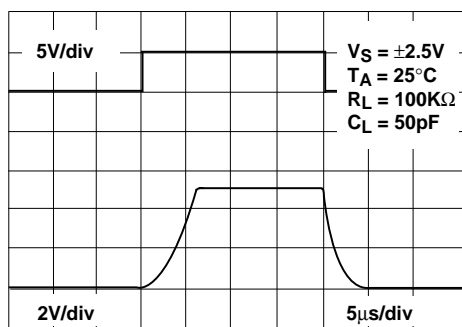
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE AND TEMPERATURE



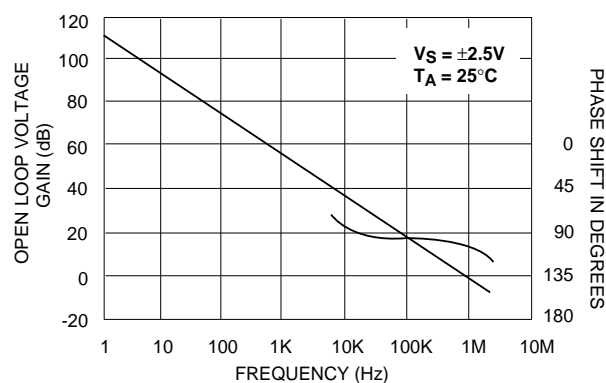
OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE



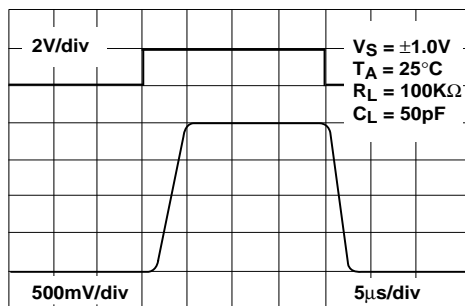
LARGE - SIGNAL TRANSIENT RESPONSE



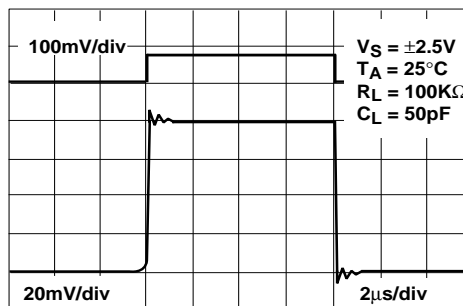
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



LARGE - SIGNAL TRANSIENT RESPONSE

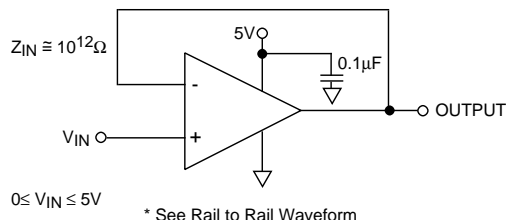


SMALL - SIGNAL TRANSIENT RESPONSE

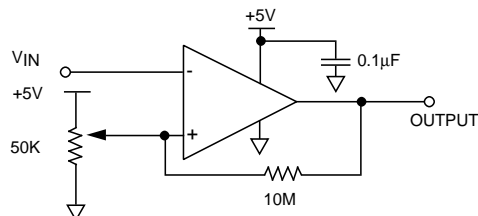


TYPICAL APPLICATIONS

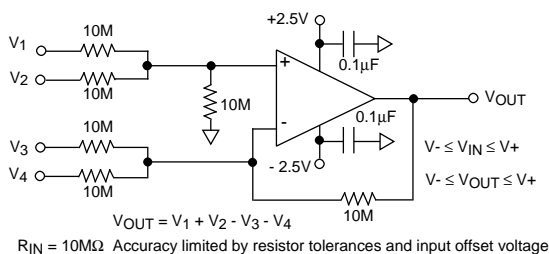
RAIL-TO-RAIL VOLTAGE FOLLOWER/BUFFER



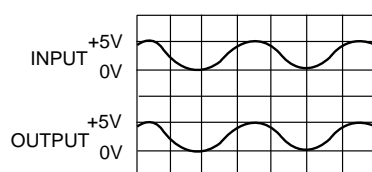
RAIL-TO-RAIL VOLTAGE COMPARATOR



HIGH INPUT IMPEDANCE RAIL-TO-RAIL PRECISION DC SUMMING AMPLIFIER



RAIL-TO-RAIL WAVEFORM



Performance waveforms.
Upper trace is the output of a Wien Bridge Oscillator. Lower trace is the output of Rail-to-rail voltage follower.

WIEN BRIDGE OSCILLATOR (RAIL-TO-RAIL) SINE WAVE GENERATOR

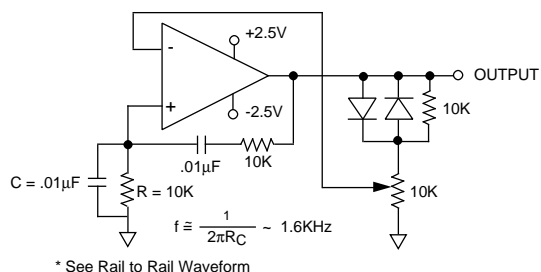
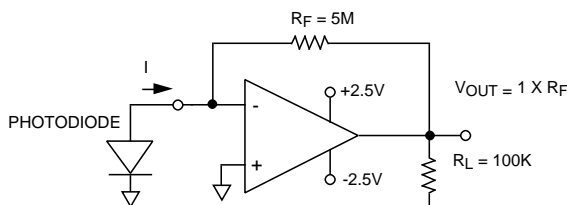
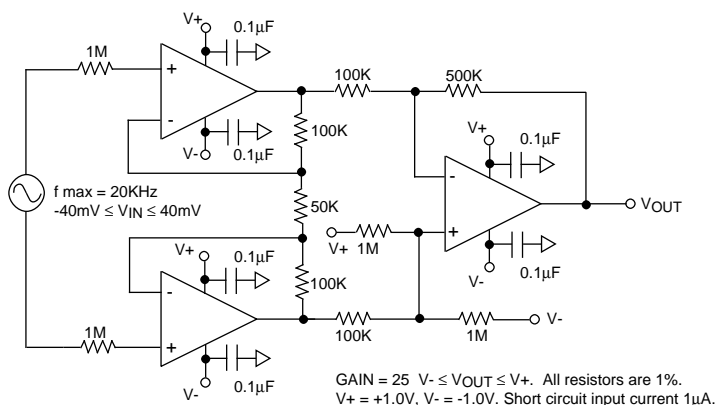


PHOTO DETECTOR CURRENT TO VOLTAGE CONVERTER

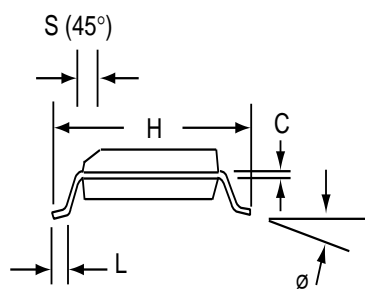
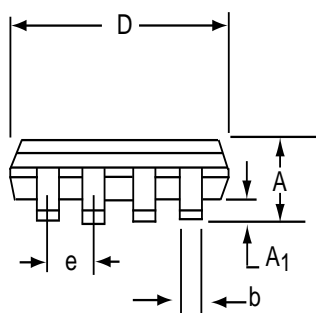
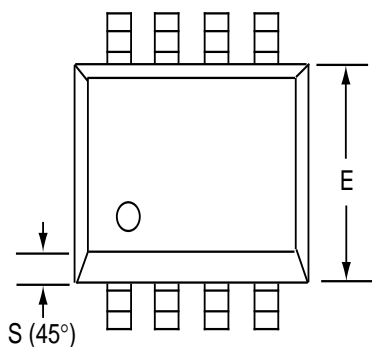


LOW VOLTAGE INSTRUMENTATION AMPLIFIER



SOIC-8 PACKAGE DRAWING

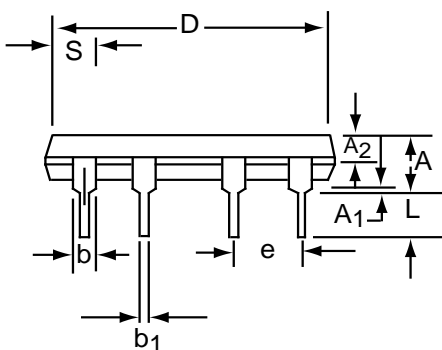
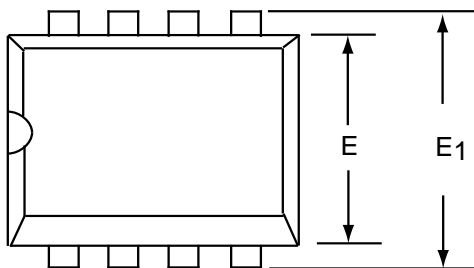
8 Pin Plastic SOIC Package



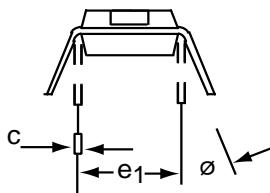
Dim	Millimeters		Inches	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A ₁	0.10	0.25	0.004	0.010
b	0.35	0.45	0.014	0.018
C	0.18	0.25	0.007	0.010
D-8	4.69	5.00	0.185	0.196
E	3.50	4.05	0.140	0.160
e	1.27 BSC		0.050 BSC	
H	5.70	6.30	0.224	0.248
L	0.60	0.937	0.024	0.037
Ø	0°	8°	0°	8°
S	0.25	0.50	0.010	0.020

PDIP-8 PACKAGE DRAWING

8 Pin Plastic DIP Package

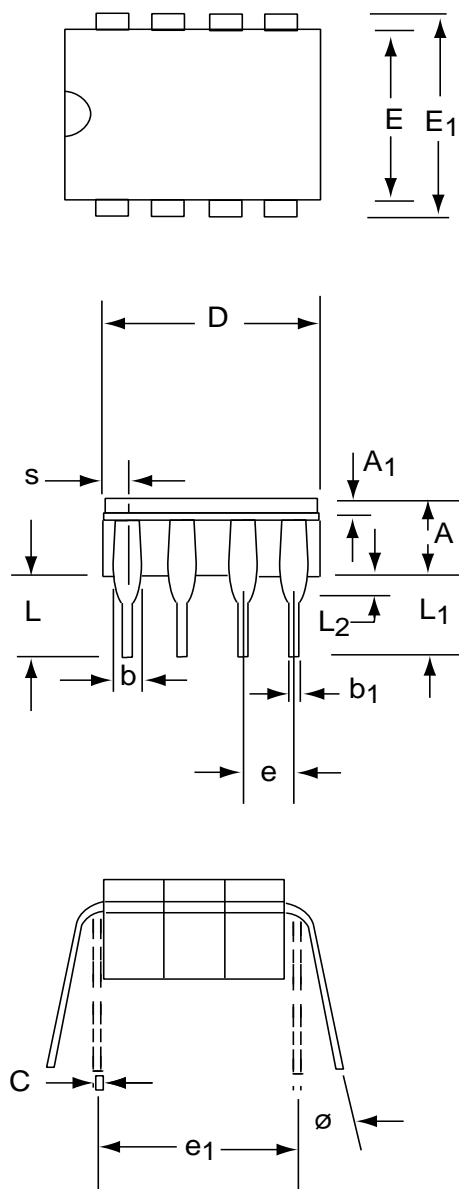


Dim	Millimeters		Inches	
	Min	Max	Min	Max
A	3.81	5.08	0.105	0.200
A ₁	0.38	1.27	0.015	0.050
A ₂	1.27	2.03	0.050	0.080
b	0.89	1.65	0.035	0.065
b ₁	0.38	0.51	0.015	0.020
c	0.20	0.30	0.008	0.012
D-8	9.40	11.68	0.370	0.460
E	5.59	7.11	0.220	0.280
E ₁	7.62	8.26	0.300	0.325
e	2.29	2.79	0.090	0.110
e ₁	7.37	7.87	0.290	0.310
L	2.79	3.81	0.110	0.150
S-8	1.02	2.03	0.040	0.080
Ø	0°	15°	0°	15°



CERDIP-8 PACKAGE DRAWING

8 Pin CERDIP Package



Dim	Millimeters		Inches	
	Min	Max	Min	Max
A	3.55	5.08	0.140	0.200
A₁	1.27	2.16	0.050	0.085
b	0.97	1.65	0.038	0.065
b₁	0.36	0.58	0.014	0.023
C	0.20	0.38	0.008	0.015
D-8	--	10.29	--	0.405
E	5.59	7.87	0.220	0.310
E₁	7.73	8.26	0.290	0.325
e	2.54 BSC		0.100 BSC	
e₁	7.62 BSC		0.300 BSC	
L	3.81	5.08	0.150	0.200
L₁	3.18	--	0.125	--
L₂	0.38	1.78	0.015	0.070
S	--	2.49	--	0.098
Ø	0°	15°	0°	15°