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Stocking Distributor

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[Vishay/Siliconix](#)  
[SIB406EDK-T1-GE3](#)

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**New Product**



**SiB406EDK**  
 Vishay Siliconix

**N-Channel 20-V (D-S) MOSFET**

PRODUCT SUMMARY			
V <sub>DS</sub> (V)	R <sub>DS(on)</sub> (Ω)	I <sub>D</sub> (A) <sup>a</sup>	Q <sub>g</sub> (Typ.)
20	0.046 at V <sub>GS</sub> = 4.5 V	6	3.5 nC
	0.063 at V <sub>GS</sub> = 2.5 V	6	

**FEATURES**

- Halogen-free According to IEC 61249-2-21
- TrenchFET<sup>®</sup> Power MOSFET
- New Thermally Enhanced PowerPAK<sup>®</sup> SC-75 Package
  - Small Footprint Area
  - Low On-Resistance
- Typical ESD Protection 560 V

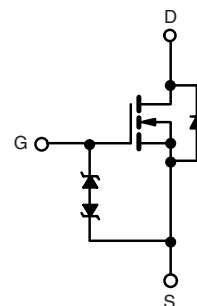
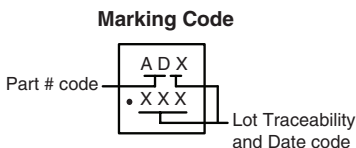
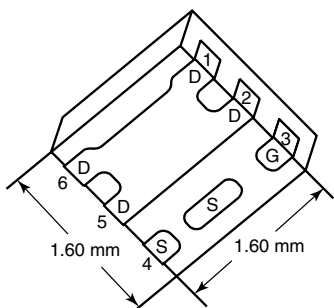


**RoHS**  
 COMPLIANT  
 HALOGEN  
**FREE**

**APPLICATIONS**

- Load Switch for Portable Applications
- High Frequency DC/DC Converter

PowerPAK SC-75-6L-Single



Ordering Information: SiB406EDK-T1-GE3 (Lead (Pb)-free and Halogen-free)

N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS T <sub>A</sub> = 25 °C, unless otherwise noted				
Parameter	Symbol	Limit	Unit	
Drain-Source Voltage	V <sub>DS</sub>	20	V	
Gate-Source Voltage	V <sub>GS</sub>	± 12		
Continuous Drain Current (T <sub>J</sub> = 150 °C)	I <sub>D</sub>	T <sub>C</sub> = 25 °C	6 <sup>a</sup>	A
		T <sub>C</sub> = 70 °C	6 <sup>a</sup>	
		T <sub>A</sub> = 25 °C	5.1 <sup>b, c</sup>	
		T <sub>A</sub> = 70 °C	4.1 <sup>b, c</sup>	
Pulsed Drain Current	I <sub>DM</sub>	15		
Continuous Source-Drain Diode Current	I <sub>S</sub>	T <sub>C</sub> = 25 °C	6 <sup>a</sup>	
		T <sub>A</sub> = 25 °C	1.6 <sup>b, c</sup>	
Maximum Power Dissipation	P <sub>D</sub>	T <sub>C</sub> = 25 °C	10	W
		T <sub>C</sub> = 70 °C	6.4	
		T <sub>A</sub> = 25 °C	1.95 <sup>b, c</sup>	
		T <sub>A</sub> = 70 °C	1.25 <sup>b, c</sup>	
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	- 55 to 150	°C	
Soldering Recommendations (Peak Temperature) <sup>d, e</sup>		260		

THERMAL RESISTANCE RATINGS					
Parameter	Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient <sup>b, f</sup>	R <sub>thJA</sub>	51	64	°C/W	
Maximum Junction-to-Case (Drain)	R <sub>thJC</sub>	10	12.5		

Notes:

- Package limited
- Surface Mounted on 1" x 1" FR4 board.
- t = 5 s.
- See Solder Profile ([www.vishay.com/ppg?73257](http://www.vishay.com/ppg?73257)). The PowerPAK SC-75 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.
- Maximum under Steady State conditions is 100 °C/W.

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<b>SPECIFICATIONS</b> $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	20			V
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 250\text{ }\mu\text{A}$		23		mV/°C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			-3.3		
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	0.6		1.4	V
Gate-Source Leakage	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = \pm 12\text{ V}$			$\pm 8$	$\mu\text{A}$
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}$ $V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$			-1 -10	
On-State Drain Current <sup>a</sup>	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}, V_{GS} = 4.5\text{ V}$	10			A
Drain-Source On-State Resistance <sup>a</sup>	$R_{DS(on)}$	$V_{GS} = 4.5\text{ V}, I_D = 3.9\text{ A}$		0.037	0.046	$\Omega$
		$V_{GS} = 2.5\text{ V}, I_D = 3.3\text{ A}$		0.051	0.063	
Forward Transconductance <sup>a</sup>	$g_{fs}$	$V_{DS} = 10\text{ V}, I_D = 3.9\text{ A}$		14		S
<b>Dynamic<sup>b</sup></b>						
Input Capacitance	$C_{iss}$	$V_{DS} = 10\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		350		$\mu\text{F}$
Output Capacitance	$C_{oss}$			63		
Reverse Transfer Capacitance	$C_{rss}$			37		
Total Gate Charge	$Q_g$	$V_{DS} = 10\text{ V}, V_{GS} = 10\text{ V}, I_D = 5.1\text{ A}$		7.5	12	nC
		$V_{DS} = 10\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 5.1\text{ A}$		3.5	5.5	
Gate-Source Charge	$Q_{gs}$			0.95		
Gate-Drain Charge	$Q_{gd}$		0.75			
Gate Resistance	$R_g$	$f = 1\text{ MHz}$		3.5		$\Omega$
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 10\text{ V}, R_L = 2.4\text{ }\Omega$ $I_D \cong 4.1\text{ A}, V_{GEN} = 4.5\text{ V}, R_g = 1\text{ }\Omega$		10	15	ns
Rise Time	$t_r$			12	20	
Turn-Off Delay Time	$t_{d(off)}$			18	30	
Fall Time	$t_f$			12	20	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 10\text{ V}, R_L = 2.4\text{ }\Omega$ $I_D \cong 4.1\text{ A}, V_{GEN} = 10\text{ V}, R_g = 1\text{ }\Omega$		5	10	
Rise Time	$t_r$			12	20	
Turn-Off Delay Time	$t_{d(off)}$			15	25	
Fall Time	$t_f$			10	15	
<b>Drain-Source Body Diode Characteristics</b>						
Continuous Source-Drain Diode Current	$I_S$	$T_C = 25\text{ }^\circ\text{C}$			6	A
Pulse Diode Forward Current	$I_{SM}$				15	
Body Diode Voltage	$V_{SD}$	$I_S = 4.1\text{ A}, V_{GS} = 0\text{ V}$		0.8	1.2	V
Body Diode Reverse Recovery Time	$t_{rr}$	$I_F = 4.1\text{ A}, di/dt = 100\text{ A}/\mu\text{s}, T_J = 25\text{ }^\circ\text{C}$		15	30	ns
Body Diode Reverse Recovery Charge	$Q_{rr}$			8	20	nC
Reverse Recovery Fall Time	$t_a$			8		ns
Reverse Recovery Rise Time	$t_b$			7		

Notes:

- a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$
- b. Guaranteed by design, not subject to production testing.

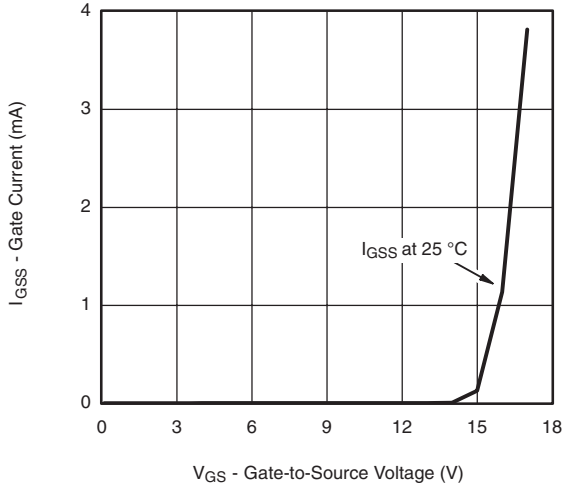
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**New Product**

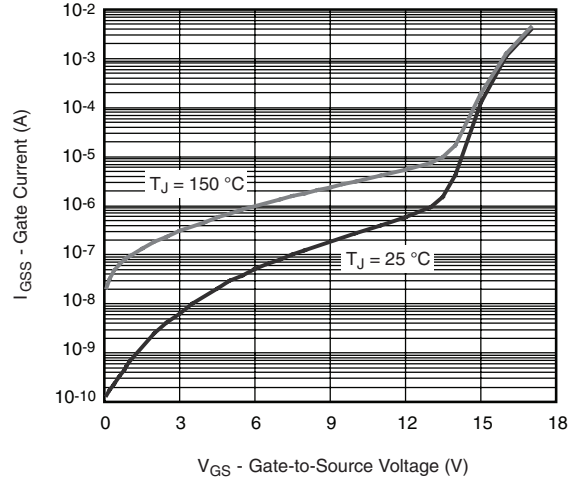


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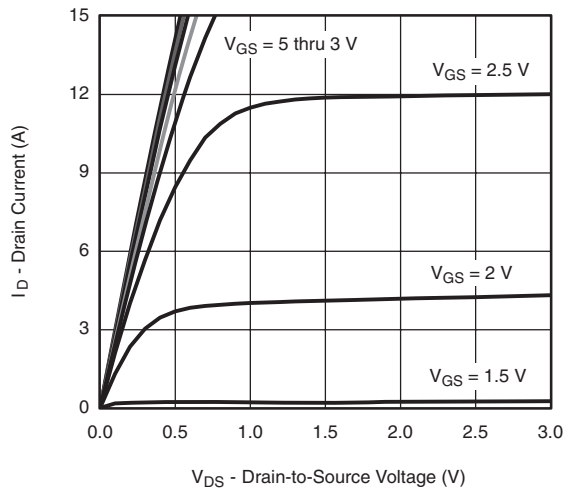
**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



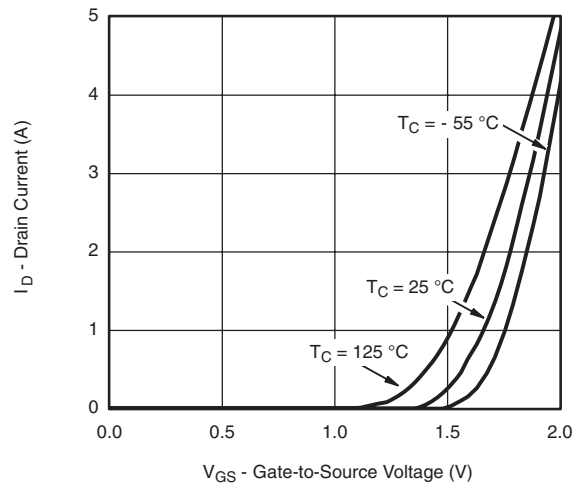
**Gate Current vs. Gate-Source Voltage**



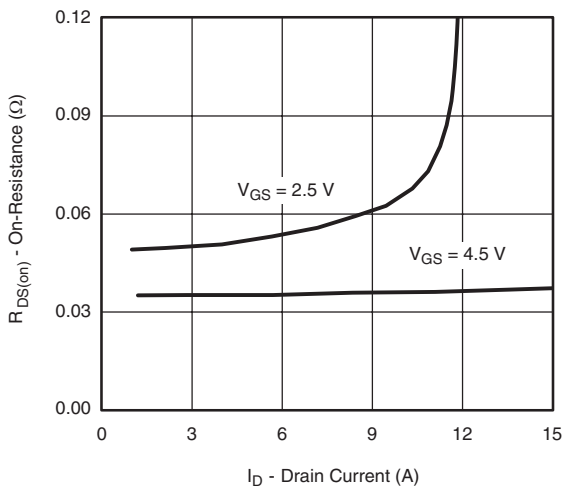
**Gate Current vs. Gate-Source Voltage**



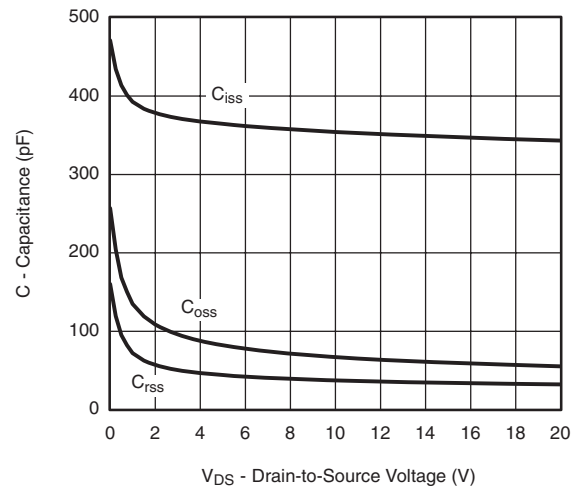
**Output Characteristics**



**Transfer Characteristics**



**On-Resistance vs. Drain Current and Gate Voltage**



**Capacitance**

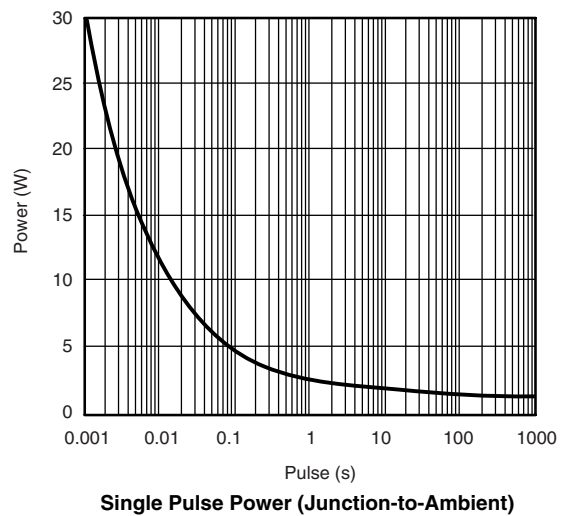
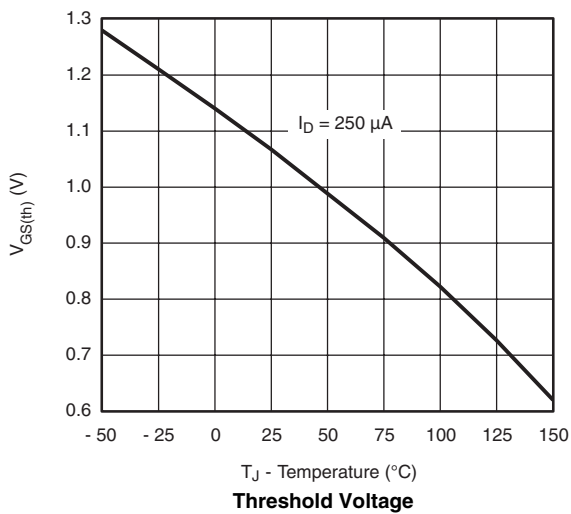
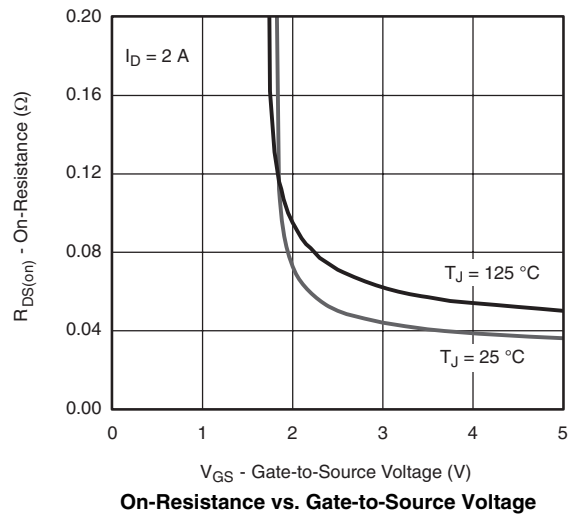
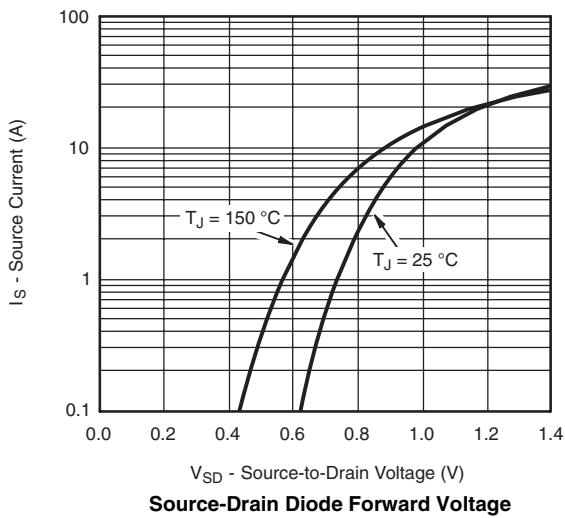
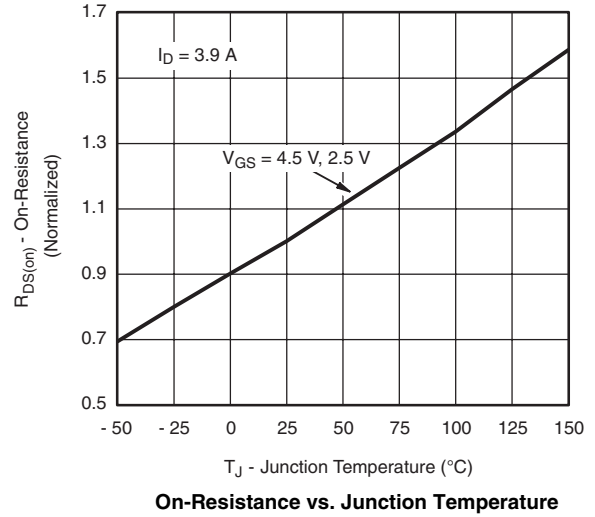
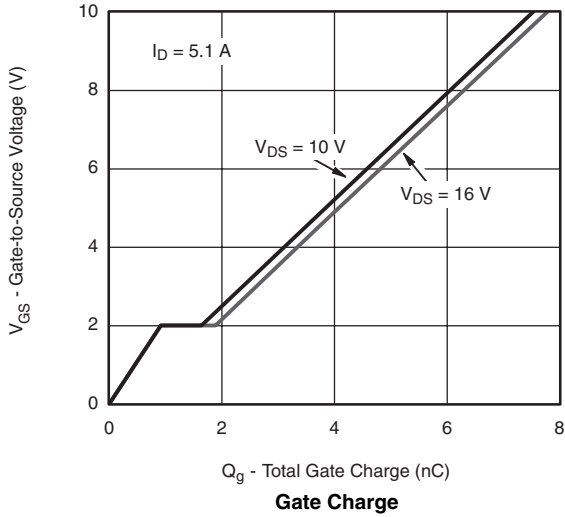
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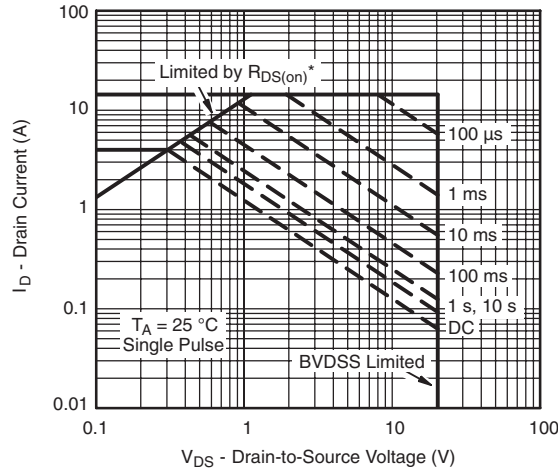


**New Product**



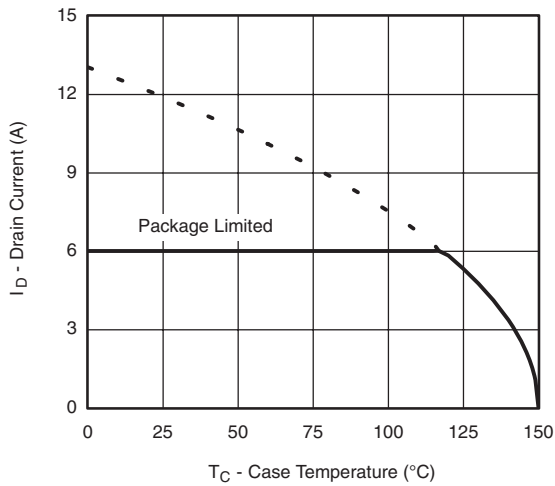
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**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted

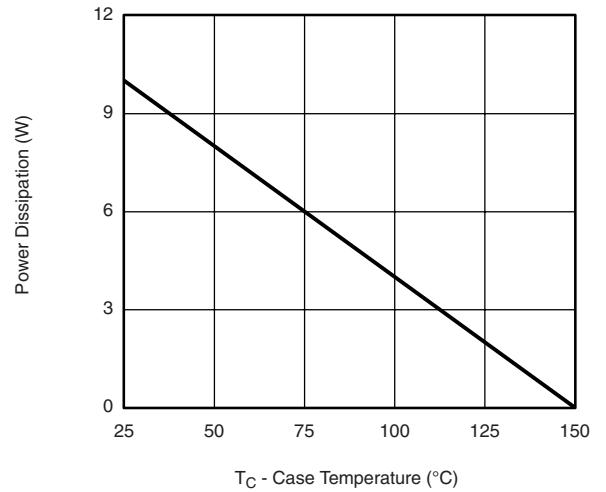


\*  $V_{GS} >$  minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified

**Safe Operating Area, Junction-to-Ambient**



**Current Derating\***



**Power Derating**

\* The power dissipation  $P_D$  is based on  $T_{J(max)} = 150$  °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

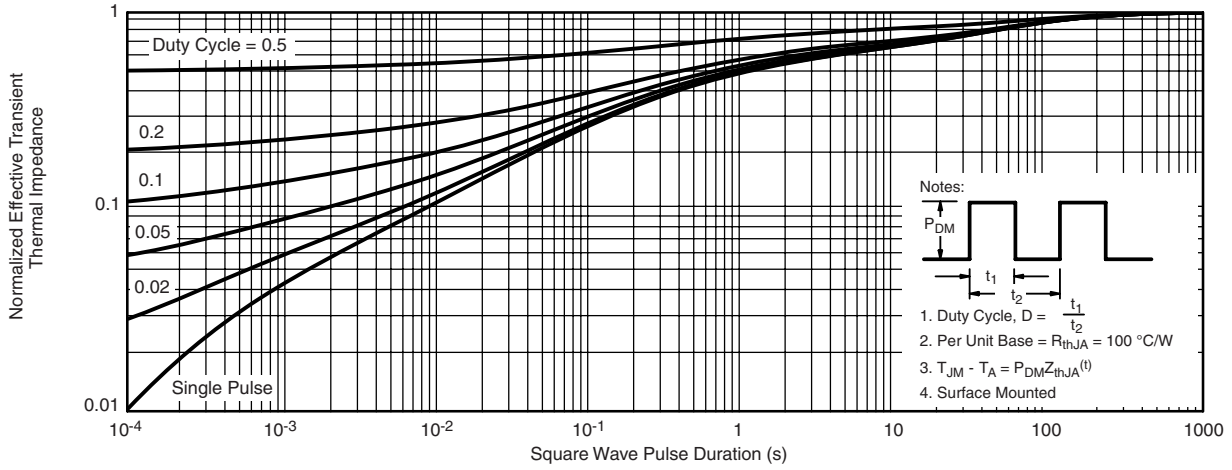
**New Product**

**SiB406EDK**

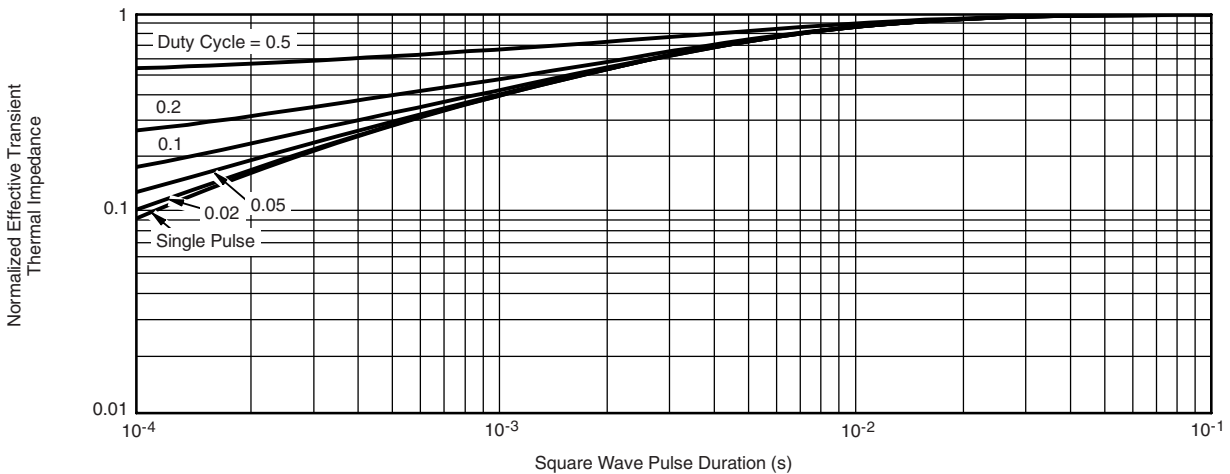
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**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



**Normalized Thermal Transient Impedance, Junction-to-Ambient**



**Normalized Thermal Transient Impedance, Junction-to-Case**

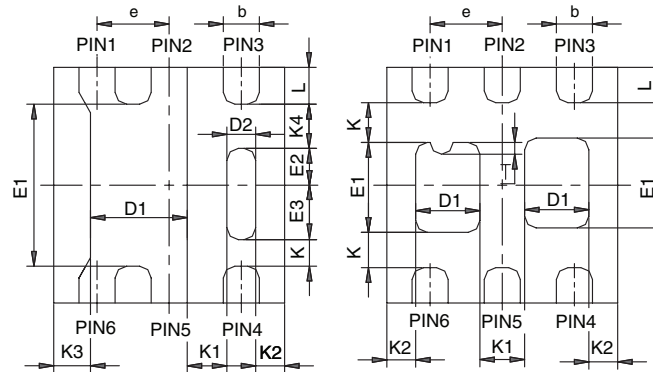
Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see [www.vishay.com/ppg?69088](http://www.vishay.com/ppg?69088).



# Package Information

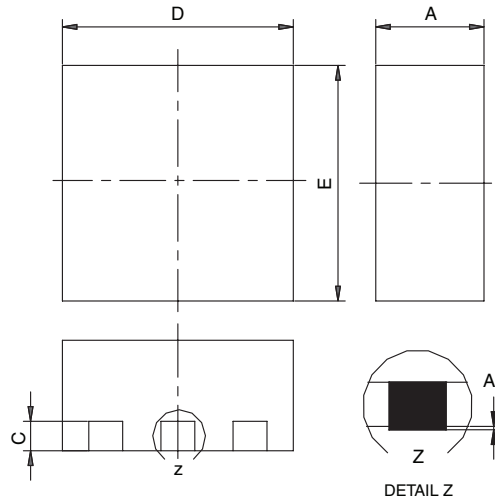
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## PowerPAK® SC75-6L



BACKSIDE VIEW OF SINGLE

BACKSIDE VIEW OF DUAL



Notes:

1. All dimensions are in millimeters
2. Package outline exclusive of mold flash and metal burr
3. Package outline inclusive of plating

DIM	SINGLE PAD						DUAL PAD					
	MILLIMETERS			INCHES			MILLIMETERS			INCHES		
	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max
A	0.675	0.75	0.80	0.027	0.030	0.032	0.675	0.75	0.80	0.027	0.030	0.032
A1	0	-	0.05	0	-	0.002	0	-	0.05	0	-	0.002
b	0.18	0.25	0.33	0.007	0.010	0.013	0.18	0.25	0.33	0.007	0.010	0.013
C	0.15	0.20	0.25	0.006	0.008	0.010	0.15	0.20	0.25	0.006	0.008	0.010
D	1.53	1.60	1.70	0.060	0.063	0.067	1.53	1.60	1.70	0.060	0.063	0.067
D1	0.57	0.67	0.77	0.022	0.026	0.030	0.34	0.44	0.54	0.013	0.017	0.021
D2	0.10	0.20	0.30	0.004	0.008	0.012						
E	1.53	1.60	1.70	0.060	0.063	0.067	1.53	1.60	1.70	0.060	0.063	0.067
E1	1.00	1.10	1.20	0.039	0.043	0.047	0.51	0.61	0.71	0.020	0.024	0.028
E2	0.20	0.25	0.30	0.008	0.010	0.012						
E3	0.32	0.37	0.42	0.013	0.015	0.017						
e	0.50 BSC			0.020 BSC			0.50 BSC			0.020 BSC		
K	0.180 TYP			0.007 TYP			0.245 TYP			0.010 TYP		
K1	0.275 TYP			0.011 TYP			0.320 TYP			0.013 TYP		
K2	0.200 TYP			0.008 TYP			0.200 BSC			0.008 TYP		
K3	0.255 TYP			0.010 TYP								
K4	0.300 TYP			0.012 TYP								
L	0.15	0.25	0.35	0.006	0.010	0.014	0.15	0.25	0.35	0.006	0.010	0.014
T							0.03	0.08	0.13	0.001	0.003	0.005

ECN: C-07431 – Rev. C, 06-Aug-07

DWG: 5935

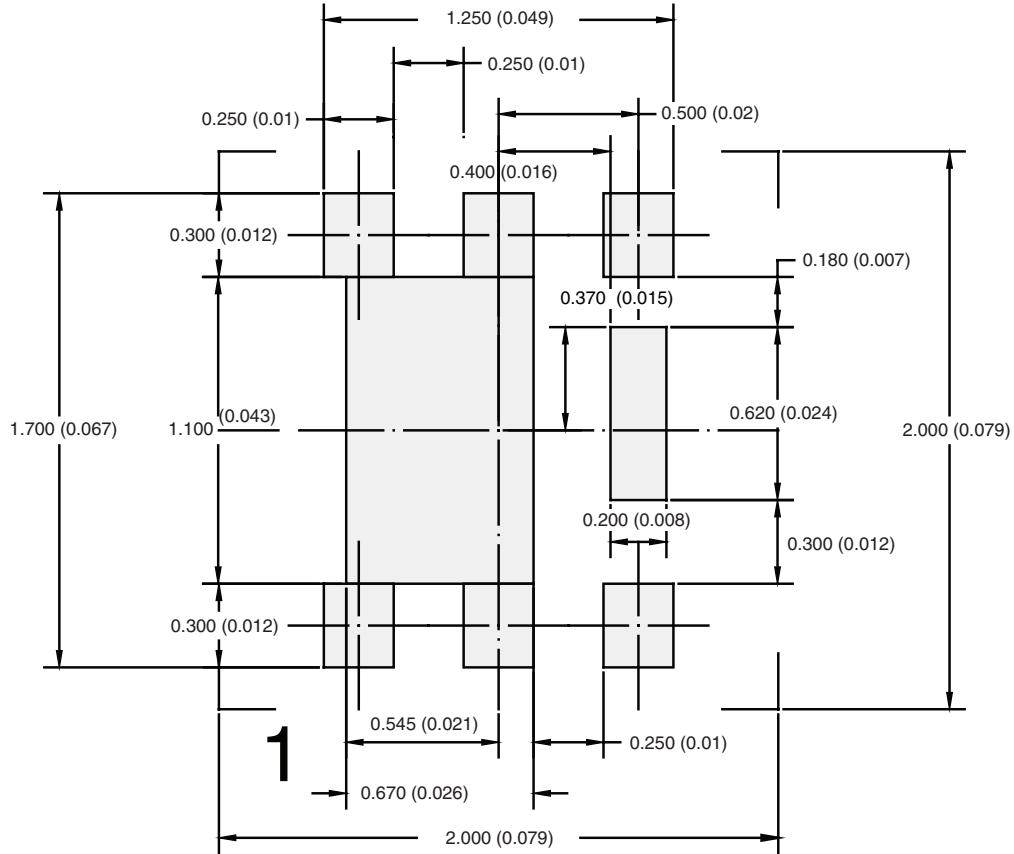




**Application Note 826**

Vishay Siliconix

**RECOMMENDED PAD LAYOUT FOR PowerPAK® SC75-6L Single**



Dimensions in mm/(Inches)

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APPLICATION NOTE



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