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Vishay/Siliconix
SUD50N02-04P-E3

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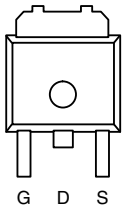
sales@integrated-circuit.com

N-Channel 20 V (D-S) 175 °C MOSFET

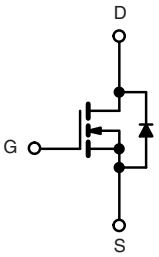
PRODUCT SUMMARY		
V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)[a]
20	0.0043 at V_{GS} = 10 V	34
	0.006 at V_{GS} = 4.5 V	28

TO-252



Drain Connected to Tab

Top View



N-Channel MOSFET

Ordering Information:
SUD50N02-04P-E3 (Lead (Pb)-free)

FEATURES

- TrenchFET® Power MOSFET
- 175 °C Junction Temperature
- PWM Optimized for High Efficiency
- Material categorization:
  For definitions of compliance please see www.vishay.com/doc?99912

RoHS COMPLIANT

APPLICATIONS

- Synchronous Buck Converter
  - Low-Side
  - Desktop, Servers, Desknote
- Synchronous Rectification
  - POL

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)				
Parameter		**Symbol**	**Limit**	**Unit**
Drain-Source Voltage		V_{DS}	20	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current[a]	T_A = 25 °C	I_D	34[a]	A
	T_C = 25 °C		50[b]	
Pulsed Drain Current		I_{DM}	100	
Continuous Source Current (Diode Conduction)[a]		I_S	8.3[a]	
Avalanche Current[c]	L = 0.1 mH	I_{AS}	50	
Avalanche Energy[c]		E_{AS}	125	mJ
Maximum Power Dissipation	T_A = 25 °C	P_D	8.3[a]	W
	T_C = 25 °C		136	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 55 to 175	°C

THERMAL RESISTANCE RATINGS					
Parameter		**Symbol**	**Typical**	**Maximum**	**Unit**
Maximum Junction-to-Ambient[a]	t ≤ 10 s	R_{thJA}	15	18	°C/W
	Steady State		40	50	
Maximum Junction-to-Case		R_{thJC}	0.85	1.1	

Notes:
a. Surface mounted on FR4 board, t ≤ 10 s.
b. Limited by package.
c. Single pulse.

SUD50N02-04P

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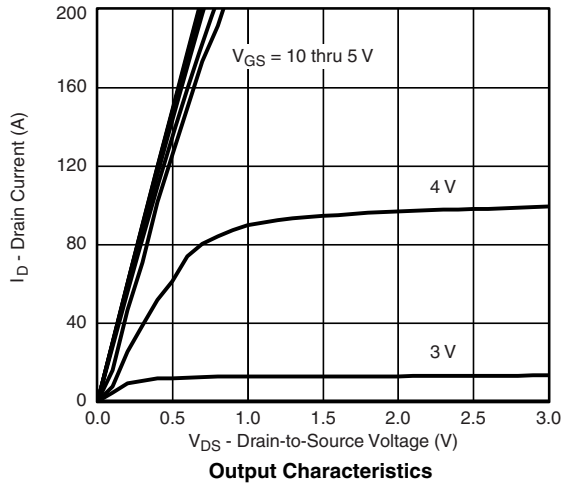
SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)

Parameter	Symbol	Test Conditions	Min.	Typ.[a]	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA	20			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	0.8		3.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 20 V, V_{GS} = 0 V			1	µA
		V_{DS} = 20 V, V_{GS} = 0 V, T_J = 125 °C			50	
On-State Drain Current[b]	$I_{D(on)}$	V_{DS} = 5 V, V_{GS} = 10 V	50			A
Drain-Source On-State Resistance[b]	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 20 A		0.0035	0.0043	Ω
		V_{GS} = 10 V, I_D = 20 A, T_J = 125 °C			0.0061	
		V_{GS} = 4.5 V, I_D = 20 A		0.0048	0.006	
Forward Transconductance[b]	g_{fs}	V_{DS} = 15 V, I_D = 20 A	15			S
Dynamic[a]						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 10 V, f = 1 MHz		5000		pF
Output Capacitance	C_{oss}			1650		
Reverse Transfer Capacitance	C_{rss}			770		
Gate Resistance	R_g	f = 1 MHz		1.6		Ω
Total Gate Charge[c]	Q_g	V_{DS} = 10 V, V_{GS} = 4.5 V, I_D = 50 A		40	60	nC
Gate-Source Charge[c]	Q_{gs}			14		
Gate-Drain Charge[c]	Q_{gd}			13		
Turn-On Delay Time[c]	$t_{d(on)}$	V_{DD} = 10 V, R_L = 0.2 Ω I_D ≅ 50 A, V_{GEN} = 10 V, R_g = 2.5 Ω		20	30	ns
Rise Time[c]	t_r			20	30	
Turn-Off Delay Time[c]	$t_{d(off)}$			50	75	
Fall Time[c]	t_f			15	25	
Source-Drain Diode Ratings and Characteristics	T_C = 25 °C					
Pulsed Current	I_{SM}				100	A
Diode Forward Voltage[b]	V_{SD}	I_F = 50 A, V_{GS} = 0 V		0.9	1.5	V
Source-Drain Reverse Recovery Time	t_{rr}	I_F = 50 A, dI/dt = 100 A/µs		45	70	ns

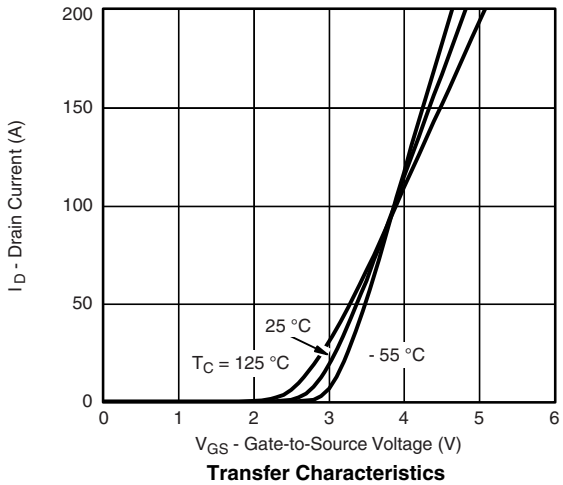
Notes:
a. Guaranteed by design, not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.
c. Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

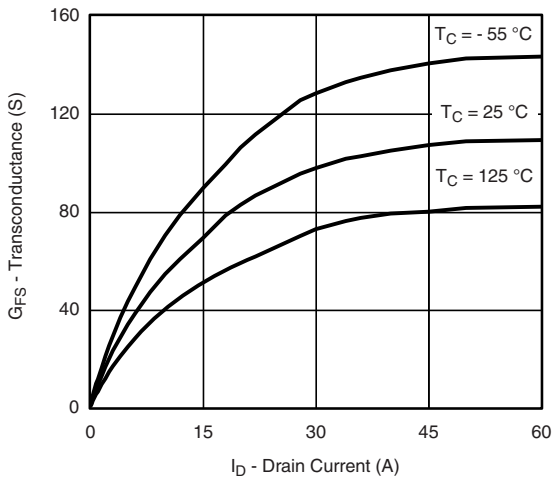


Output Characteristics

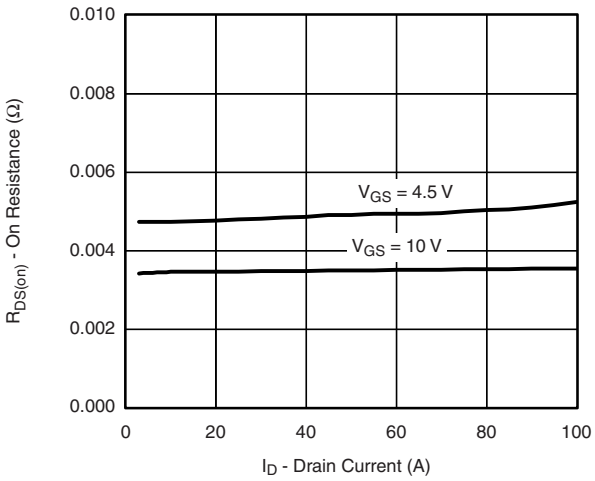


Transfer Characteristics

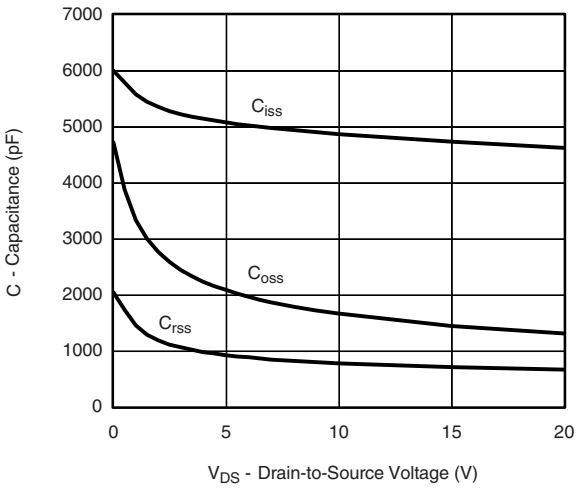
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



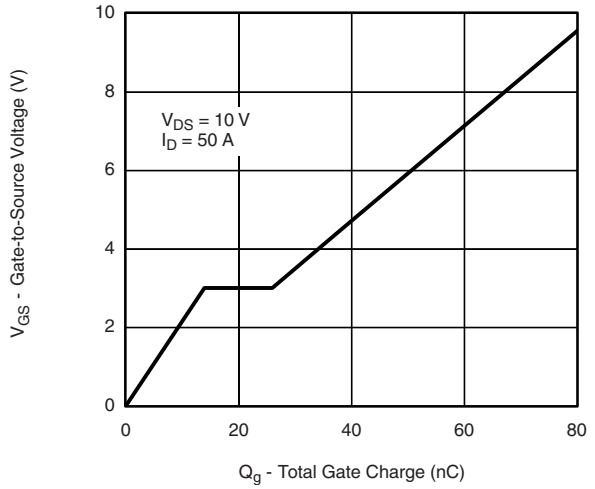
Transconductance



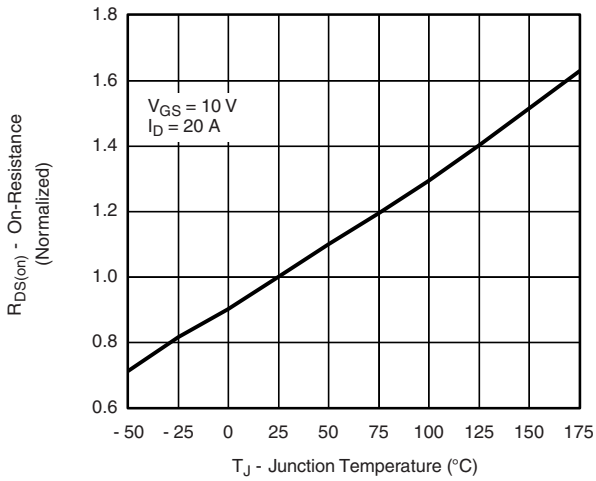
On-Resistance vs. Drain Current



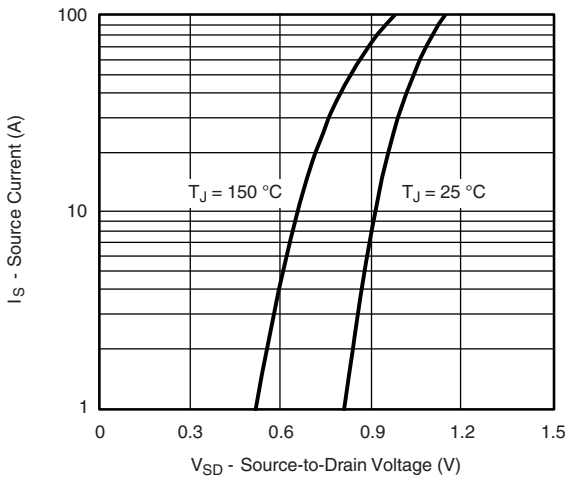
Capacitance



Gate Charge



On-Resistance vs. Junction Temperature



Source-Drain Diode Forward Voltage

SUD50N02-04P

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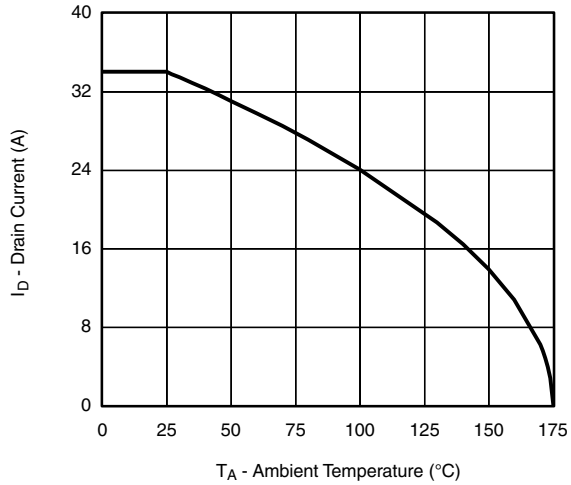
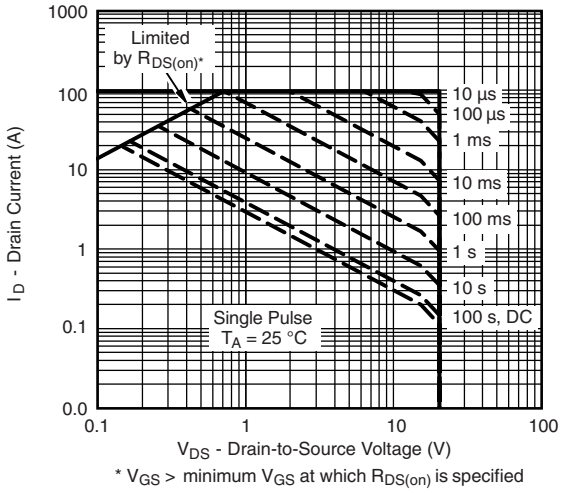
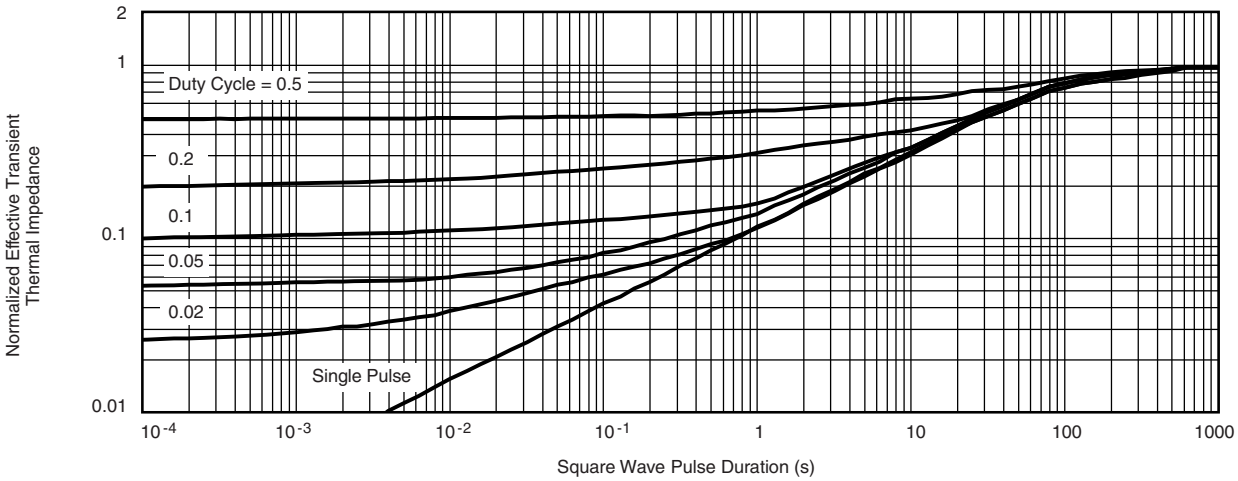
THERMAL RATINGS



Max. Avalanche and Drain Current vs. Ambient Temperature



Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Ambient

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