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[SUM90N10-8M2P-E3](#)

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**SUM90N10-8m2P**

Vishay Siliconix

**N Channel 100 V (D-S) MOSFET**

PRODUCT SUMMARY			
V <sub>(BR)DSS</sub> (V)	R <sub>DS(on)</sub> (Ω)	I <sub>D</sub> (A)	Q <sub>g</sub> (Typ)
100	0.0082 at V <sub>GS</sub> = 10 V	90 <sup>d</sup>	97

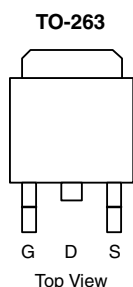
**FEATURES**

- TrenchFET<sup>®</sup> Power MOSFETS
- 175 °C Junction Temperature
- 100 % R<sub>g</sub> and UIS Tested
- Compliant to RoHS Directive 2002/95/EC

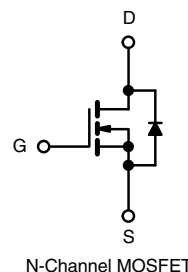


**APPLICATIONS**

- Power Supply  
- Secondary Synchronous Rectification
- Industrial
- Primary Switch



Ordering Information: SUM90N10-8m2P-E3 (Lead (Pb)-free)



ABSOLUTE MAXIMUM RATINGS (T <sub>C</sub> = 25 °C, unless otherwise noted)				
Parameter	Symbol	Limit	Unit	
Drain-Source Voltage	V <sub>DS</sub>	100	V	
Gate-Source Voltage	V <sub>GS</sub>	± 20		
Continuous Drain Current (T <sub>J</sub> = 175 °C)	I <sub>D</sub>	T <sub>C</sub> = 25 °C	90 <sup>d</sup>	A
		T <sub>C</sub> = 70 °C	90 <sup>d</sup>	
Pulsed Drain Current	I <sub>DM</sub>	240		
Avalanche Current	I <sub>AS</sub>	60		
Single Avalanche Energy <sup>a</sup>	E <sub>AS</sub>	180	mJ	
Maximum Power Dissipation <sup>a</sup>	P <sub>D</sub>	T <sub>C</sub> = 25 °C	300 <sup>b</sup>	W
		T <sub>A</sub> = 25 °C <sup>c</sup>	3.75	
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	- 55 to 175	°C	

THERMAL RESISTANCE RATINGS			
Parameter	Symbol	Limit	Unit
Junction-to-Ambient (PCB Mount) <sup>c</sup>	R <sub>thJA</sub>	40	°C/W
Junction-to-Case (Drain)	R <sub>thJC</sub>	0.5	

Notes:

- a. Duty cycle ≤ 1 %.
- b. See SOA curve for voltage derating.
- c. When mounted on 1" square PCB (FR-4 material).
- d. Package limited.

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SPECIFICATIONS (T <sub>J</sub> = 25 °C, unless otherwise noted)						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	V <sub>DS</sub> = 0 V, I <sub>D</sub> = 250 μA	100			V
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	2.5		4.5	
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ± 20 V			± 250	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 100 V, V <sub>GS</sub> = 0 V			1	μA
		V <sub>DS</sub> = 100 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 125 °C			50	
		V <sub>DS</sub> = 100 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 150 °C			250	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> ≥ 10 V, V <sub>GS</sub> = 10 V	70			A
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 20 A		0.0067	0.0082	Ω
		V <sub>GS</sub> = 10 V, I <sub>D</sub> = 20 A, T <sub>J</sub> = 125 °C		0.0127	0.0170	
Forward Transconductance <sup>a</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 20 A		62		S
<b>Dynamic<sup>b</sup></b>						
Input Capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 50 V, f = 1 MHz		6290		pF
Output Capacitance	C <sub>oss</sub>			535		
Reverse Transfer Capacitance	C <sub>rss</sub>			182		
Total Gate Charge <sup>c</sup>	Q <sub>g</sub>	V <sub>DS</sub> = 50 V, V <sub>GS</sub> = 10 V, I <sub>D</sub> = 85 A		97	150	nC
Gate-Source Charge <sup>c</sup>	Q <sub>gs</sub>			32		
Gate-Drain Charge <sup>c</sup>	Q <sub>gd</sub>			25		
Gate Resistance	R <sub>g</sub>	f = 1 MHz	0.28	1.4	2.8	Ω
Turn-On Delay Time <sup>c</sup>	t <sub>d(on)</sub>	V <sub>DD</sub> = 50 V, R <sub>L</sub> = 0.588 Ω I <sub>D</sub> ≅ 85 A, V <sub>GEN</sub> = 10 V, R <sub>g</sub> = 1 Ω		23	35	ns
Rise Time <sup>c</sup>	t <sub>r</sub>			17	26	
Turn-Off Delay Time <sup>c</sup>	t <sub>d(off)</sub>			34	52	
Fall Time <sup>c</sup>	t <sub>f</sub>			9	18	
<b>Source-Drain Diode Ratings and Characteristics (T<sub>C</sub> = 25 °C)<sup>b</sup></b>						
Continuous Current	I <sub>S</sub>				85	A
Pulsed Current	I <sub>SM</sub>				240	
Forward Voltage <sup>a</sup>	V <sub>SD</sub>	I <sub>F</sub> = 30 A, V <sub>GS</sub> = 0 V		0.85	1.5	V
Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = 75 A, di/dt = 100 A/μs		61	100	ns
Peak Reverse Recovery Current	I <sub>RM(REC)</sub>			3	4.5	A
Reverse Recovery Charge	Q <sub>rr</sub>			91	130	μC

Notes:

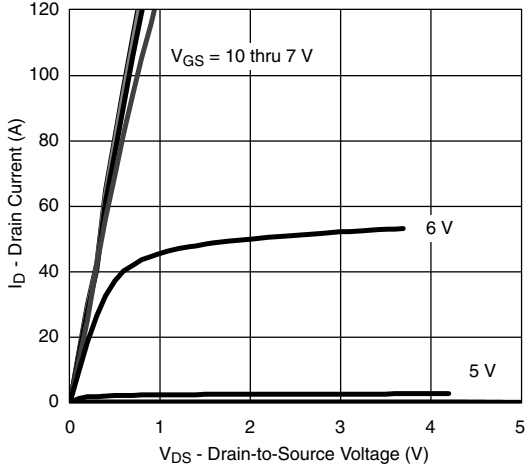
- Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %.
- Guaranteed by design, not subject to production testing.
- Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

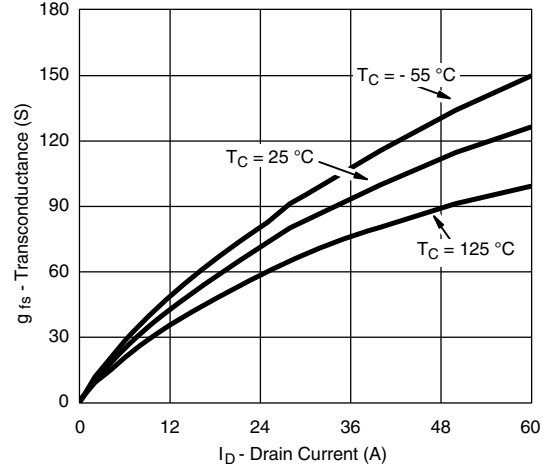


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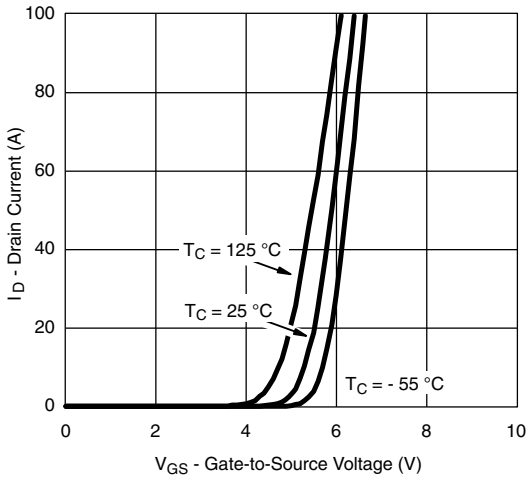
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



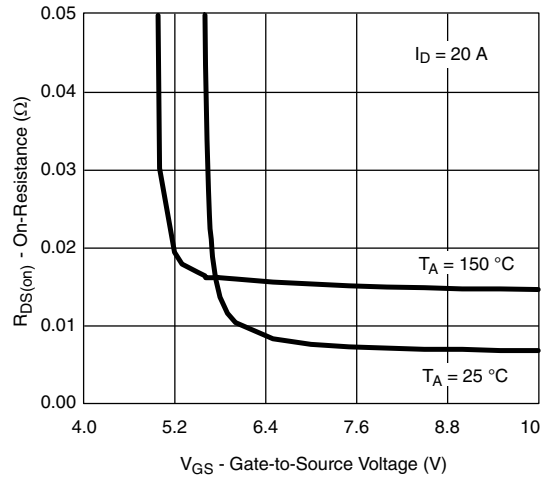
**Output Characteristics**



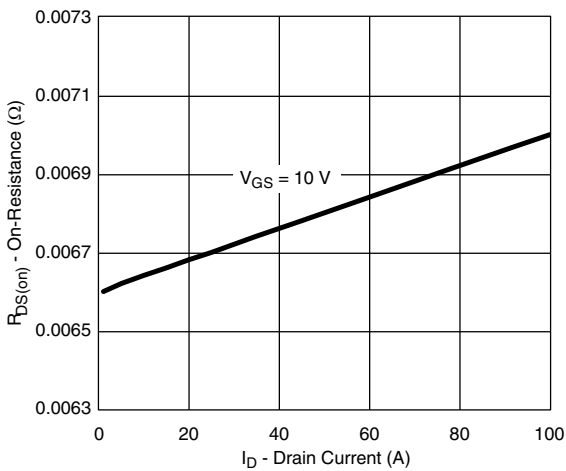
**Transconductance**



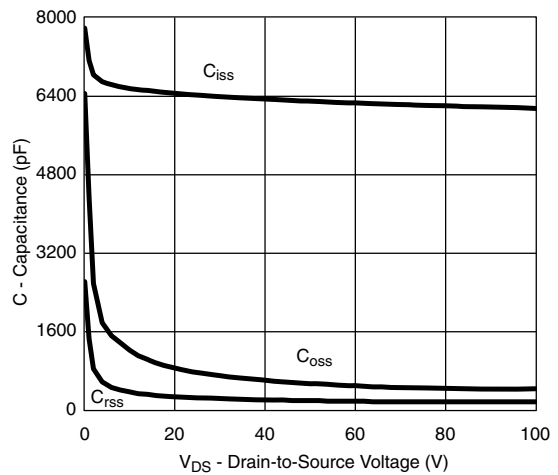
**Transfer Characteristics**



**On-resistance vs. Gate-to-Source Voltage**



**On-Resistance vs. Drain Current**



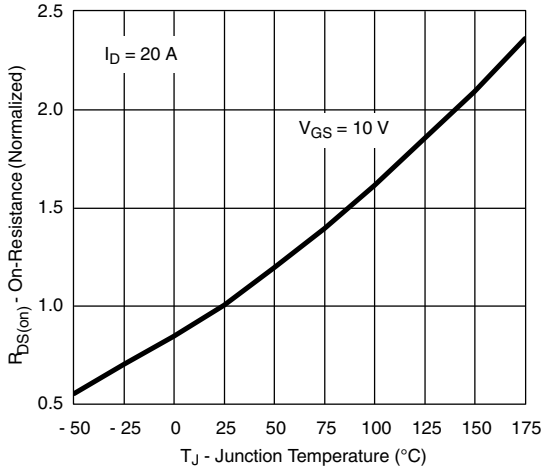
**Capacitance**



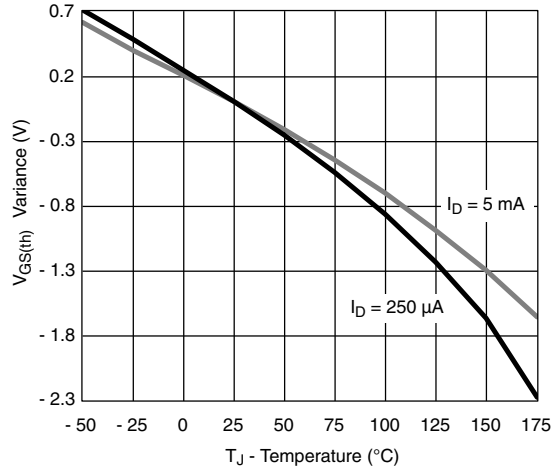
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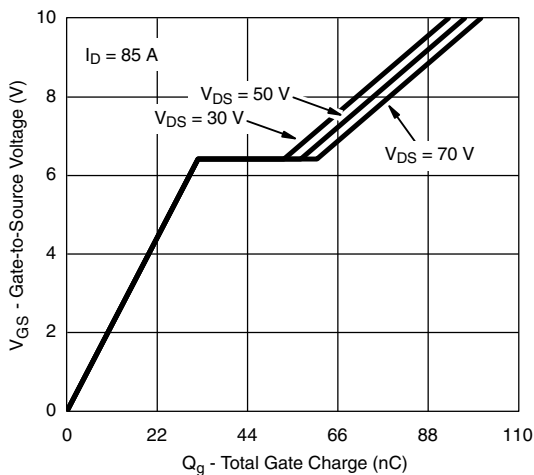
## TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



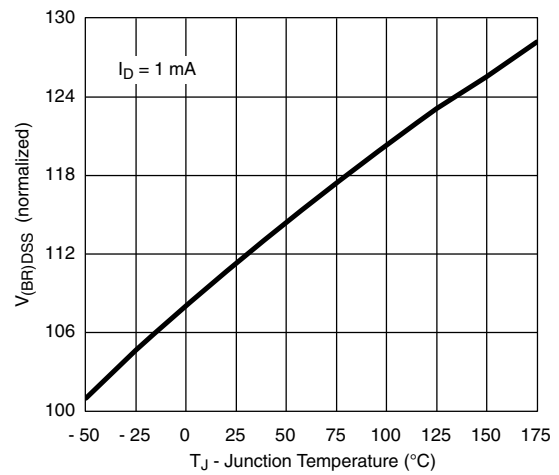
**On-Resistance vs. Junction Temperature**



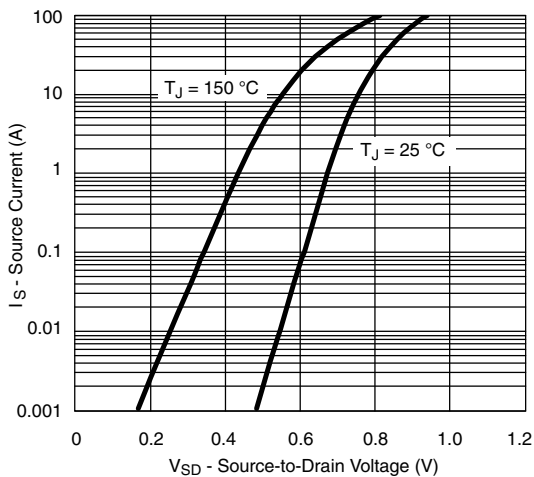
**Threshold Voltage**



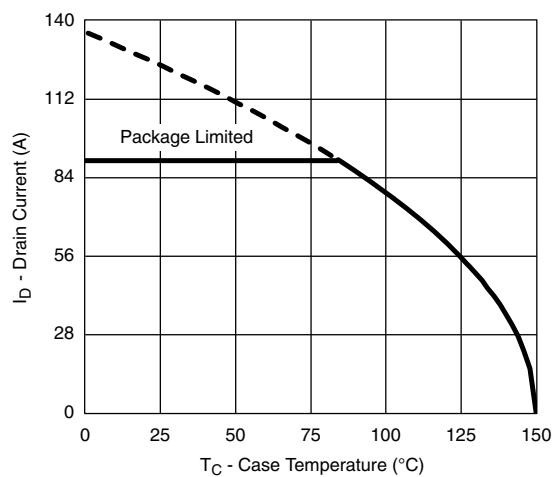
**Gate Charge**



**Drain Source Breakdown vs. Junction Temperature**



**Source-Drain Diode Forward Voltage**

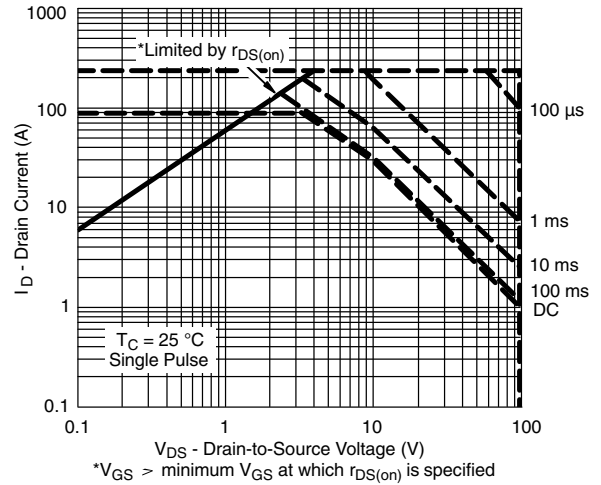
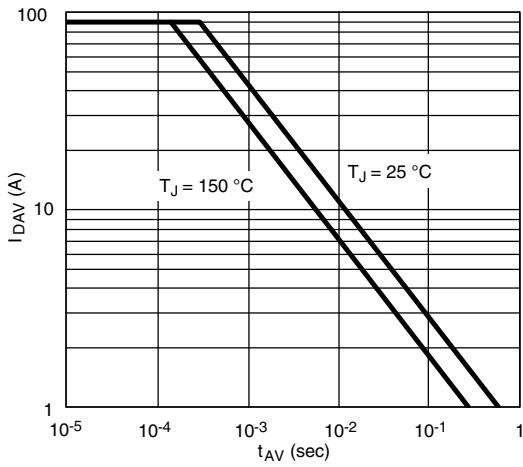


**Maximum Drain Current vs. Case Temperature**



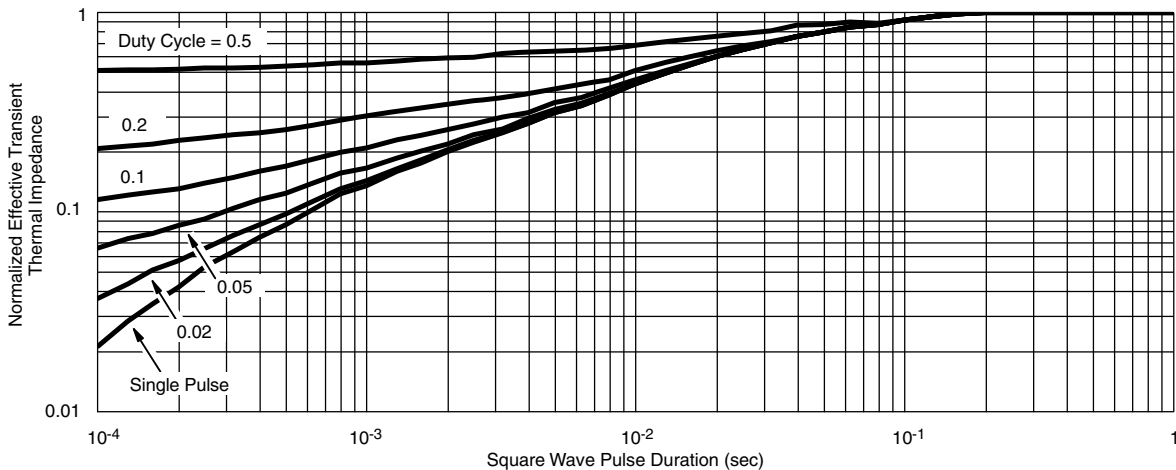
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**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



Single Pulse Avalanche Current Capability vs. Time

Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Case

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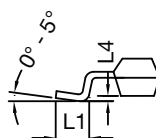
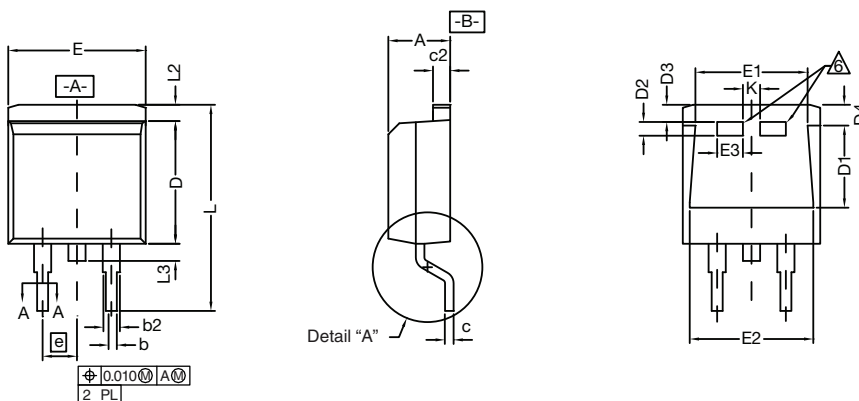


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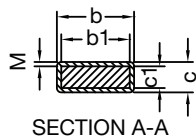
## Package Information

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### TO-263 (D<sup>2</sup>PAK): 3-LEAD



DETAIL A (ROTATED 90°)



SECTION A-A

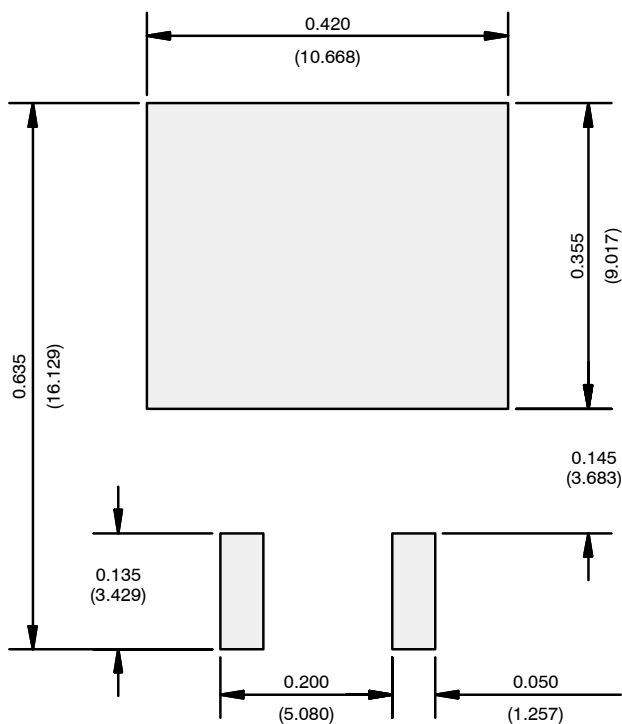
DIM.	INCHES		MILLIMETERS		
	MIN.	MAX.	MIN.	MAX.	
A	0.160	0.190	4.064	4.826	
b	0.020	0.039	0.508	0.990	
b1	0.020	0.035	0.508	0.889	
b2	0.045	0.055	1.143	1.397	
c*	Thin lead	0.013	0.018	0.330	0.457
	Thick lead	0.023	0.028	0.584	0.711
c1	Thin lead	0.013	0.017	0.330	0.431
	Thick lead	0.023	0.027	0.584	0.685
c2	0.045	0.055	1.143	1.397	
D	0.340	0.380	8.636	9.652	
D1	0.220	0.240	5.588	6.096	
D2	0.038	0.042	0.965	1.067	
D3	0.045	0.055	1.143	1.397	
D4	0.044	0.052	1.118	1.321	
E	0.380	0.410	9.652	10.414	
E1	0.245	-	6.223	-	
E2	0.355	0.375	9.017	9.525	
E3	0.072	0.078	1.829	1.981	
e	0.100 BSC		2.54 BSC		
K	0.045	0.055	1.143	1.397	
L	0.575	0.625	14.605	15.875	
L1	0.090	0.110	2.286	2.794	
L2	0.040	0.055	1.016	1.397	
L3	0.050	0.070	1.270	1.778	
L4	0.010 BSC		0.254 BSC		
M	-	0.002	-	0.050	
ECN: T13-0707-Rev. K, 30-Sep-13					
DWG: 5843					

#### Notes

- Plane B includes maximum features of heat sink tab and plastic.
- No more than 25 % of L1 can fall above seating plane by max. 8 mils.
- Pin-to-pin coplanarity max. 4 mils.
- \*: Thin lead is for SUB, SYB.  
Thick lead is for SUM, SYM, SQM.
- Use inches as the primary measurement.
- This feature is for thick lead.



**RECOMMENDED MINIMUM PADS FOR D<sup>2</sup>PAK: 3-Lead**



Recommended Minimum Pads  
Dimensions in Inches/(mm)

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