



## FDC3535

### P-Channel Power Trench® MOSFET -80 V, -2.1 A, 183 mΩ



#### Features

- Max  $r_{DS(on)}$  = 183 mΩ at  $V_{GS} = -10$  V,  $I_D = -2.1$  A
- Max  $r_{DS(on)}$  = 233 mΩ at  $V_{GS} = -4.5$  V,  $I_D = -1.9$  A
- High performance trench technology for extremely low  $r_{DS(on)}$
- High power and current handling capability in a widely used surface mount package
- Fast switching speed
- 100% UIL Tested
- RoHS Compliant

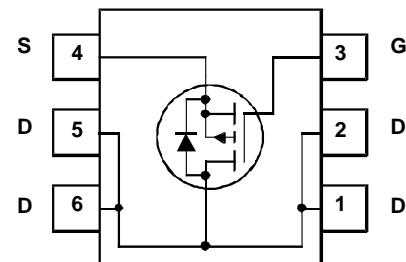
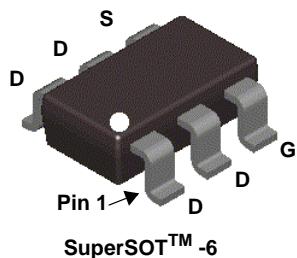


#### General Description

This P-Channel MOSFET is produced using Fairchild Semiconductor's advanced Power Trench® process that has been optimized for  $r_{DS(on)}$ , switching performance and ruggedness.

#### Applications

- Load Switch
- Synchronous Rectifier



#### MOSFET Maximum Ratings $T_A = 25$ °C unless otherwise noted

Symbol	Parameter	Ratings	Units
$V_{DS}$	Drain to Source Voltage	-80	V
$V_{GS}$	Gate to Source Voltage	$\pm 20$	V
$I_D$	Drain Current -Continuous	(Note 1a)	A
	-Pulsed	-10	
$E_{AS}$	Single Pulse Avalanche Energy	(Note 3)	mJ
$P_D$	Power Dissipation	(Note 1a)	W
	Power Dissipation	(Note 1b)	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	°C

#### Thermal Characteristics

$R_{0JC}$	Thermal Resistance, Junction to Case	30	
$R_{0JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	78 °C/W

#### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
.535	FDC3535	SSOT-6	7 "	8 mm	3000 units

**Electrical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
<b>Off Characteristics</b>						
$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = -250 \mu\text{A}$ , $V_{GS} = 0 \text{ V}$	-80			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = -250 \mu\text{A}$ , referenced to $25^\circ\text{C}$		-64		$\text{mV/}^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = -64 \text{ V}$ , $V_{GS} = 0 \text{ V}$			-1	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 20 \text{ V}$ , $V_{DS} = 0 \text{ V}$			$\pm 100$	nA

**On Characteristics**

$V_{GS(\text{th})}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$ , $I_D = -250 \mu\text{A}$	-1	-1.6	-3	V
$\frac{\Delta V_{GS(\text{th})}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = -250 \mu\text{A}$ , referenced to $25^\circ\text{C}$		5		$\text{mV/}^\circ\text{C}$
$r_{DS(\text{on})}$	Static Drain to Source On Resistance	$V_{GS} = -10 \text{ V}$ , $I_D = -2.1 \text{ A}$		147	183	$\text{m}\Omega$
		$V_{GS} = -4.5 \text{ V}$ , $I_D = -1.9 \text{ A}$		176	233	
		$V_{GS} = -10 \text{ V}$ , $I_D = -2.1 \text{ A}$ , $T_J = 125^\circ\text{C}$		246	307	
$g_{FS}$	Forward Transconductance	$V_{DD} = -10 \text{ V}$ , $I_D = -2.1 \text{ A}$		6.3		S

**Dynamic Characteristics**

$C_{iss}$	Input Capacitance	$V_{DS} = -40 \text{ V}$ , $V_{GS} = 0 \text{ V}$ , $f = 1 \text{ MHz}$		659	880	pF
$C_{oss}$	Output Capacitance			49	65	pF
$C_{rss}$	Reverse Transfer Capacitance			24	40	pF
$R_g$	Gate Resistance			5.7		$\Omega$

**Switching Characteristics**

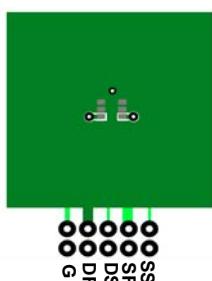
$t_{d(\text{on})}$	Turn-On Delay Time	$V_{DD} = -40 \text{ V}$ , $I_D = -2.1 \text{ A}$ , $V_{GS} = -10 \text{ V}$ , $R_{\text{GEN}} = 6 \Omega$		6.5	13	ns
$t_r$	Rise Time			3.1	10	ns
$t_{d(\text{off})}$	Turn-Off Delay Time			23	38	ns
$t_f$	Fall Time			2.9	10	ns
$Q_{g(\text{TOT})}$	Total Gate Charge	$V_{GS} = 0 \text{ V}$ to $-10 \text{ V}$		14	20	nC
	Total Gate Charge	$V_{GS} = 0 \text{ V}$ to $-4.5 \text{ V}$	$V_{DD} = -40 \text{ V}$ $I_D = -2.1 \text{ A}$	6.8	10	nC
$Q_{gs}$	Total Gate Charge	1.6			nC	
$Q_{gd}$	Gate to Drain "Miller" Charge	2.7			nC	

**Drain-Source Diode Characteristics**

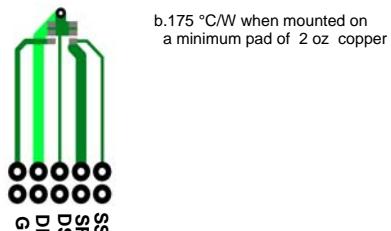
$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0 \text{ V}$ , $I_S = -2.1 \text{ A}$	(Note 2)		-0.81	-1.3	V
$t_{rr}$	Reverse Recovery Time	$I_F = -2.1 \text{ A}$ , $di/dt = 100 \text{ A}/\mu\text{s}$			25	40	ns
$Q_{rr}$	Reverse Recovery Charge				23	38	nC

NOTES:

1.  $R_{\thetaJA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\thetaJC}$  is guaranteed by design while  $R_{\thetaCA}$  is determined by the user's board design.



a.  $78^\circ\text{C}/\text{W}$  when mounted on  
a  $1 \text{ in}^2$  pad of 2 oz copper



b.  $175^\circ\text{C}/\text{W}$  when mounted on  
a minimum pad of 2 oz copper

2. Pulse Test: Pulse Width  $< 300 \mu\text{s}$ , Duty cycle  $< 2.0\%$ .

3. Starting  $T_J = 25^\circ\text{C}$ ,  $L = 3 \text{ mH}$ ,  $I_{AS} = -5 \text{ A}$ ,  $V_{DD} = -80 \text{ V}$ ,  $V_{GS} = -10 \text{ V}$ .

**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted

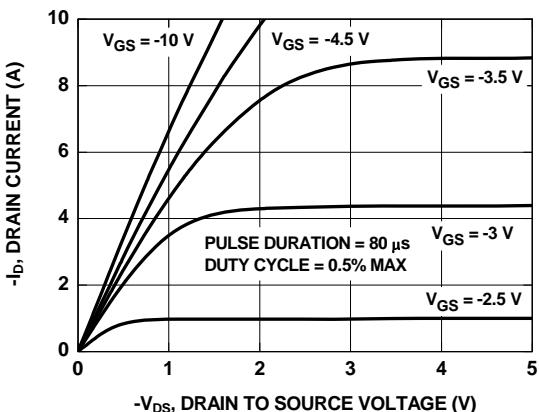


Figure 1. On-Region Characteristics

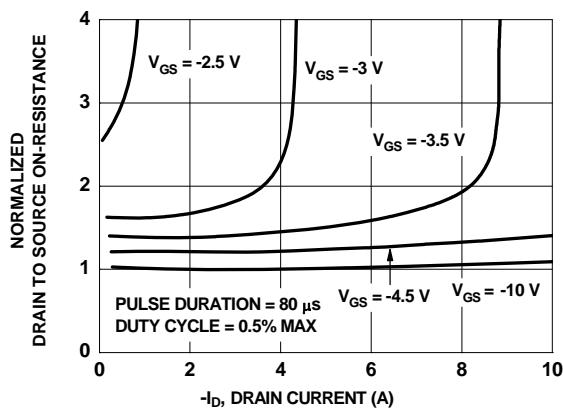


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

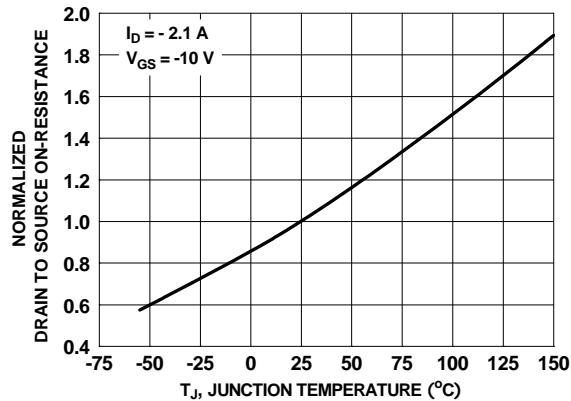


Figure 3. Normalized On-Resistance vs Junction Temperature

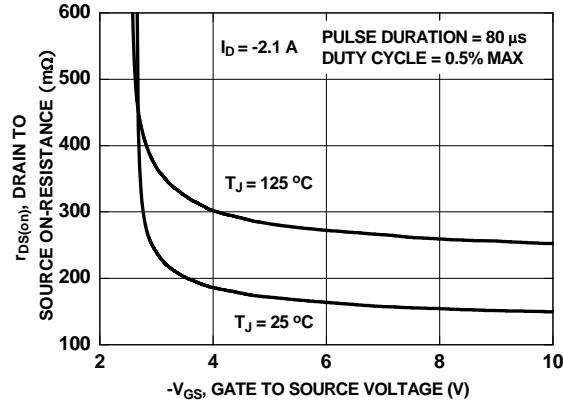


Figure 4. On-Resistance vs Gate to Source Voltage

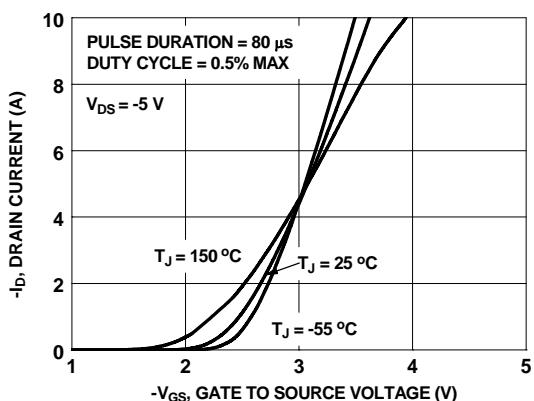


Figure 5. Transfer Characteristics

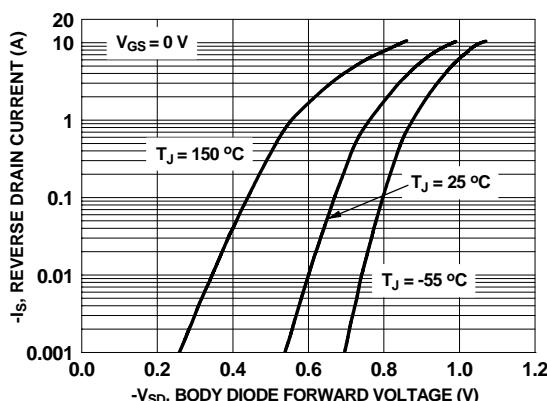


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted

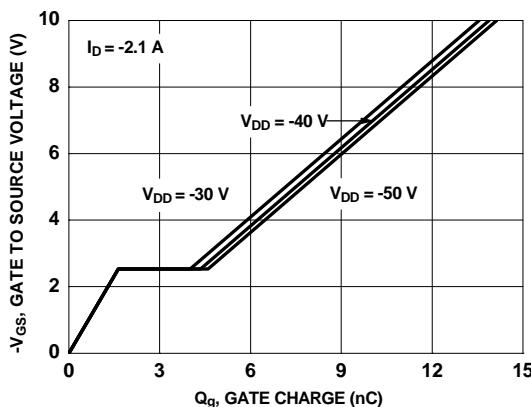


Figure 7. Gate Charge Characteristics

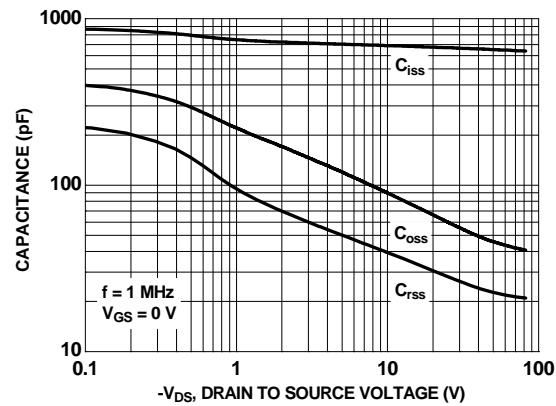


Figure 8. Capacitance vs Drain to Source Voltage

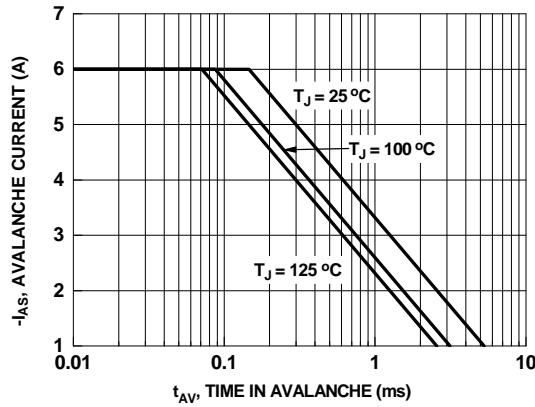


Figure 9. Unclamped Inductive Switching Capability

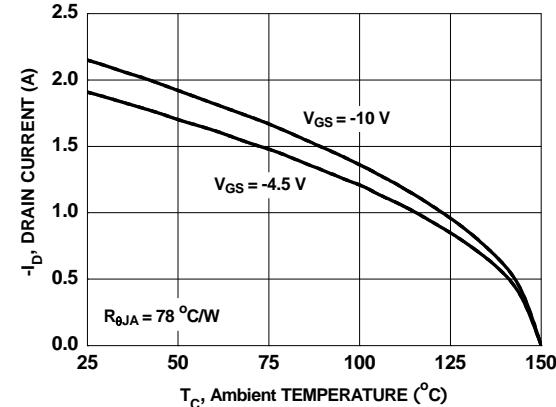


Figure 10. Maximum Continuous Drain Current vs Ambient Temperature

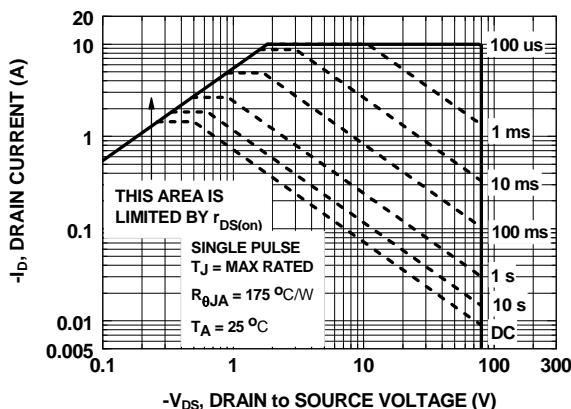


Figure 11. Forward Bias Safe Operating Area

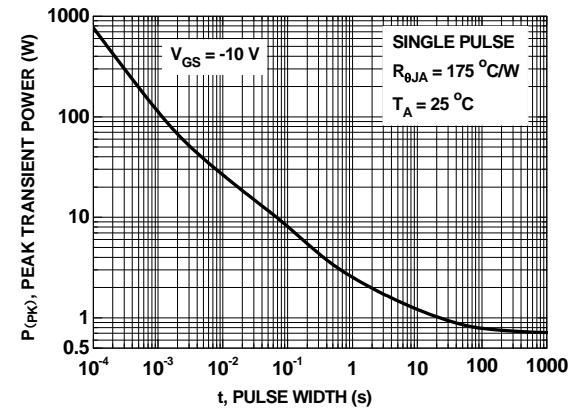
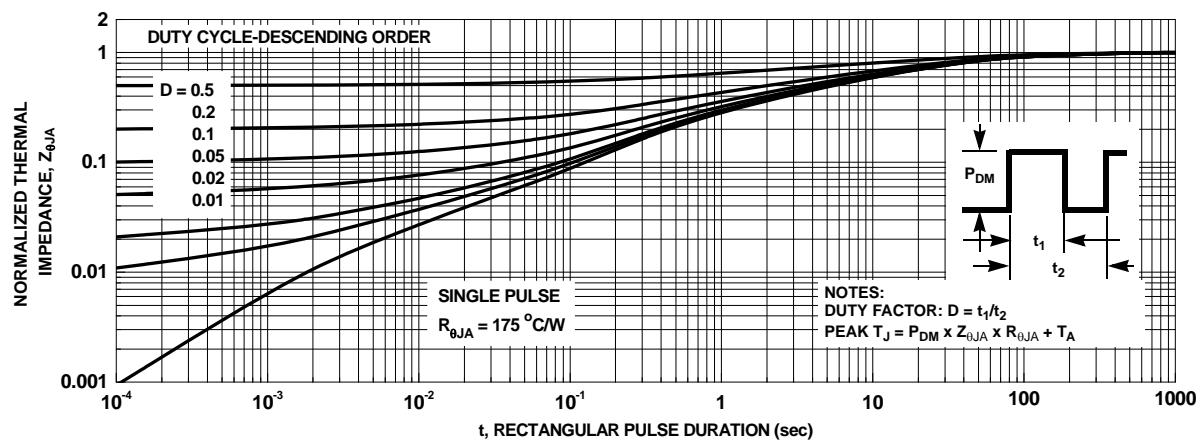
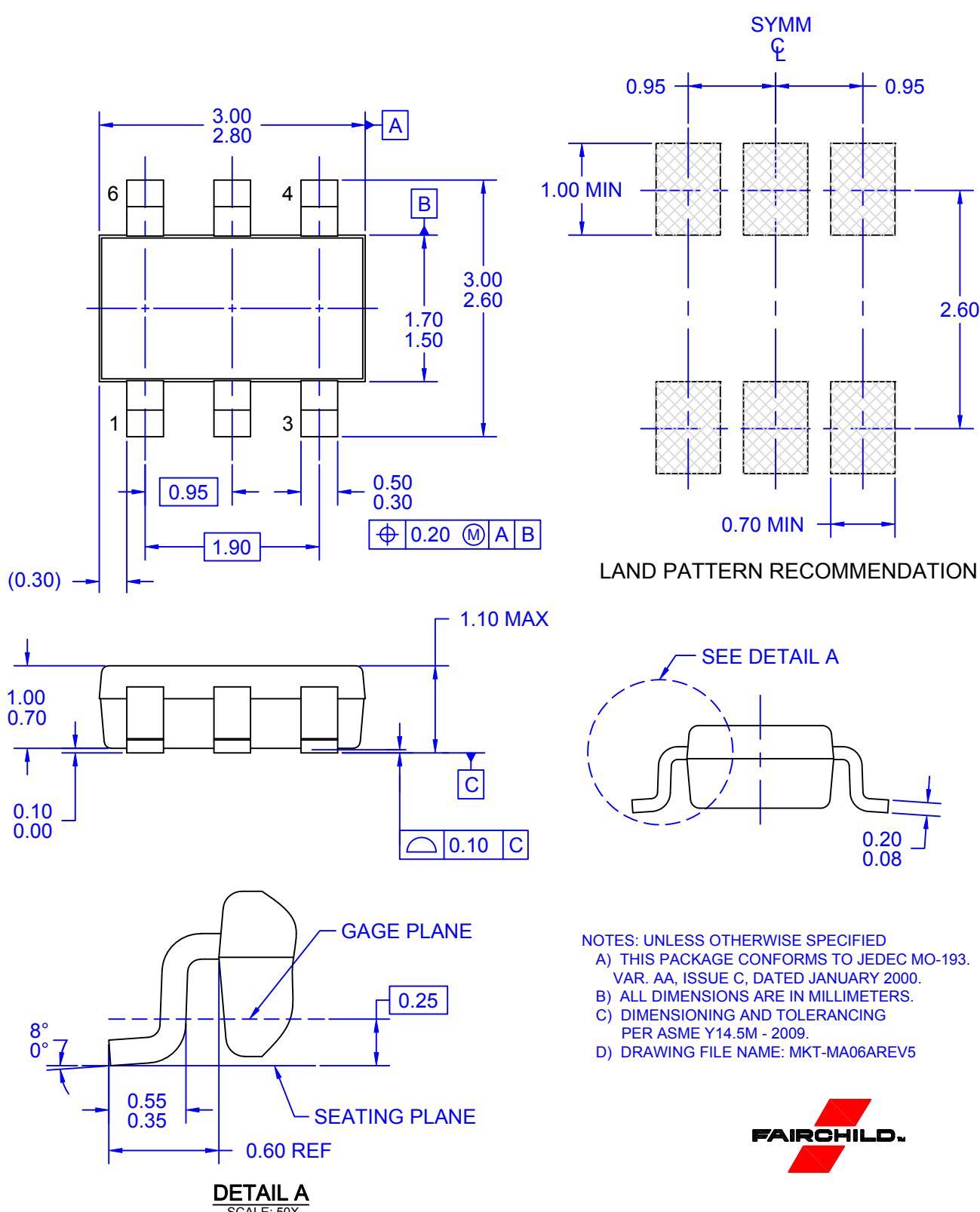


Figure 12. Single Pulse Maximum Power Dissipation

**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted







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