FAIRCHILD

July 2015

FDMC7660DC

N-Channel Dual Cool™ 33 PowerTrench® MOSFET

30 V, 40 A, 2.2 mΩ

Features

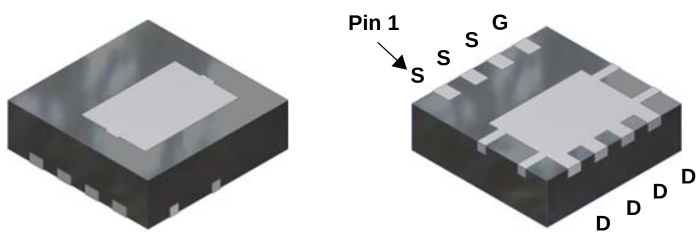
- Dual Cool™ Top Side Cooling PQFN package
- Max $r_{DS(on)}$ = 2.2 mΩ at V_{GS} = 10 V, I_D = 22 A
- Max $r_{DS(on)}$ = 3.3 mΩ at V_{GS} = 4.5 V, I_D = 18 A
- High performance technology for extremely low $r_{DS(on)}$
- SyncFET Schottky Body Diode
- RoHS Compliant

General Description

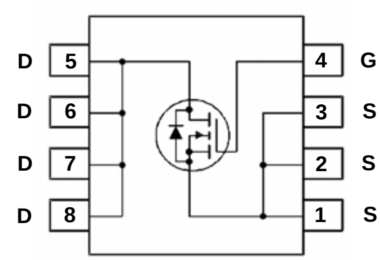
This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench® process. Advancements in both silicon and Dual Cool™ package technologies have been combined to offer the lowest $r_{DS(on)}$ while maintaining excellent switching performance by extremely low Junction-to-Ambient thermal resistance.

Applications

- Synchronous Rectifier for DC/DC Converters
- Telecom Secondary Side Rectification
- High End Server/Workstation



Top Dual Cool™ 33 Bottom



MOSFET Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter			Ratings	Units
V_{DS}	Drain to Source Voltage			30	V
V_{GS}	Gate to Source Voltage		(Note 4)	±20	V
I_D	Drain Current -Continuous (Package limited)	T_C = 25 °C		40	A
	-Continuous (Silicon limited)	T_C = 25 °C		150	
	-Continuous	T_A = 25 °C	(Note 1a)	30	
	-Pulsed			200	
E_{AS}	Single Pulse Avalanche Energy		(Note 3)	220	mJ
dv/dt	Peak Diode Recovery dv/dt		(Note 5)	1.0	V/ns
P_D	Power Dissipation	T_C = 25 °C		78	W
	Power Dissipation	T_A = 25 °C	(Note 1a)	3.0	
T_J, T_{STG}	Operating and Storage Junction Temperature Range			-55 to + 150	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	(Top Source)	4.3	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction to Case	(Bottom Drain)	1.6	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	42	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1b)	105	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1i)	17	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1j)	26	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1k)	12	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
7660	FDMC7660DC	Dual Cool™ 33	13''	12 mm	3000 units

Electrical Characteristics T_J = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units

Off Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V	30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25 °C		15		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 24 V, V_{GS} = 0 V			1	μA
I_{GSS}	Gate to Source Leakage Current, Forward	V_{GS} = 20 V, V_{DS} = 0 V			100	nA

On Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA	1.2	2	2.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25 °C		-7		mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 22 A		1.6	2.2	mΩ
		V_{GS} = 4.5 V, I_D = 18 A		2.5	3.3	
		V_{GS} = 10 V, I_D = 22 A, T_J = 125°C		2.2	3.3	
g_{FS}	Forward Transconductance	V_{DS} = 5 V, I_D = 22 A		147		S

Dynamic Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
C_{iss}	Input Capacitance	V_{DS} = 15 V, V_{GS} = 0 V, f = 1MHz		3885	5170	pF
C_{oss}	Output Capacitance			1215	1620	pF
C_{rss}	Reverse Transfer Capacitance			100	150	pF
R_g	Gate Resistance			0.7	1.5	Ω

Switching Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 15 V, I_D = 22 A, V_{GS} = 10 V, R_{GEN} = 6 Ω		17	31	ns
t_r	Rise Time			6.6	13	ns
$t_{d(off)}$	Turn-Off Delay Time			36	58	ns
t_f	Fall Time			5	10	ns
Q_g	Total Gate Charge	V_{GS} = 0 V to 10 V; V_{DD} = 15 V, I_D = 22 A		54	76	nC
Q_g	Total Gate Charge	V_{GS} = 0 V to 4.5 V; V_{DD} = 15 V, I_D = 22 A		24	34	nC
Q_{gs}	Gate to Source Charge	V_{DD} = 15 V, I_D = 22 A		13		nC
Q_{gd}	Gate to Drain “Miller” Charge			5.5		nC

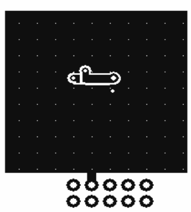
Drain-Source Diode Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
V_{SD}	Source-Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = 22 A (Note 2)		0.8	1.2	V
		V_{GS} = 0 V, I_S = 1.9 A (Note 2)		0.7	1.2	
t_{rr}	Reverse Recovery Time	I_F = 22 A, di/dt = 100 A/μs		43	69	ns
Q_{rr}	Reverse Recovery Charge			24	38	nC

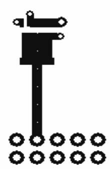
Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case (Top Source)	4.3		°C/W
$R_{\theta JC}$	Thermal Resistance, Junction to Case (Bottom Drain)	1.6		
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	42		
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1b)	105		
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1c)	29		
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1d)	40		
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1e)	19		
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1f)	23		
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1g)	30		
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1h)	79		
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1i)	17		
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1j)	26		
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1k)	12		
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1l)	16		

NOTES:
1. $R_{\theta JA}$ is determined with the device mounted on a FR-4 board using a specified pad of 2 oz copper as shown below. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. 42 °C/W when mounted on a 1 in^2 pad of 2 oz copper



b. 105 °C/W when mounted on a minimum pad of 2 oz copper

c. Still air, 20.9x10.4x12.7mm Aluminum Heat Sink, 1 in^2 pad of 2 oz copper

d. Still air, 20.9x10.4x12.7mm Aluminum Heat Sink, minimum pad of 2 oz copper

e. Still air, 45.2x41.4x11.7mm Aavid Thermalloy Part # 10-L41B-11 Heat Sink, 1 in^2 pad of 2 oz copper

f. Still air, 45.2x41.4x11.7mm Aavid Thermalloy Part # 10-L41B-11 Heat Sink, minimum pad of 2 oz copper

g. 200FPM Airflow, No Heat Sink,1 in^2 pad of 2 oz copper

h. 200FPM Airflow, No Heat Sink, minimum pad of 2 oz copper

i. 200FPM Airflow, 20.9x10.4x12.7mm Aluminum Heat Sink, 1 in^2 pad of 2 oz copper

j. 200FPM Airflow, 20.9x10.4x12.7mm Aluminum Heat Sink, minimum pad of 2 oz copper

k. 200FPM Airflow, 45.2x41.4x11.7mm Aavid Thermalloy Part # 10-L41B-11 Heat Sink, 1 in^2 pad of 2 oz copper

l. 200FPM Airflow, 45.2x41.4x11.7mm Aavid Thermalloy Part # 10-L41B-11 Heat Sink, minimum pad of 2 oz copper

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.
3. E_{AS} of 220 mJ is based on starting T_J = 25 °C; N-ch: L = 1 mH, I_{AS} = 21 A, V_{DD} = 27 V, V_{GS} = 10 V. 100% test at L = 0.3 mH, I_{AS} = 33.5 A.
4. As an N-ch device, the negative Vgs rating is for low duty cycle pulse ocurrence only. No continuous rating is implied.
5. $I_{SD} \le 22$ A, di/dt ≤ 100 A/μs, $V_{DD} \le BV_{DSS}$, Starting T_J = 25 °C.

Typical Characteristics T_J = 25°C unless otherwise noted

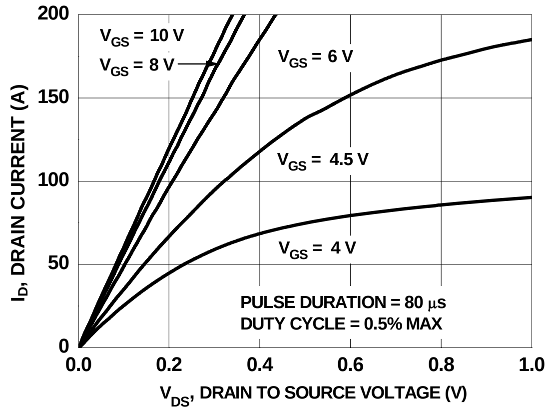


Figure 1. On Region Characteristics

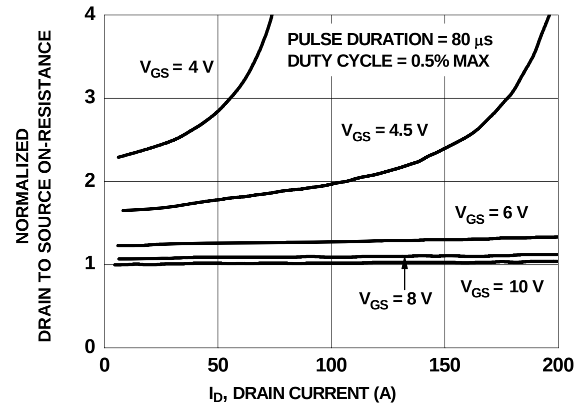


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

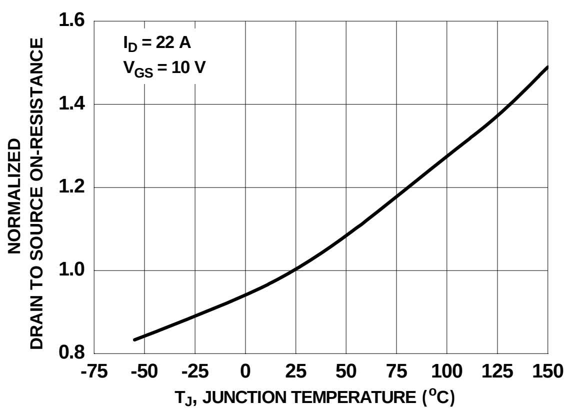


Figure 3. Normalized On Resistance vs Junction Temperature

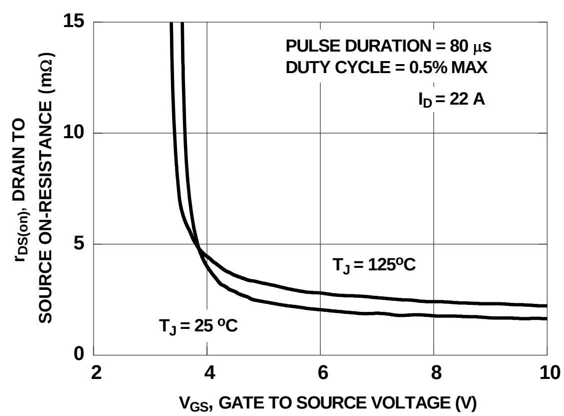


Figure 4. On-Resistance vs Gate to Source Voltage

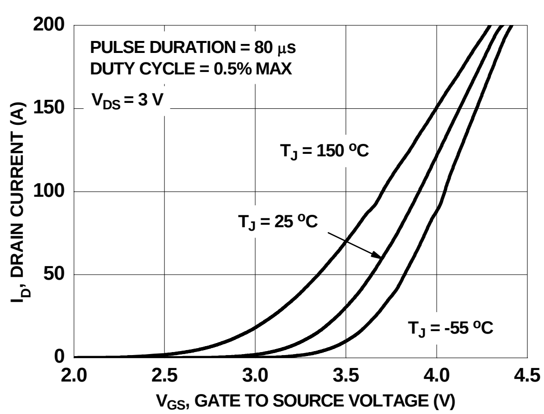


Figure 5. Transfer Characteristics

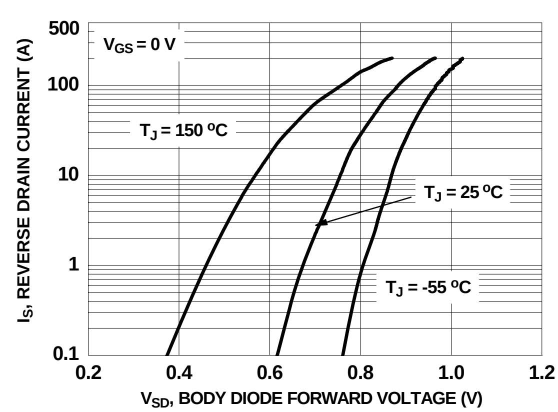


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics T_J = 25°C unless otherwise noted

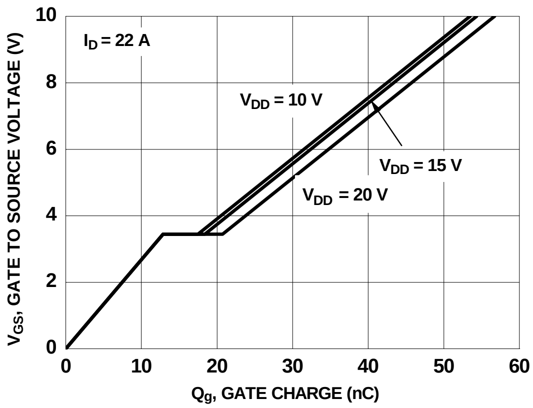


Figure 7. Gate Charge Characteristics

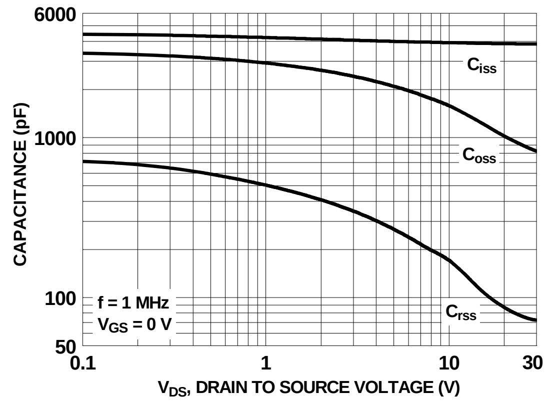


Figure 8. Capacitance vs Drain to Source Voltage

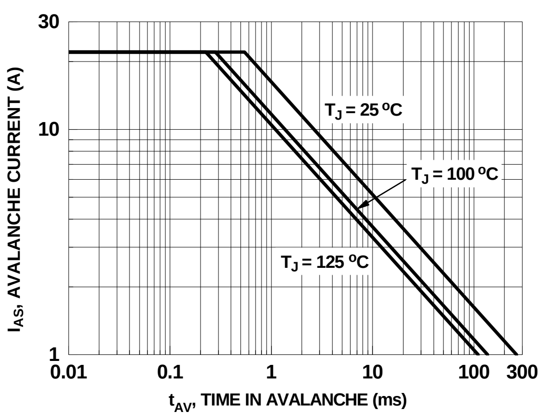


Figure 9. Unclamped Inductive Switching Capability

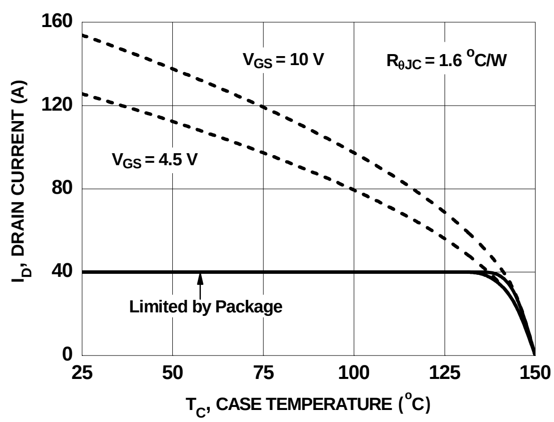


Figure 10. Maximum Continuous Drain Current vs Case Temperature

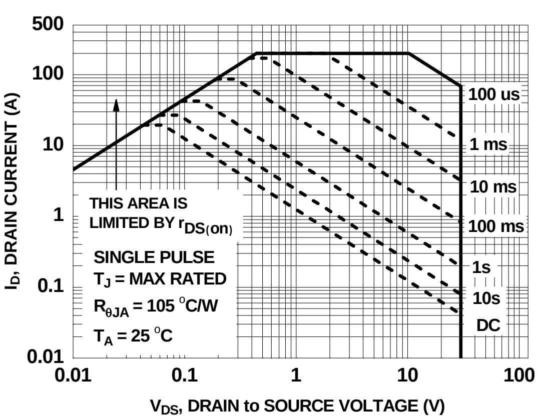


Figure 11. Forward Bias Safe Operating Area

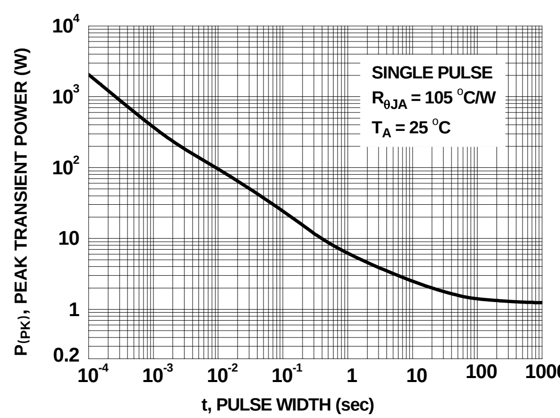


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics T_J = 25°C unless otherwise noted

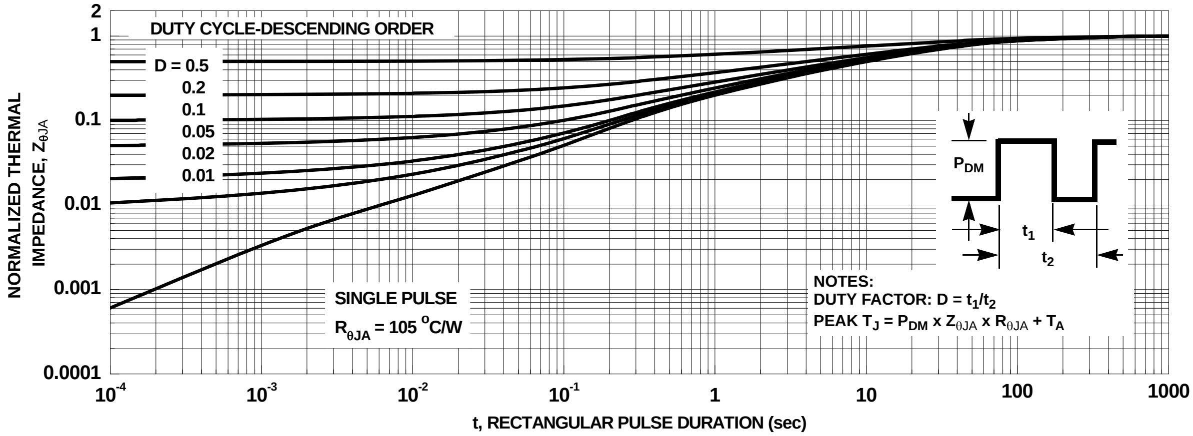
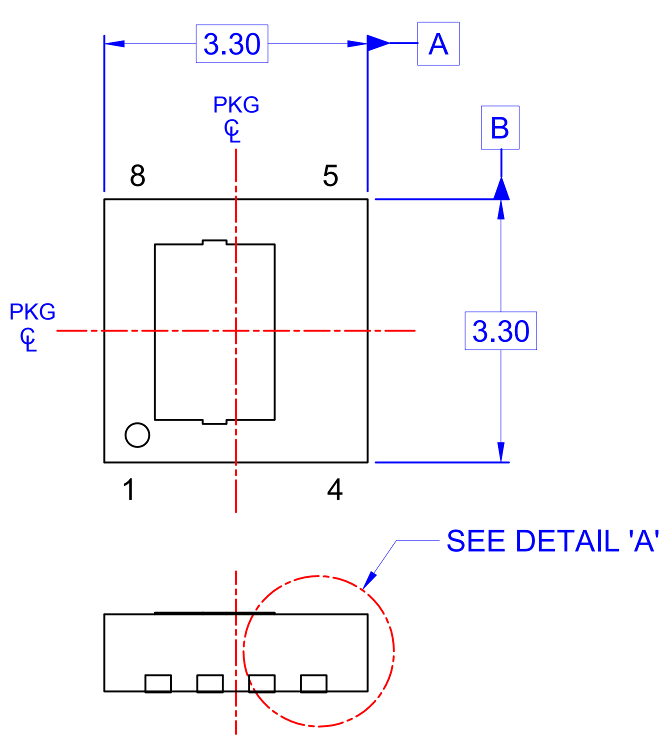
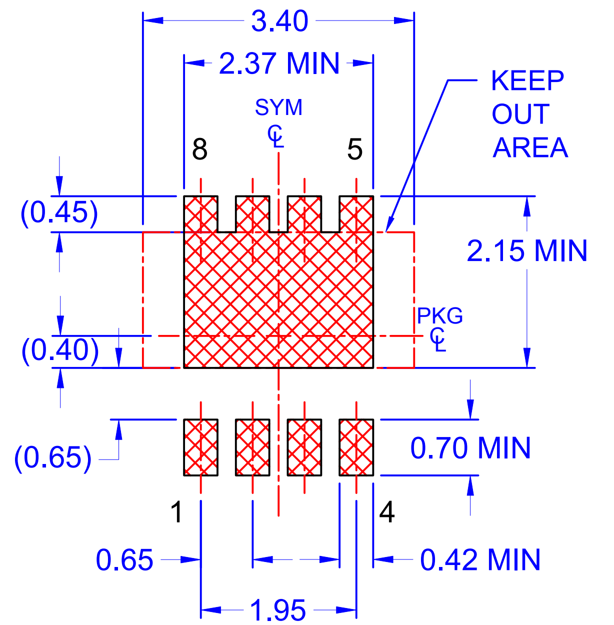
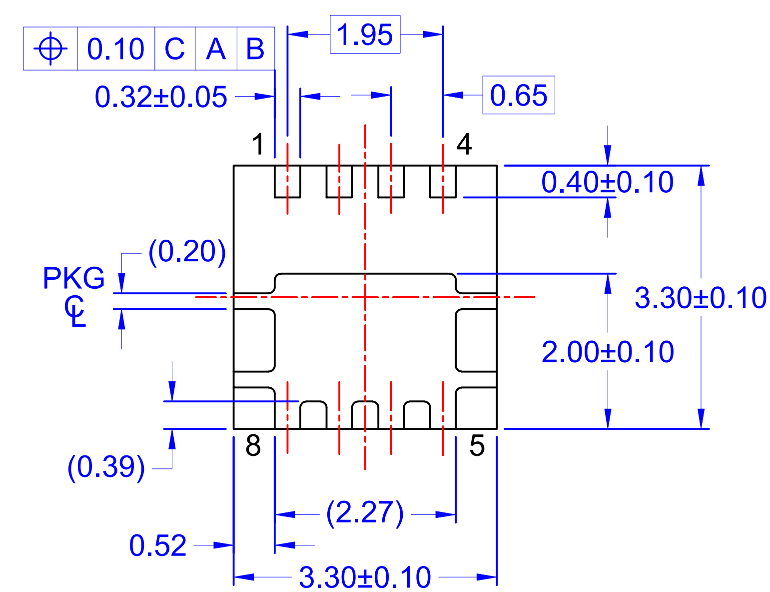


Figure 13. Junction-to-Ambient Transient Thermal Response Curve





LAND PATTERN RECOMMENDATION



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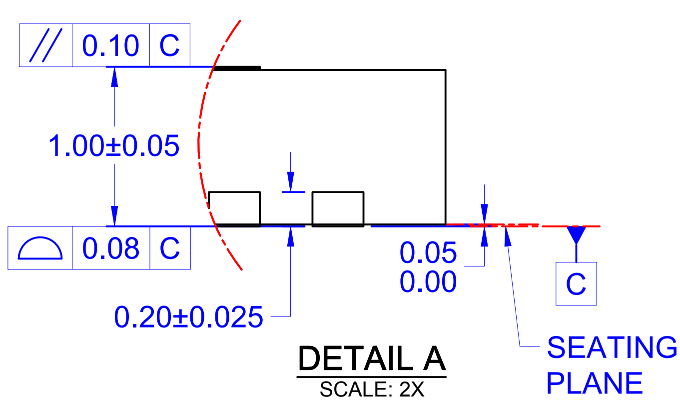
A) PACKAGE STANDARD REFERENCE: JEDEC MO-240, ISSUE A, VAR. BA, DATED OCTOBER 2002.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
E) DRAWING FILE NAME: PQFN08CREV3



DETAIL A
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No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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