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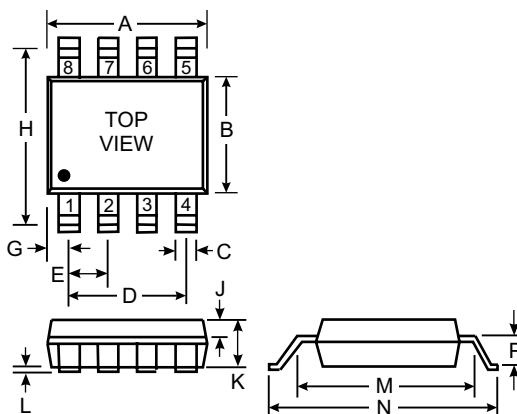


DI9430

SINGLE P-CHANNEL ENHANCEMENT MODE FIELD EFFECT TRANSISTOR

Features

- High Cell Density DMOS Technology
- Low On-State Resistance
- High Power and Current Capability
- Fast Switching Speed
- High Transient Tolerance



SO-8		
Dim	Min	Max
A	3.94	4.19
B	3.20	3.40
C	0.381	0.495
D	2.67	3.05
E	0.89	1.02
G	0.527	0.679
J	0.41 Nominal	
K	0.94	1.09
L	0.025	0.152
M	4.37	4.62
N	4.39	4.70
P	0.939 Nominal	
All Dimensions in mm		

Mechanical Data

- SO-8 Plastic Case
- Terminal Connections: See Outline Drawing and Internal Circuit Diagram above

Maximum Ratings 25°C unless otherwise specified

Characteristic	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	-20	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current Note 1a Continuous @ $T_A = 25^\circ\text{C}$ Note 1a Continuous @ $T_A = 70^\circ\text{C}$ Pulsed @ $T_A = 25^\circ\text{C}$	I_D	± 5.3 ± 4.2 ± 15	A
Maximum Power Dissipation Note 1a Note 1b Note 1c	P_d	2.5 1.2 1.0	W
Operating and Storage Temperature Range	T_J, T_{STG}	-55 to +150	$^\circ\text{C}$

Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction-to-Ambient Note 1a	$R_{\theta JA}$	50	$^\circ\text{C/W}$
Thermal Resistance, Junction-to-Case Note 1	$R_{\theta JC}$	25	$^\circ\text{C/W}$

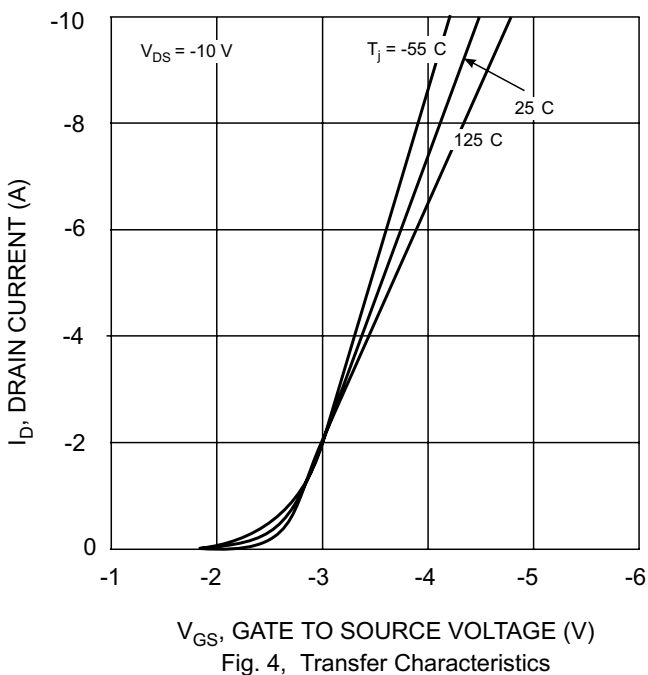
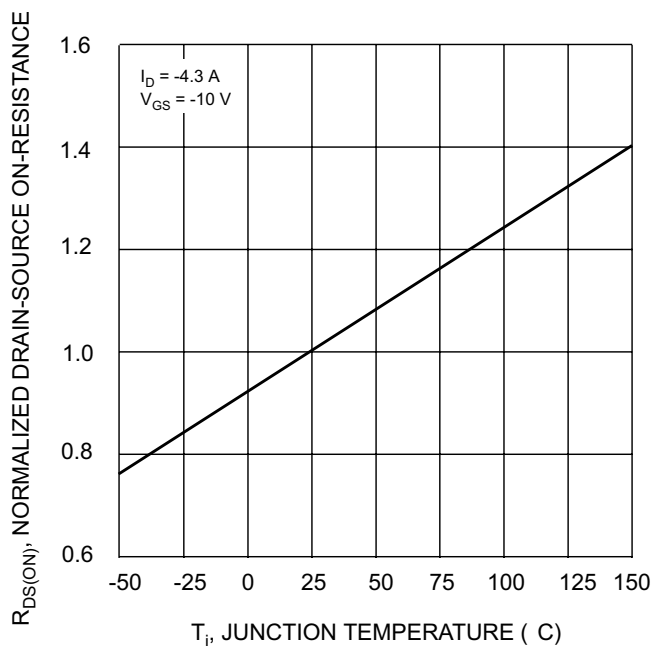
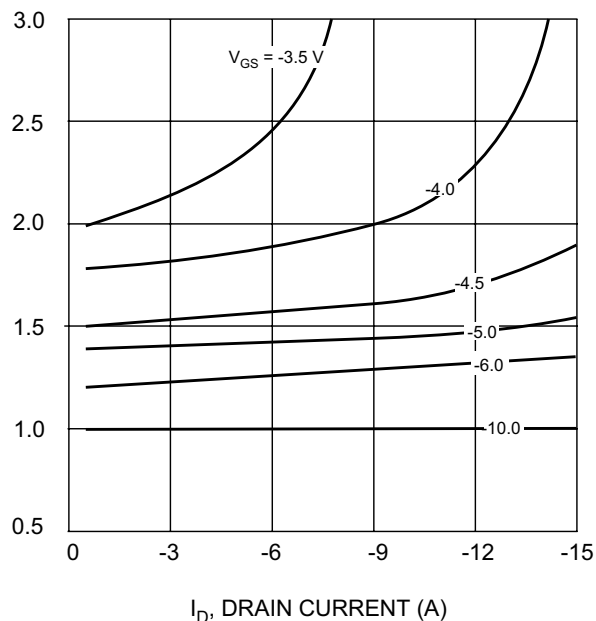
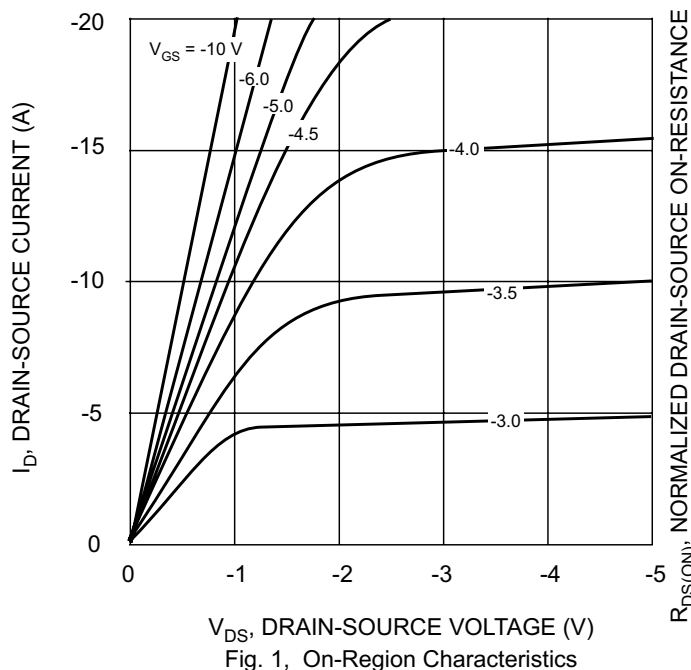
Notes: 1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance ($R_{\theta JC} + R_{\theta CA}$) where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ in this instance is 25°C/W but is dependent on the specific circuit board thermal design.

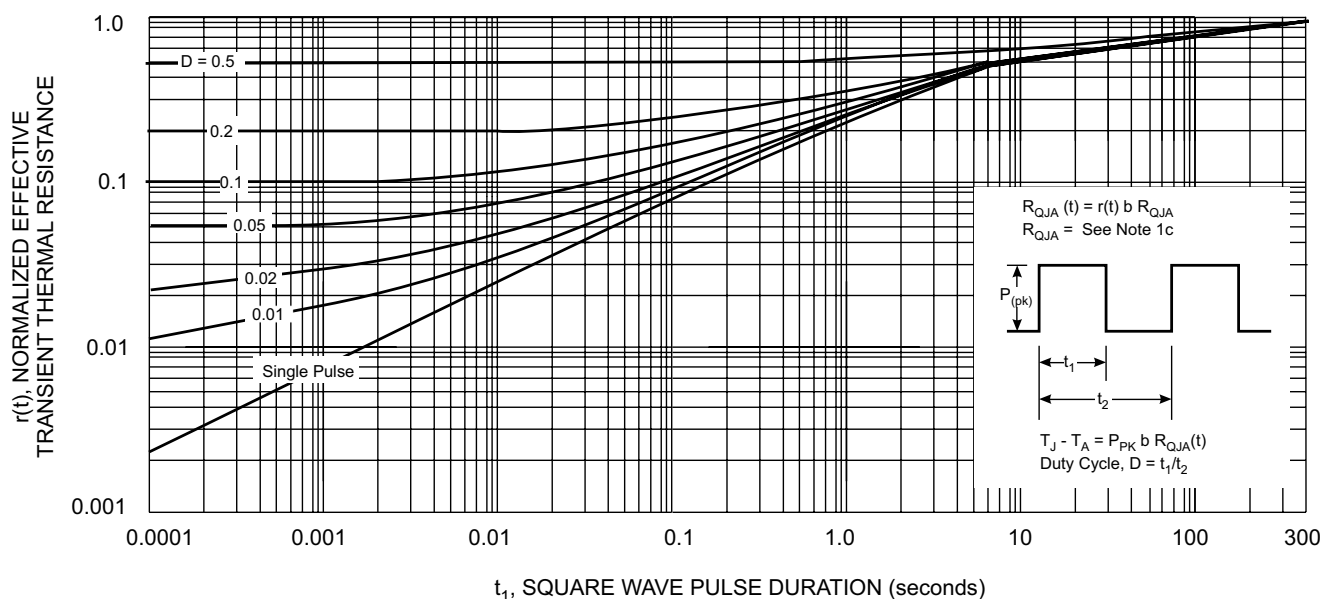
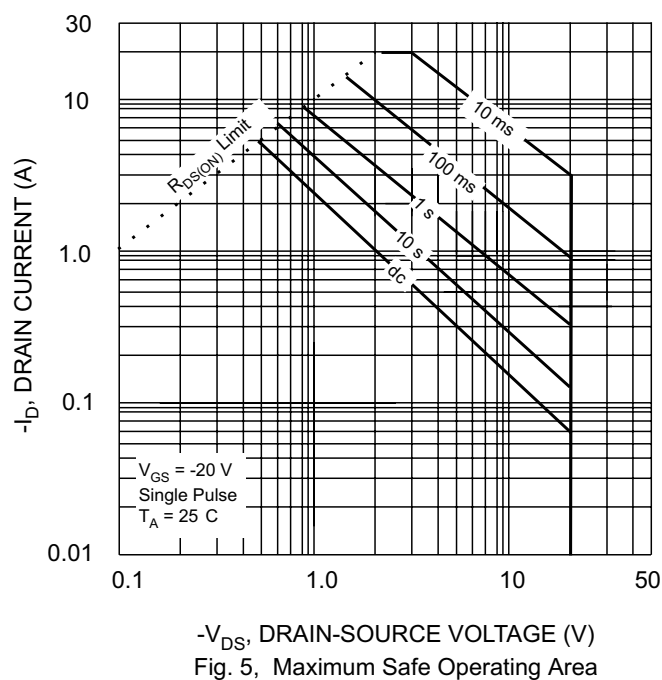
- With 1 in² of 2 oz. copper mounting pad $R_{\theta JA} = 50^\circ\text{C/W}$.
- With 0.04 in² of 2 oz. copper mounting pad $R_{\theta JA} = 105^\circ\text{C/W}$.
- With 0.006 in² of 2 oz. copper mounting pad $R_{\theta JA} = 125^\circ\text{C/W}$.

Electrical Characteristics^{25°C unless otherwise specified}

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV _{DSS}	-20	—	—	V	V _{GS} = 0V, I _D = -25 μA
Zero Gate Voltage Drain Current T _j = 55°C	I _{DSS}	—	—	-1.0 -10	μA	V _{DS} = -16V, V _{GS} = 0V
Gate-Body Leakage, Forward	I _{GSSF}	—	—	100	nA	V _{GS} = 20V, V _{DS} = 0V
Gate-Body Leakage, Reverse	I _{GSSR}	—	—	-100	nA	V _{GS} = -20V, V _{DS} = 0V
ON CHARACTERISTICS (Note 2)						
Gate Threshold Voltage T _j = 125°C	V _{GS(th)}	-1.0 -0.85	-2.0 -1.7	-3.0 -2.6	V	V _{DS} = V _{GS} , I _D = -25 μA
Static Drain-Source On-Resistance T _j = 125°C	R _{DS (ON)}	— —	0.055 0.077 0.067 0.082 0.120	0.060 0.090 0.080 0.115 0.190	Ω	V _{GS} = -10V, I _D = -5.3A V _{GS} = -10V, I _D = -5.3A V _{GS} = -6.0V, I _D = -3.6A V _{GS} = -4.5V, I _D = -2.0A V _{GS} = -4.5V, I _D = -2.0A
On-State Drain Current	I _{D(ON)}	-15 -3.6	—	—	A	V _{GS} = -10V, V _{DS} = -5.0V V _{GS} = -4.5V, V _{DS} = -5.0V
Forward Transconductance	g _{FS}	—	8.0	—	m	V _{DS} = -15V, I _D = -5.3A
DYNAMIC CHARACTERISTICS						
Input Capacitance	C _{ISS}	—	1430	—	pF	V _{DS} = -10V, V _{GS} = 0V f = 1.0MHz
Output Capacitance	C _{OSS}	—	810	—	pF	
Reverse Transfer Capacitance	C _{RSS}	—	375	—	pF	
SWITCHING CHARACTERISTICS (Note 2)						
Turn-On Delay Time	t _{D(ON)}	—	13	30	ns	V _{DD} = -10V, I _D = -1A V _{GEN} = -10V, R _{GEN} = 6.0Ω
Turn-On Rise Time	t _r	—	22	60	ns	
Turn-Off Delay Time	t _{D(OFF)}	—	66	120	ns	
Turn-Off Fall Time	t _f	—	28	100	ns	
Total Gate Charge	Q _g	—	38	—	nC	V _{DS} = -10V. I _D = -5.3A. V _{GS} = -10V
Gate-Source Charge	Q _{gs}	—	3.0	—	nC	
Gate-Drain Charge	Q _{gd}	—	12	—	nC	
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
Max Continuous Drain-Source Diode Forward Current	I _S	—	—	-2.2	A	
Drain-Source Diode Forward Voltage	V _{SD}	—	-1.04	-1.2	V	V _{GS} = 0V, I _S = -5.3A (Note 2)
Reverse Recovery Time	t _{rr}	—	80	100	ns	V _{GS} = 0V, I _F = -5.3A, dI _F /dt = 100A/μs

Note: 2. Pulse Test width $\leq 300 \mu s$, duty cycle $\leq 2\%$.





Remark: Thermal characterization performed under conditions of Note 1c. Better thermal design such as shown in Notes 1a and 1b or 1d will offer lower R_{QJA} values and allow junction to reach thermal equilibrium sooner.