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[FDD5N50NZTM](#)

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November 2013



## FDD5N50NZ

### N-Channel UniFET™ II MOSFET

#### 500 V, 4 A, 1.5 Ω

#### Features

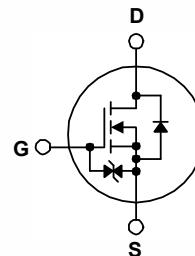
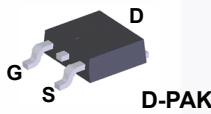
- $R_{DS(on)} = 1.38 \Omega$  (Typ.) @  $V_{GS} = 10$  V,  $I_D = 2$  A
- Low Gate Charge (Typ. 9 nC)
- Low  $C_{rss}$  (Typ. 4 pF)
- 100% Avalanche Tested
- Improved dv/dt Capability
- ESD Improved Capability
- RoHS Compliant

#### Applications

- LCD/LED/PDP TV
- Lighting
- Uninterruptible Power Supply

#### Description

UniFET™ II MOSFET is Fairchild Semiconductor's high voltage MOSFET family based on advanced planar stripe and DMOS technology. This advanced MOSFET family has the smallest on-state resistance among the planar MOSFET, and also provides superior switching performance and higher avalanche energy strength. In addition, internal gate-source ESD diode allows UniFET™ II MOSFET to withstand over 2kV HBM surge stress. This device family is suitable for switching power converter applications such as power factor correction (PFC), flat panel display (FPD) TV power, ATX and electronic lamp ballasts.



#### Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter		FDD5N50NZTM	Unit
$V_{DSS}$	Drain to Source Voltage		500	V
$V_{GSS}$	Gate to Source Voltage		$\pm 25$	V
$I_D$	Drain Current	- Continuous ( $T_C = 25^\circ\text{C}$ )	4	A
		- Continuous ( $T_C = 100^\circ\text{C}$ )	2.4	
$I_{DM}$	Drain Current	- Pulsed	(Note 1)	A
$E_{AS}$	Single Pulsed Avalanche Energy		(Note 2)	mJ
$I_{AR}$	Avalanche Current		(Note 1)	A
$E_{AR}$	Repetitive Avalanche Energy		(Note 1)	mJ
$dv/dt$	Peak Diode Recovery $dv/dt$		(Note 3)	V/ns
$P_D$	Power Dissipation	( $T_C = 25^\circ\text{C}$ )	62	W
		- Derate Above $25^\circ\text{C}$	0.5	W/ $^\circ\text{C}$
$T_J, T_{STG}$	Operating and Storage Temperature Range		-55 to +150	$^\circ\text{C}$
$T_L$	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds		300	$^\circ\text{C}$

#### Thermal Characteristics

Symbol	Parameter	FDD5N50NZTM	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	2.0	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	90	

### Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FDD5N50NZTM	FDD5N50NZ	DPAK	Tape and Reel	330 mm	16 mm	2500 units

### Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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#### Off Characteristics

$\text{BV}_{\text{DSS}}$	Drain to Source Breakdown Voltage	$I_D = 250 \mu\text{A}, V_{GS} = 0 \text{ V}, T_J = 25^\circ\text{C}$	500	-	-	V
$\Delta \text{BV}_{\text{DSS}} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250 \mu\text{A}, \text{Referenced to } 25^\circ\text{C}$	-	0.5	-	$^\circ\text{C}$
$I_{\text{DSS}}$	Zero Gate Voltage Drain Current	$V_{DS} = 500 \text{ V}, V_{GS} = 0 \text{ V}$ $V_{DS} = 400 \text{ V}, T_C = 125^\circ\text{C}$	-	-	10	$\mu\text{A}$
$I_{\text{GSS}}$	Gate to Body Leakage Current	$V_{GS} = \pm 25 \text{ V}, V_{DS} = 0 \text{ V}$	-	-	$\pm 10$	$\mu\text{A}$

#### On Characteristics

$V_{GS(\text{th})}$	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250 \mu\text{A}$	3.0	-	5.0	V
$R_{DS(\text{on})}$	Static Drain to Source On Resistance	$V_{GS} = 10 \text{ V}, I_D = 2 \text{ A}$	-	1.38	1.5	$\Omega$
$g_{\text{FS}}$	Forward Transconductance	$V_{DS} = 20 \text{ V}, I_D = 2 \text{ A}$	-	3.54	-	S

#### Dynamic Characteristics

$C_{\text{iss}}$	Input Capacitance	$V_{DS} = 25 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	-	330	440	pF
$C_{\text{oss}}$	Output Capacitance		-	50	70	pF
$C_{\text{rss}}$	Reverse Transfer Capacitance		-	4	6	pF
$Q_{\text{g}(\text{tot})}$	Total Gate Charge at 10V	$V_{DS} = 400 \text{ V}, I_D = 4 \text{ A}, V_{GS} = 10 \text{ V}$	-	9	12	nC
$Q_{\text{gs}}$	Gate to Source Gate Charge		-	2	-	nC
$Q_{\text{gd}}$	Gate to Drain "Miller" Charge		(Note 4)	-	4	nC

#### Switching Characteristics

$t_{\text{d}(\text{on})}$	Turn-On Delay Time	$V_{DD} = 250 \text{ V}, I_D = 4 \text{ A}, V_{GS} = 10 \text{ V}, R_G = 25 \Omega$	-	12	35	ns
$t_r$	Turn-On Rise Time		-	22	55	ns
$t_{\text{d}(\text{off})}$	Turn-Off Delay Time		-	28	65	ns
$t_f$	Turn-Off Fall Time		(Note 4)	-	21	50

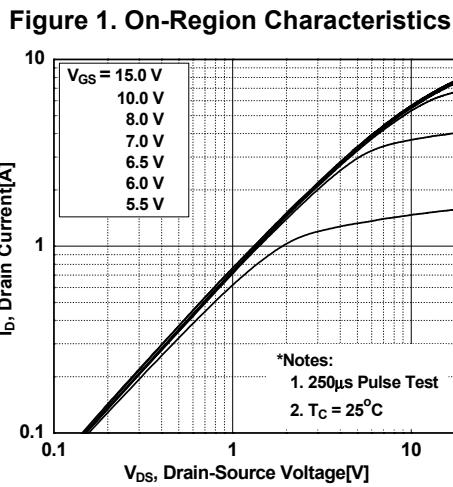
#### Drain-Source Diode Characteristics

$I_S$	Maximum Continuous Drain to Source Diode Forward Current	-	-	4	A	
$I_{\text{SM}}$	Maximum Pulsed Drain to Source Diode Forward Current	-	-	16	A	
$V_{SD}$	Drain to Source Diode Forward Voltage	$V_{GS} = 0 \text{ V}, I_{SD} = 4 \text{ A}$	-	-	1.4	V
$t_{\text{rr}}$	Reverse Recovery Time	$V_{GS} = 0 \text{ V}, I_{SD} = 4 \text{ A}, dI/dt = 100 \text{ A}/\mu\text{s}$	-	210	-	ns
$Q_{\text{rr}}$	Reverse Recovery Charge	-	-	1.1	-	$\mu\text{C}$

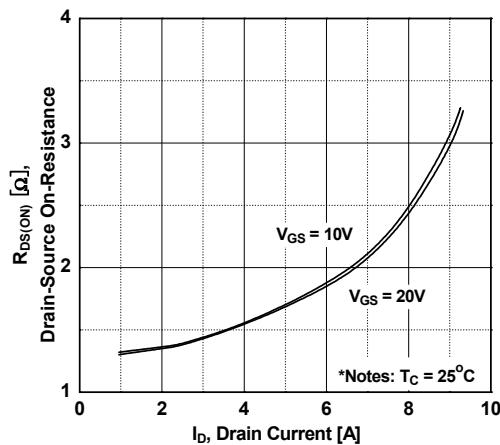
#### Notes:

1. Repetitive rating: pulse-width limited by maximum junction temperature.
2. L = 38 mH,  $I_{AS} = 4 \text{ A}, V_{DD} = 50 \text{ V}, R_G = 25 \Omega$ , starting  $T_J = 25^\circ\text{C}$ .
3.  $I_{SD} \leq 4 \text{ A}, dI/dt \leq 200 \text{ A}/\mu\text{s}, V_{DD} \leq \text{BV}_{\text{DSS}}$ , starting  $T_J = 25^\circ\text{C}$ .
4. Essentially independent of operating temperature typical characteristics.

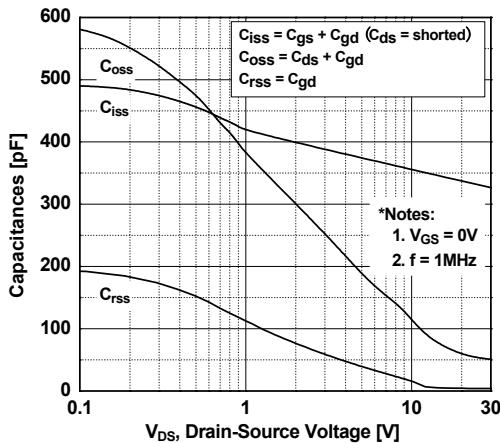
## Typical Performance Characteristics



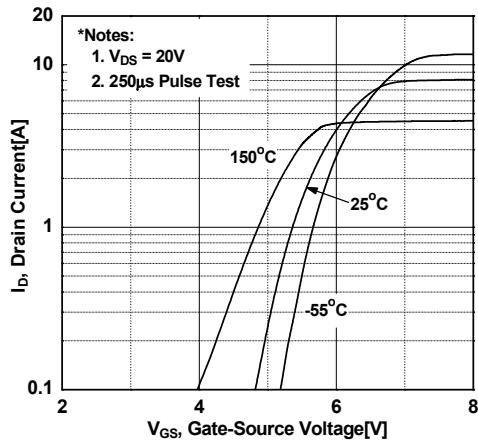
**Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage**



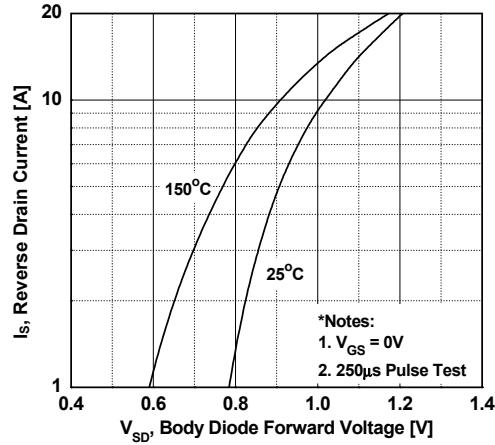
**Figure 5. Capacitance Characteristics**



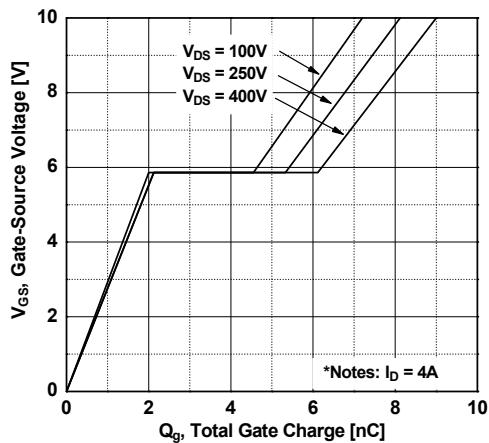
**Figure 2. Transfer Characteristics**



**Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature**

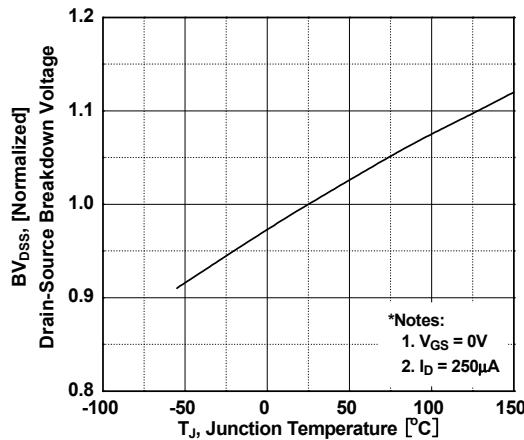


**Figure 6. Gate Charge Characteristics**

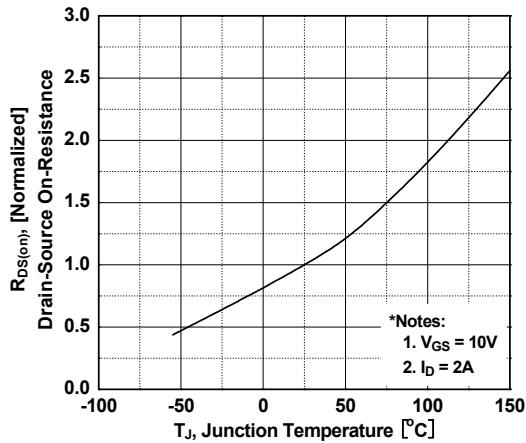


**Typical Performance Characteristics (Continued)**

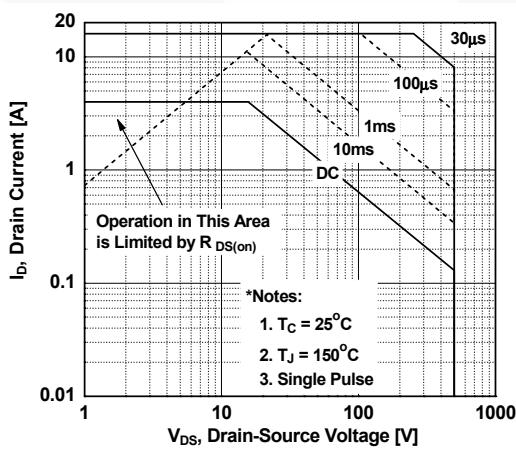
**Figure 7. Breakdown Voltage Variation vs. Temperature**



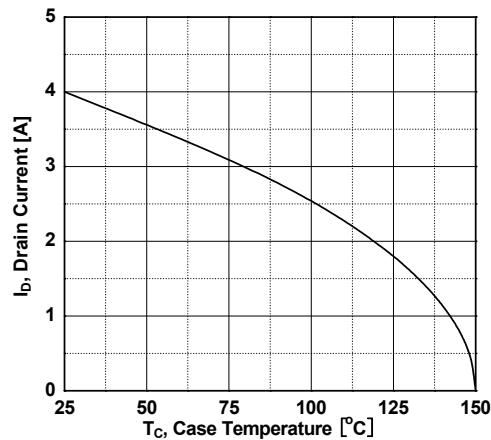
**Figure 8. On-Resistance Variation vs. Temperature**



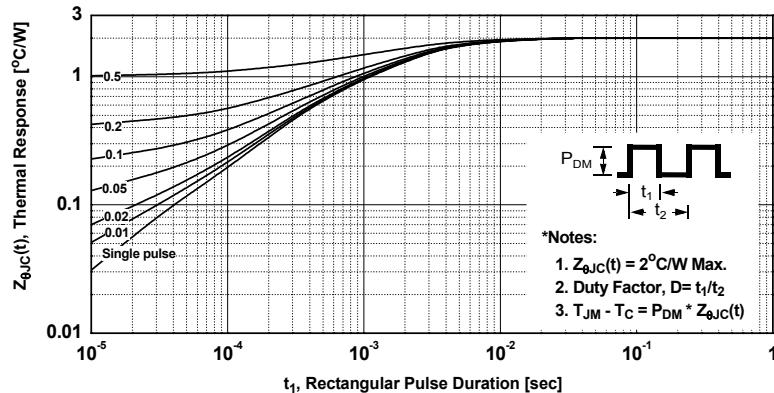
**Figure 9. Maximum Safe Operating Area**

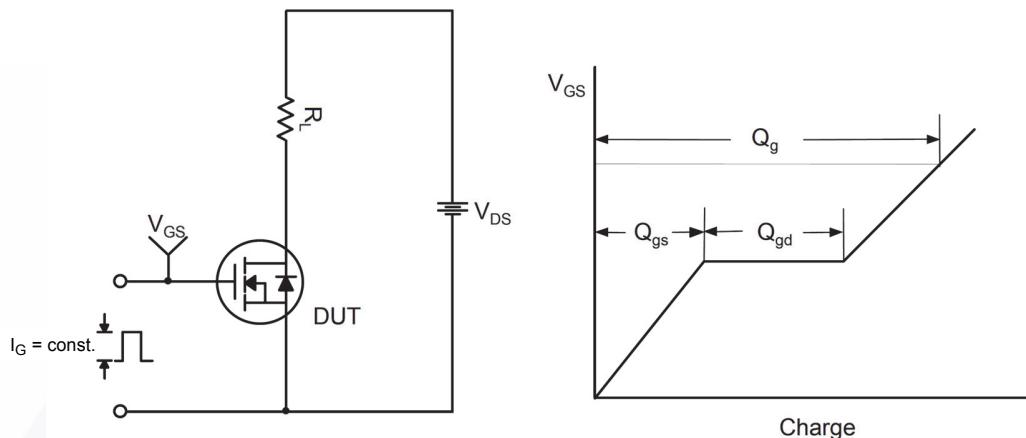


**Figure 10. Maximum Drain Current vs. Case Temperature**

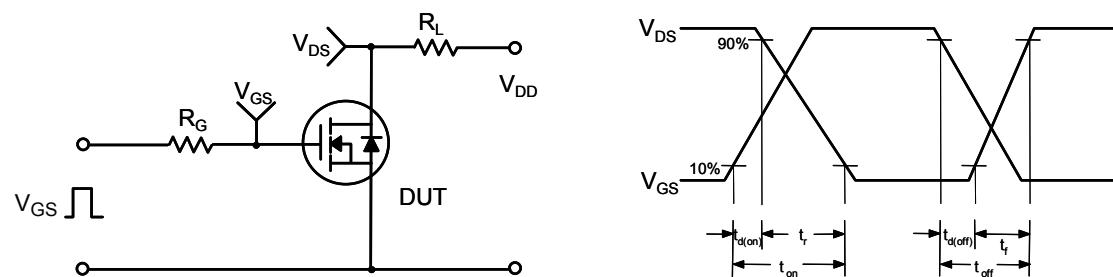


**Figure 11. Transient Thermal Response Curve**

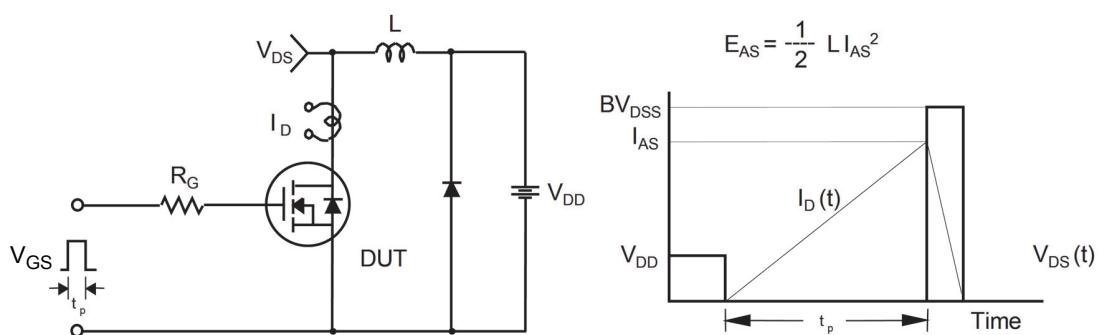




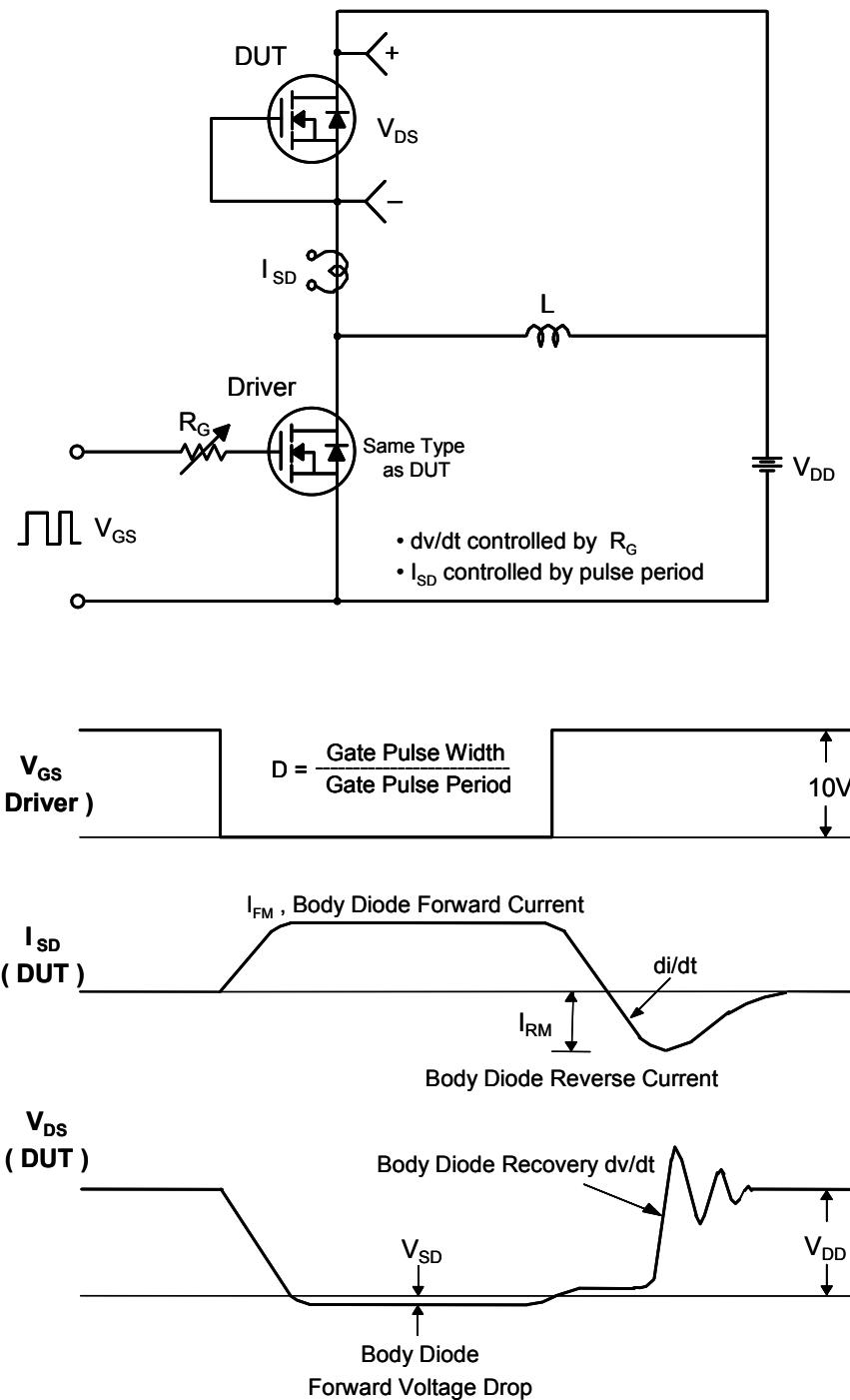
**Figure 12. Gate Charge Test Circuit & Waveform**



**Figure 13. Resistive Switching Test Circuit & Waveforms**

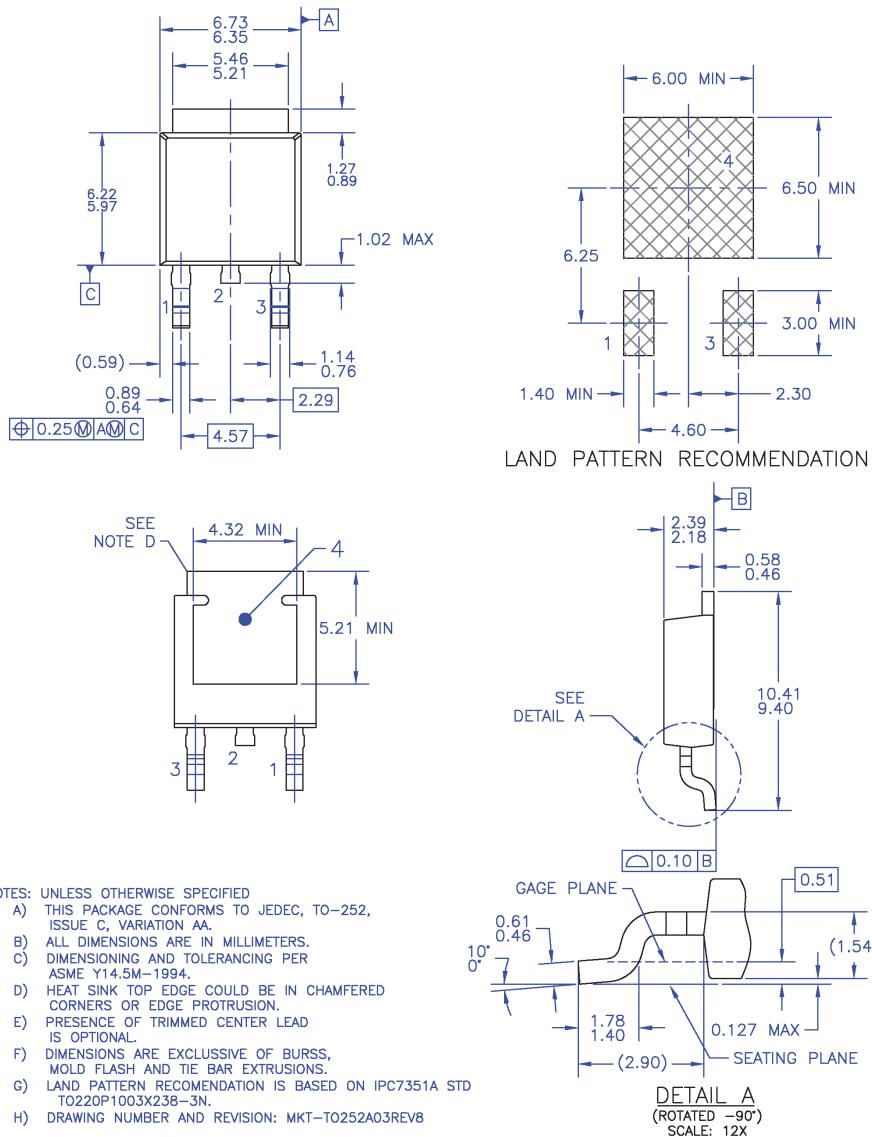


**Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms**



**Figure 15. Peak Diode Recovery  $dv/dt$  Test Circuit & Waveforms**

## Mechanical Dimensions



**Figure 16. TO252 (D-PAK), Molded, 3-Lead, Option AA&AB**

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