

TC74VHC273F,TC74VHC273FW,TC74VHC273FT,TC74VHC273FK**Octal D-Type Flip-Flop with Clear**

The TC74VHC273 is an advanced high speed CMOS OCTAL D-TYPE FLIP FLOP fabricated with silicon gate C²MOS technology.

It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

Information signals applied to D inputs are transferred to the Q outputs on the positive going edge of the clock pulse.

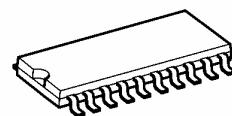
When the CLR input is held "L", the Q outputs are at a low logic level independent of the other inputs.

An input protection circuit ensures that 0 to 5.5 V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5 V to 3 V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

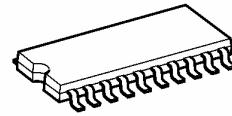
Features

- High speed: $f_{max} = 165$ MHz (typ.) at $V_{CC} = 5$ V
- Low power dissipation: $I_{CC} = 4$ μ A (max) at $T_a = 25^\circ$ C
- High noise immunity: $V_{NIH} = V_{NIL} = 28\%$ V_{CC} (min)
- Power down protection is provided on all inputs.
- Balanced propagation delays: $t_{PLH} \approx t_{PHL}$
- Wide operating voltage range: V_{CC} (opr) = 2 to 5.5 V
- Low noise: $V_{OLP} = 0.9$ V (max)
- Pin and function compatible with 74ALS273

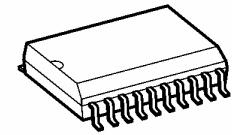
Note: xxxFW (JEDEC SOP) is not available in Japan.

TC74VHC273F

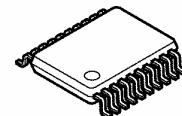
SOP20-P-300-1.27A



SOP20-P-300-1.27

TC74VHC273FW

SOL20-P-300-1.27

TC74VHC273FT

TSSOP20-P-0044-0.65A

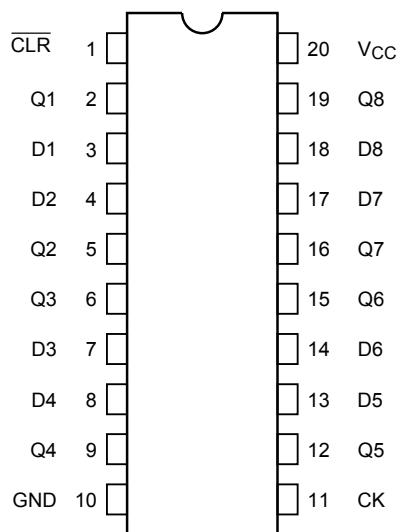
TC74VHC273FK

VSSOP20-P-0030-0.50

Weight

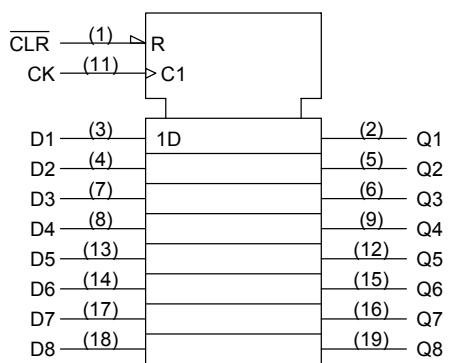
SOP20-P-300-1.27A	: 0.22 g (typ.)
SOP20-P-300-1.27	: 0.22 g (typ.)
SOL20-P-300-1.27	: 0.46 g (typ.)
TSSOP20-P-0044-0.65A	: 0.08 g (typ.)
VSSOP20-P-0030-0.50	: 0.03 g (typ.)

Pin Assignment



(top view)

IEC Logic Symbol

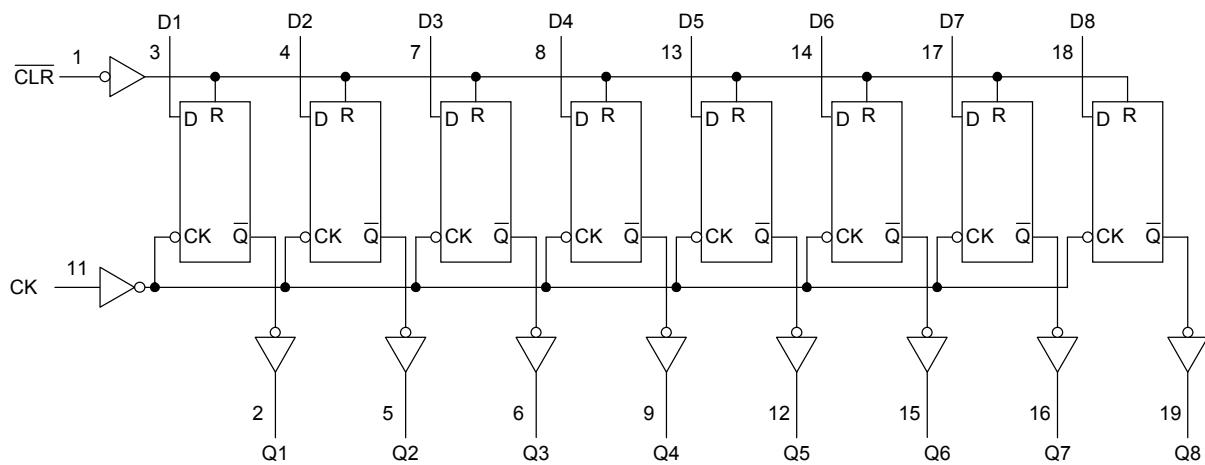


Truth Table

Inputs			Output	Function
$\overline{\text{CLR}}$	D	CK	Q	
L	X	X	L	Clear
H	L	↑	L	—
H	H	↑	H	—
H	X	↓	Q_n	No Change

X: Don't care

System Diagram



Absolute Maximum Ratings (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage range	V_{CC}	-0.5 to 7.0	V
DC input voltage	V_{IN}	-0.5 to 7.0	V
DC output voltage	V_{OUT}	-0.5 to $V_{CC} + 0.5$	V
Input diode current	I_{IK}	-20	mA
Output diode current	I_{OK}	± 20	mA
DC output current	I_{OUT}	± 25	mA
DC V_{CC} /ground current	I_{CC}	± 75	mA
Power dissipation	P_D	180	mW
Storage temperature	T_{stg}	-65 to 150	°C

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Recommended Operating Conditions (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{CC}	2.0 to 5.5	V
Input voltage	V_{IN}	0 to 5.5	V
Output voltage	V_{OUT}	0 to V_{CC}	V
Operating temperature	T_{opr}	-40 to 85	°C
Input rise and fall time	dt/dv	0 to 100 ($V_{CC} = 3.3 \pm 0.3$ V) 0 to 20 ($V_{CC} = 5 \pm 0.5$ V)	ns/V

Note: The recommended operating conditions are required to ensure the normal operation of the device.
Unused inputs must be tied to either VCC or GND.

Electrical Characteristics

DC Characteristics

Characteristics	Symbol	Test Condition		Ta = 25°C			Ta = -40 to 85°C		Unit
				V _{CC} (V)	Min	Typ.	Max	Min	
High-level input voltage	V _{IH}	—		2.0	1.50	—	—	1.50	V
				3.0 to 5.5	V _{CC} × 0.7	—	—	V _{CC} × 0.7	
Low-level input voltage	V _{IL}	—		2.0	—	—	0.50	—	V
				3.0 to 5.5	V _{CC} × 0.3	—	V _{CC} × 0.3	—	
High-level output voltage	V _{OH}	V _{IN} = V _{IH} or V _{IL}	I _{OH} = -50 µA	2.0	1.9	2.0	—	1.9	V
				3.0	2.9	3.0	—	2.9	
				4.5	4.4	4.5	—	4.4	
			I _{OH} = -4 mA	3.0	2.58	—	—	2.48	—
Low-level output voltage	V _{OL}	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 50 µA	4.5	3.94	—	—	3.80	V
				2.0	—	0.0	0.1	—	
				3.0	—	0.0	0.1	—	
				4.5	—	0.0	0.1	—	
Input leakage current	I _{IN}	V _{IN} = 5.5 V or GND	I _{OL} = 4 mA	3.0	—	—	0.36	—	0.44
			I _{OL} = 8 mA	4.5	—	—	0.36	—	
Quiescent supply current	I _{CC}	V _{IN} = V _{CC} or GND	0 to 5.5	—	—	±0.1	—	±1.0	µA

Timing Requirements (input: t_r = t_f = 3 ns)

Characteristics	Symbol	Test Condition		Ta = 25°C		Ta = -40 to 85°C		Unit
				V _{CC} (V)	Typ.	Limit	Limit	
Minimum pulse width (CK)	t _w (L) t _w (H)	—		3.3 ± 0.3	—	5.5	6.5	ns
				5.0 ± 0.5	—	5.0	5.0	
Minimum pulse width (CLR)	t _w (L)	—		3.3 ± 0.3	—	5.0	6.0	ns
				5.0 ± 0.5	—	5.0	5.0	
Minimum set-up time	t _s	—		3.3 ± 0.3	—	5.5	6.5	ns
				5.0 ± 0.5	—	4.5	4.5	
Minimum hold time	t _h	—		3.3 ± 0.3	—	1.0	1.0	ns
				5.0 ± 0.5	—	1.0	1.0	
Minimum removal time (CLR)	t _{rem}	—		3.3 ± 0.3	—	2.5	2.5	ns
				5.0 ± 0.5	—	2.0	2.0	

AC Characteristics (input: $t_r = t_f = 3$ ns)

Characteristics	Symbol	Test Condition		Ta = 25°C			Ta = -40 to 85°C		Unit	
		V _{CC} (V)	C _L (pF)	Min	Typ.	Max	Min	Max		
Propagation delay time (CK-Q)	t _{pLH}	—	3.3 ± 0.3	15	—	8.7	13.6	1.0	16.0	
				50	—	11.2	17.1	1.0	19.5	
	t _{pHL}		5.0 ± 0.5	15	—	5.8	9.0	1.0	10.5	
				50	—	7.3	11.0	1.0	12.5	
Propagation delay time (CLR-Q)	t _{pHL}	—	3.3 ± 0.3	15	—	8.9	13.6	1.0	16.0	
				50	—	11.4	17.1	1.0	19.5	
	t _{pLH}		5.0 ± 0.5	15	—	5.2	8.5	1.0	10.0	
				50	—	6.7	10.5	1.0	12.0	
Maximum clock frequency	f _{max}	—	3.3 ± 0.3	15	75	120	—	65	MHz	
				50	50	75	—	45		
	f _{max}		5.0 ± 0.5	15	120	165	—	100		
				50	80	110	—	70		
Output to output skew	t _{osLH}	(Note 1)	3.3 ± 0.3	50	—	—	1.5	—	ns	
	t _{osHL}		5.0 ± 0.5	50	—	—	1.0	—		
Input capacitance	C _{IN}	—			—	4	10	—	10	pF
Power dissipation capacitance	C _{PD}	(Note 2)			—	31	—	—	—	pF

Note 1: Parameter guaranteed by design.

$$t_{osLH} = |t_{pLHm} - t_{pLHn}|, t_{osHL} = |t_{pHLM} - t_{pHLn}|$$

Note 2: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC} (\text{opr}) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 \text{ (per bit)}$$

And the total C_{PD} when n pcs.of flip flop operate can be gained by the following equation:

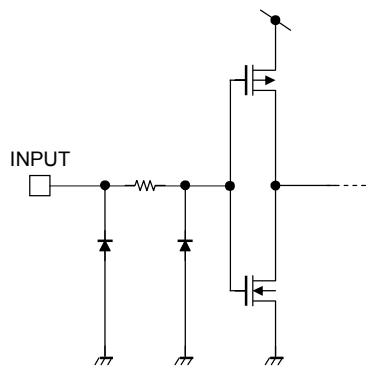
$$C_{PD} (\text{total}) = 22 + 9 \cdot n$$

Noise Characteristics (input: $t_r = t_f = 3$ ns) (Note)

Characteristics	Symbol	Test Condition		Ta = 25°C		Unit
		V _{CC} (V)	Typ.	Max		
Quiet output maximum dynamic V _{OL}	V _{OLP}	C _L = 50 pF	5.0	0.5 (0.6)	0.8 (0.9)	V
Quiet output minimum dynamic V _{OL}	V _{OLV}	C _L = 50 pF	5.0	-0.5 (-0.6)	-0.8 (-0.9)	V
Minimum high level dynamic input voltage	V _{IHD}	C _L = 50 pF	5.0	—	3.5	V
Maximum low level dynamic input voltage	V _{ILD}	C _L = 50 pF	5.0	—	1.5	V

Note: The value in () only applies to JEDEC SOP (FW) devices.

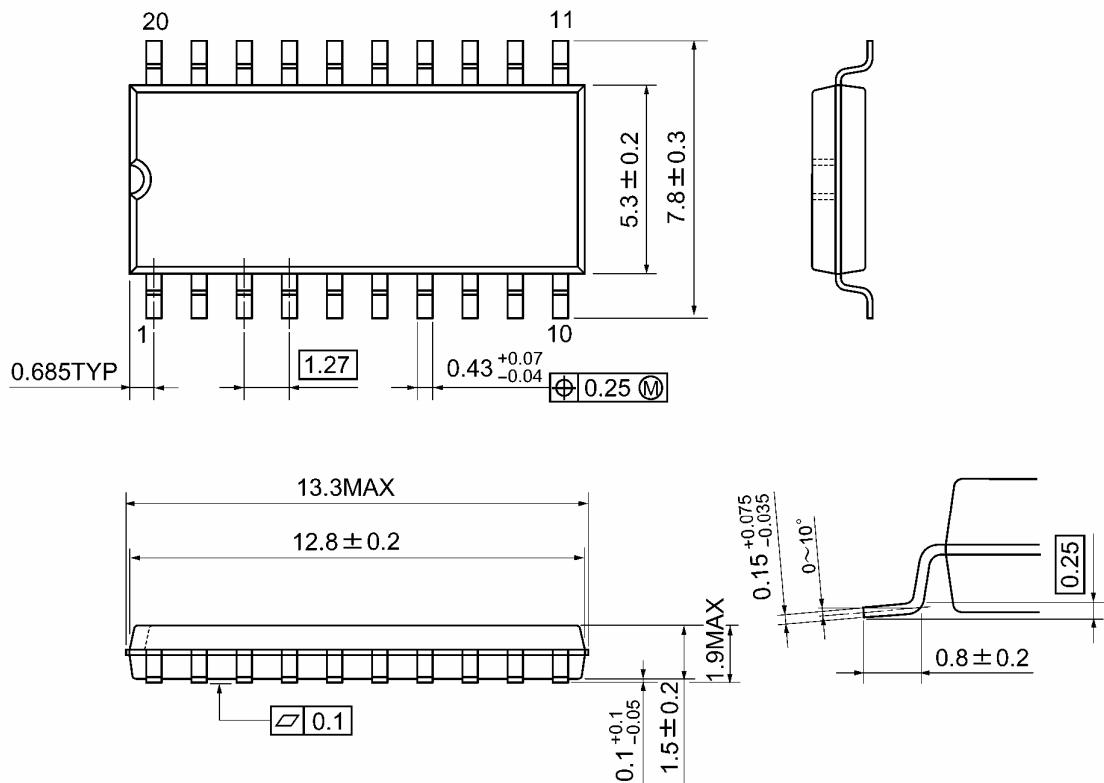
Input Equivalent Circuit



Package Dimensions

SOP20-P-300-1.27A

Unit: mm

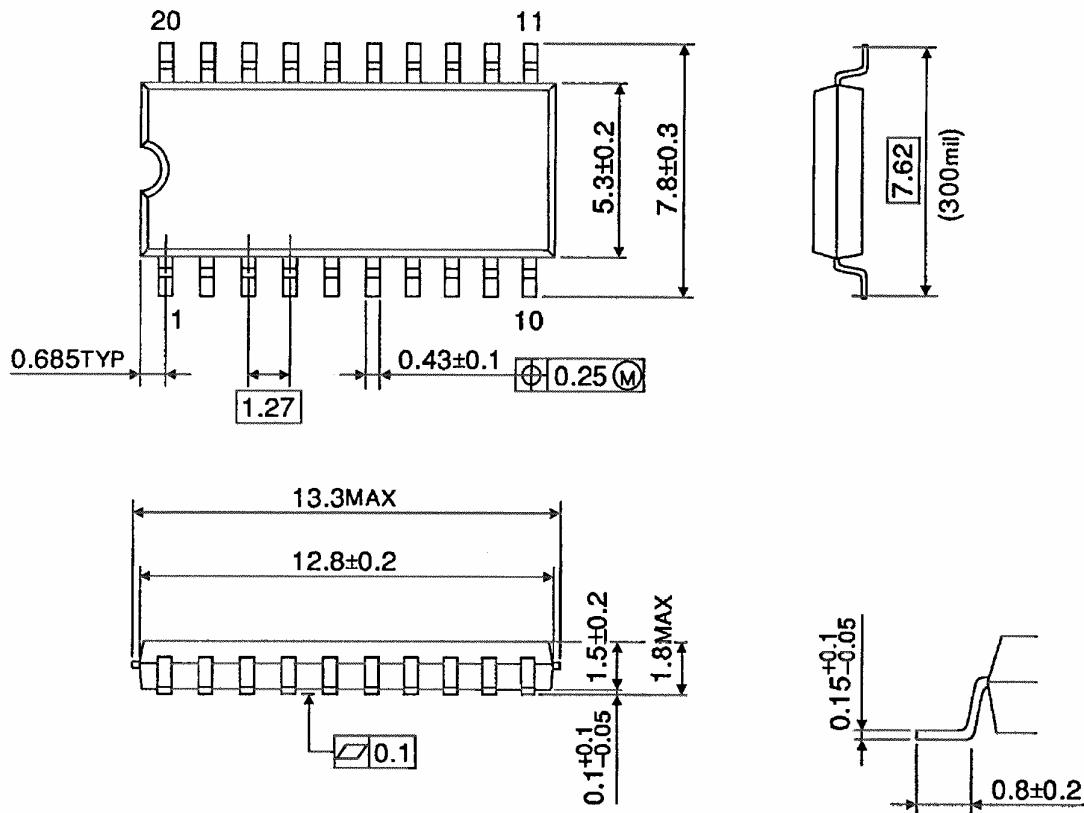


Weight: 0.22 g (typ.)

Package Dimensions

SOP20-P-300-1.27

Unit : mm

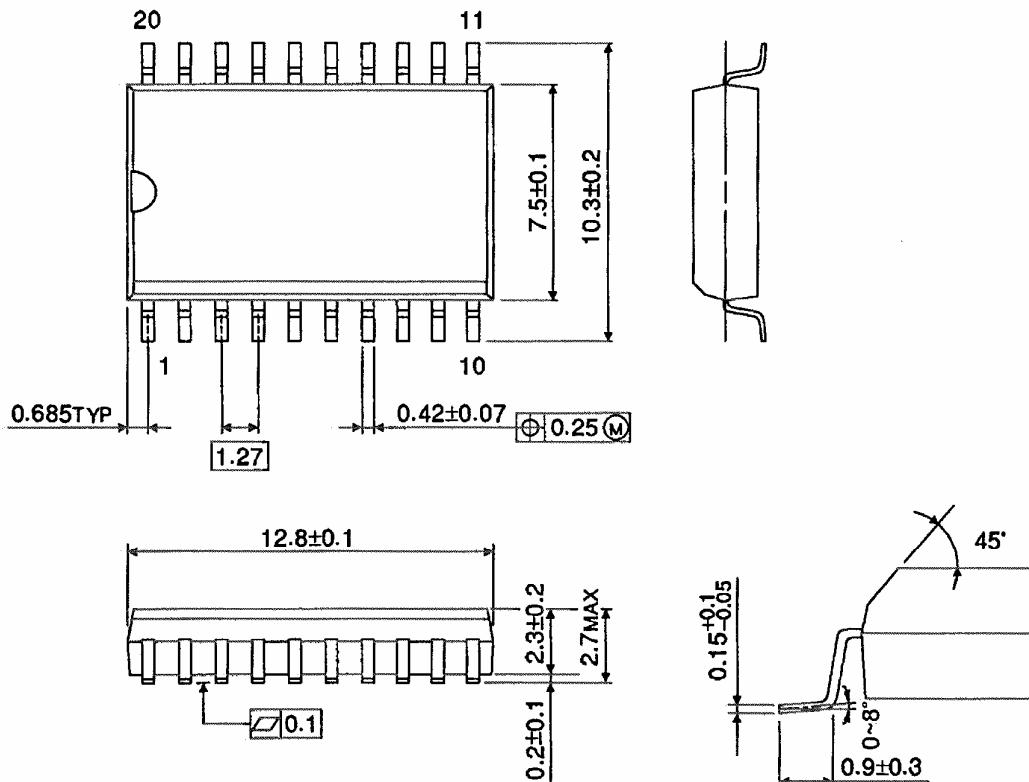


Weight: 0.22 g (typ.)

Package Dimensions (Note)

SOL20-P-300-1.27

Unit : mm



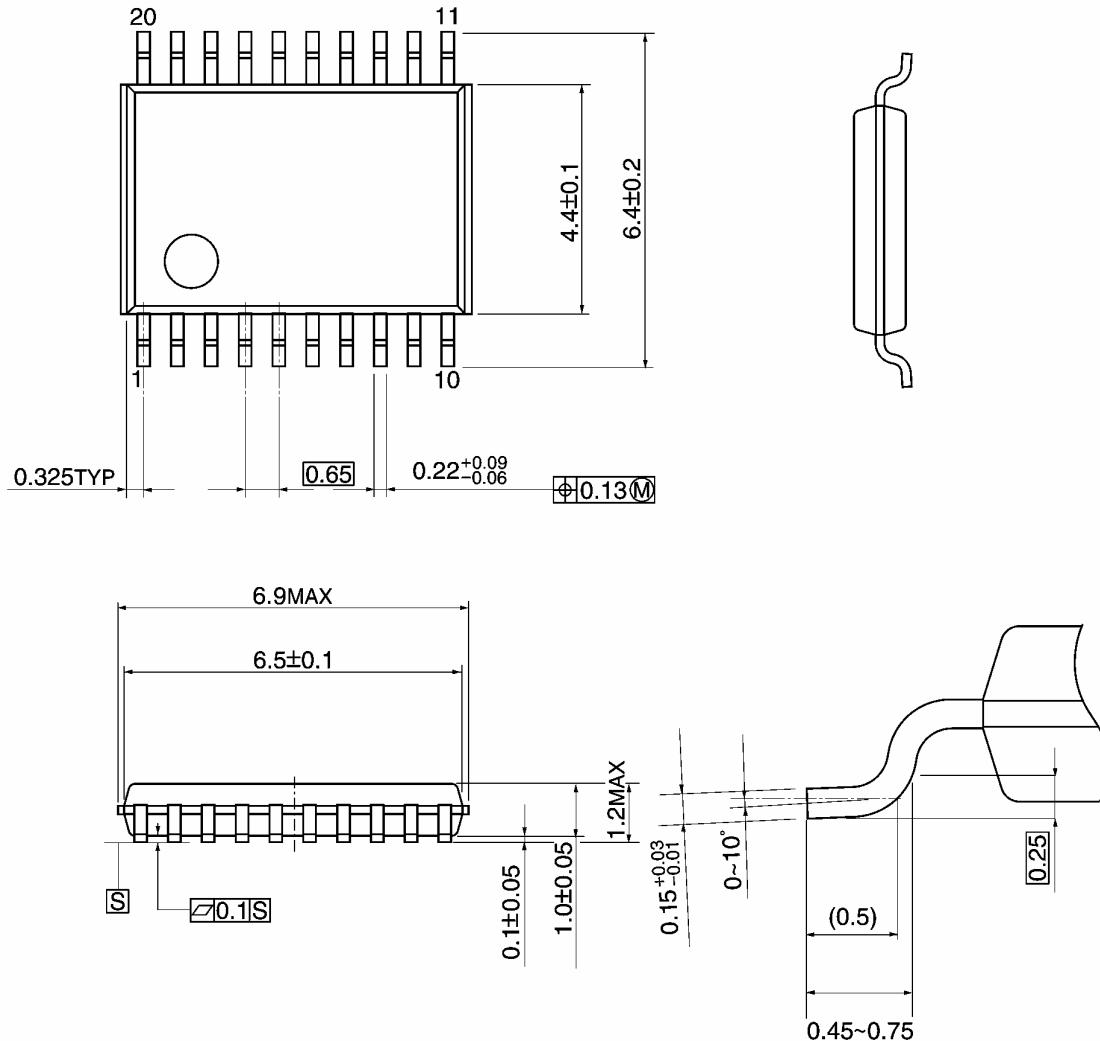
Note: This package is not available in Japan.

Weight: 0.46 g (typ.)

Package Dimensions

TSSOP20-P-0044-0.65A

Unit: mm

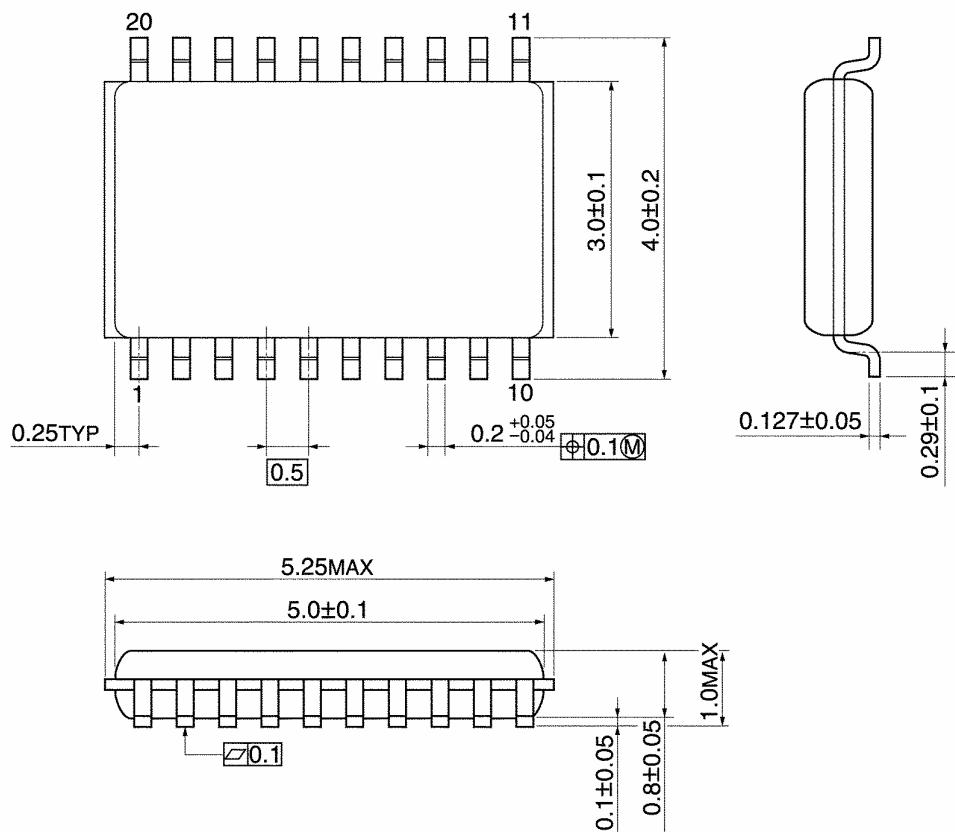


Weight: 0.08 g (typ.)

Package Dimensions

VSSOP20-P-0030-0.50

Unit: mm



Weight: 0.03 g (typ.)

Note: Lead (Pb)-Free Packages**SOP20-P-300-1.27A TSSOP20-P-0044-0.65A VSSOP20-P-0030-0.50****RESTRICTIONS ON PRODUCT USE**

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