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[International Rectifier \(Infineon Technologies Americas Corp.\)
AUIRS4427S](#)

For any questions, you can email us directly:

sales@integrated-circuit.com

Features

- Gate drive supply range from 6 V to 20 V
- CMOS Schmitt-triggered inputs
- 3.3V and 5V logic compatible
- Two independent gate drivers
- Matched propagation delay for both channels
- Outputs in phase with inputs
- Leadfree, RoHS compliant
- Automotive qualified*

Typical Applications

- Automotive General Purpose Dual Low Side Driver
- Automotive DC-DC converters
- Hybrid Power Train Drives
- Direct Fuel Injection

Product Summary

Topology	General Driver
V _{OUT}	6V - 20V
I _{o+} & I _{o-} (typical)	2.3A & 3.3A
t _{on} & t _{off} (typical)	50ns & 50ns

Package Type

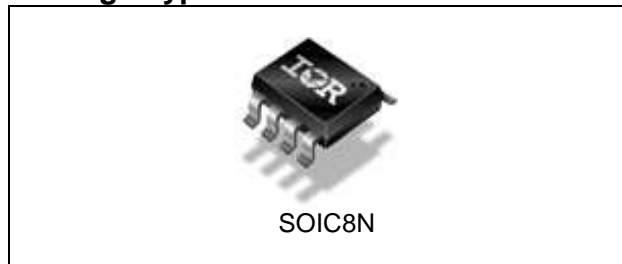
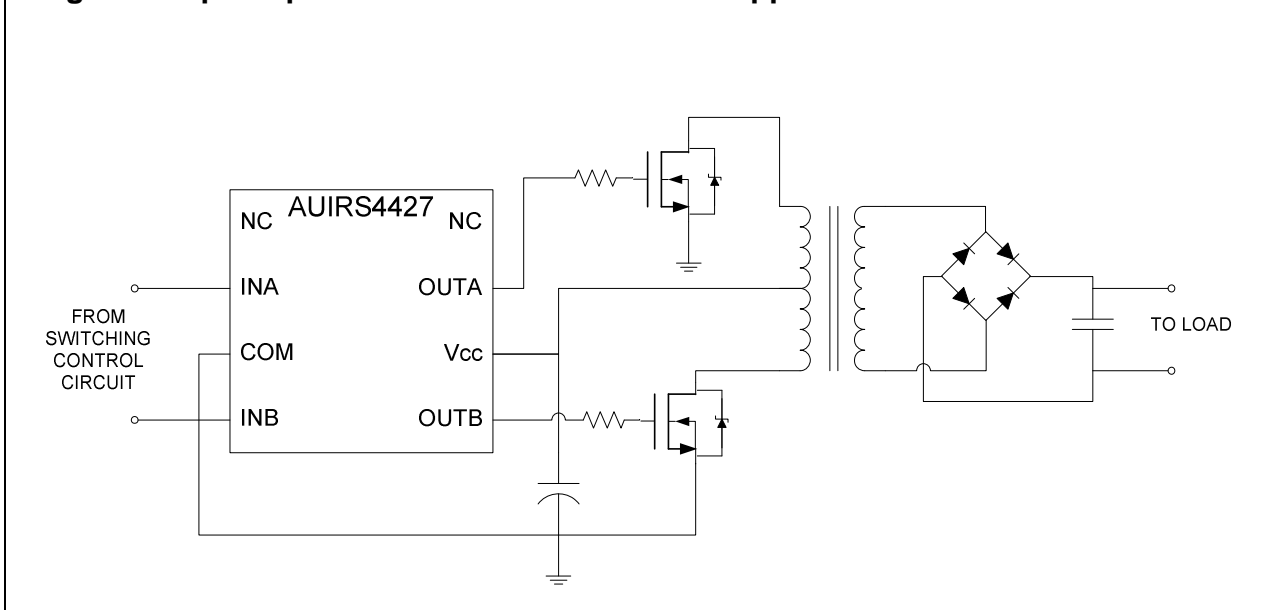


Diagram for push-pull forward DC-DC converter application



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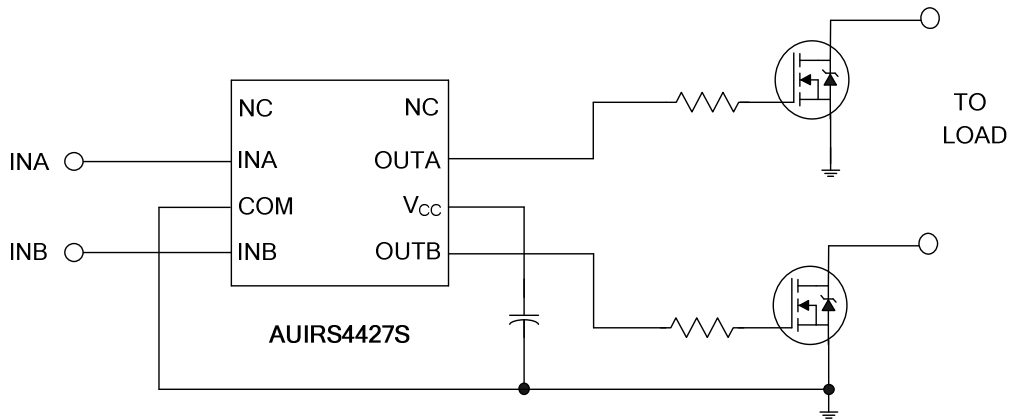
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Description

The AUIRS4427S is a low voltage, high speed power MOSFET and IGBT driver. Proprietary latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL output. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. Propagation delays between two channels are matched.

Typical Connection Diagram



(Refer to Lead Assignments for correct pin configuration). This/These diagram(s) show electrical connections only. Please refer to our Application Notes and Design Tips for proper circuit board layout.

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Qualification Information[†]

Qualification Level		Automotive (per AEC-Q100 ^{††})	
		Comments: This family of ICs has passed an Automotive qualification. IR's Industrial and Consumer qualification level is granted by extension of the higher Automotive level.	
Moisture Sensitivity Level		SOIC8N	MSL3 ^{†††} 260°C (per IPC/JEDEC J-STD-020)
ESD	Machine Model	Class M3 (+/-200V) (per AEC-Q100-003)	
	Human Body Model	Class H3A (+/-4000V) (per AEC-Q100-002)	
	Charged Device Model	Class C5 (+/-1000V) (per AEC-Q100-011)	
IC Latch-Up Test		Class II, Level B (per AEC-Q100-004)	
RoHS Compliant		Yes	

† Qualification standards can be found at International Rectifier's web site <http://www.irf.com/>

†† Exceptions to AEC-Q100 requirements are noted in the qualification report.

††† Higher MSL ratings may be available for the specific package types listed here. Please contact your International Rectifier sales representative for further information.

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Absolute Maximum Ratings

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition	Min	Max	Units
V_{CC}	Fixed supply voltage	-0.3	20	V
V_O	Output voltage	-0.3	$V_{CC} + 0.3$	
V_{IN}	Logic input voltage	-0.3	$V_{CC} + 0.3$	
P_D	Package power dissipation @ $T_A \leq 25^\circ\text{C}$	—	0.625	W
R_{thJA}	Thermal resistance, junction to ambient	—	200	$^\circ\text{C}/\text{W}$
T_J	Junction temperature	—	150	$^\circ\text{C}$
T_S	Storage temperature	-55	150	
T_L	Lead temperature (soldering, 10 seconds)	—	300	

Recommended Operating Conditions

For proper operation, the device should be used within the recommended conditions. All voltage parameters are absolute voltages referenced to COM unless otherwise stated in the table. The offset rating is tested with supply of $V_{CC} = 15\text{V}$.

Symbol	Definition	Min	Max	Units
V_{CC}	Fixed supply voltage	6	20	V
V_O	Output voltage	0	V_{CC}	
V_{IN}	Logic input voltage	0	V_{CC}	
T_A	Ambient temperature	-40	125	$^\circ\text{C}$

Static Electrical Characteristics

$V_{CC} = 15V$, $T_A = 25^\circ C$ unless otherwise specified. The V_{IN} and I_{IN} parameters are referenced to COM and are applicable to input leads: INA and INB. The V_O and I_O parameters are referenced to COM and are applicable to the output leads: OUTA and OUTB.

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
V_{IH}	Logic "1" input voltage	2.5	—	—	V	
V_{IL}	Logic "0" input voltage	—	—	0.8	V	
V_{OH}	High level output voltage, $V_{BIAS} - V_O$	—	—	1.4		$I_O = 0 \text{ mA}$
V_{OL}	Low level output voltage, V_O	—	—	0.15		$I_O = 20 \text{ mA}$
I_{IN+}	Logic "1" input bias current	—	5	15	μA	$V_{IN} = 5V$
I_{IN-}	Logic "0" input bias current	-30	-10	—		$V_{IN} = 0V$
I_{QCC}	Quiescent V_{CC} supply current	—	100	200		$V_{IN} = 0V$ or $5V$
I_{O+}	Output high short circuit pulsed current ^(†)	1.5	2.3	—	A	$V_O = 0V$, $V_{IN} = 5V$ $PW \leq 10 \mu s$
I_{O-}	Output low short circuit pulsed current ^(†)	1.5	3.3	—		$V_O = 15V$, $V_{IN} = COM$ $PW \leq 10 \mu s$

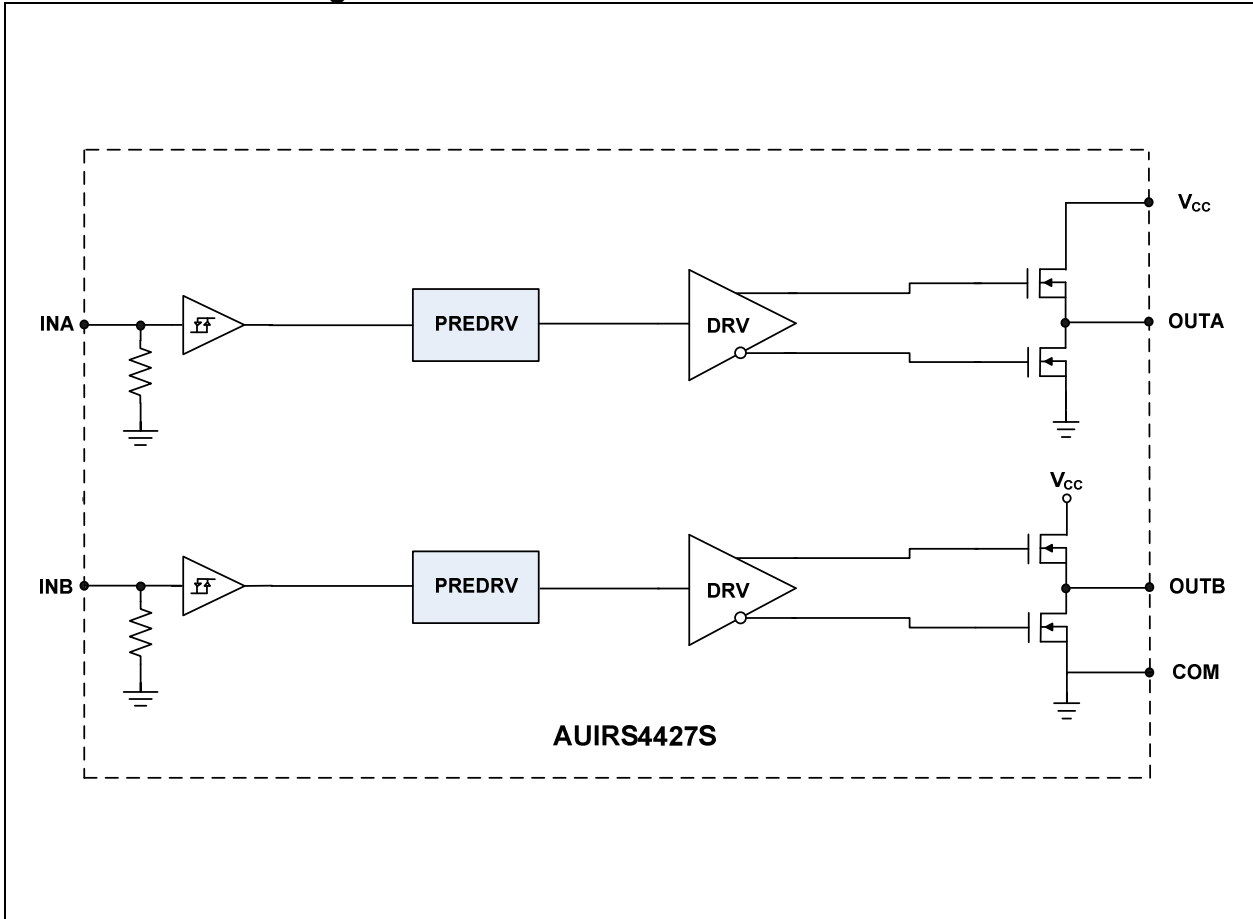
(†) Guaranteed by design

Dynamic Electrical Characteristics

$V_{CC} = 15V$, $T_A = 25^\circ C$, and $C_L = 1000pF$ unless otherwise specified.

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
t_{on}	Turn-on propagation delay	—	50	95	ns	Figure 2
t_{off}	Turn-off propagation delay	—	50	95		
t_r	Turn-on rise time	—	25	55		
t_f	Turn-off fall time	—	25	55		

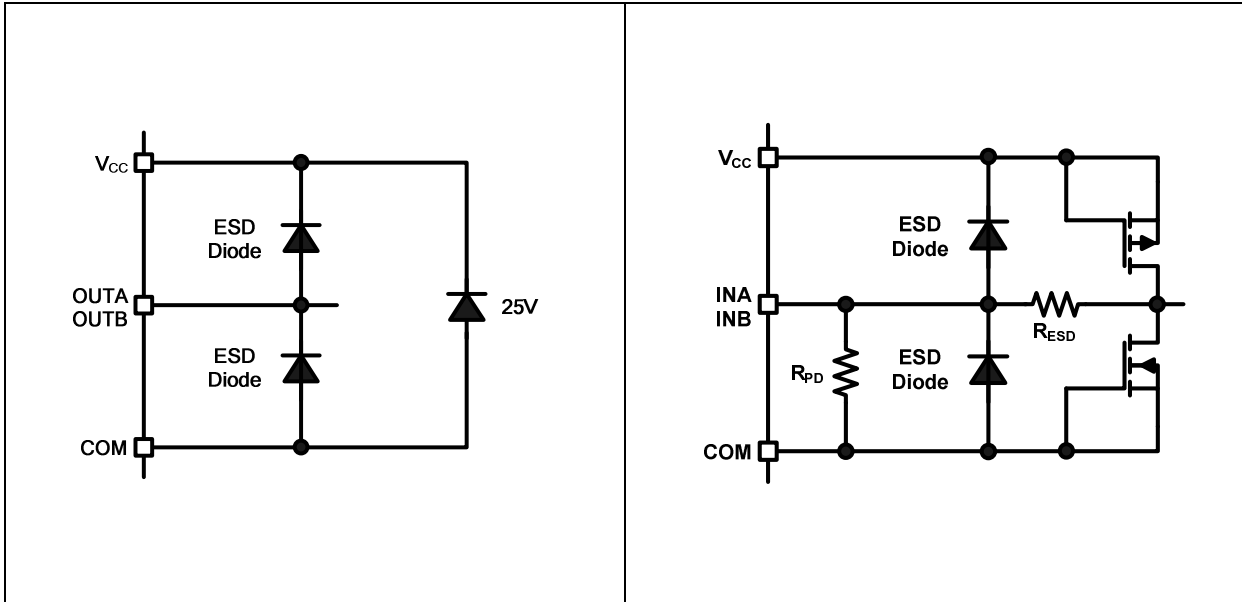
Functional Block Diagram



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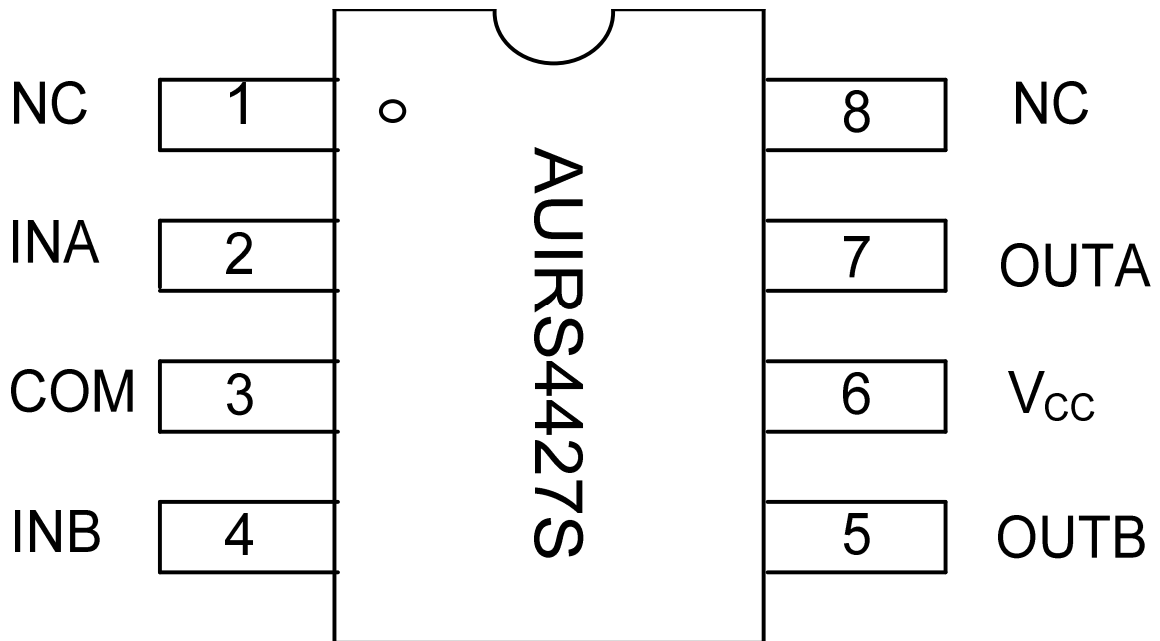
Input/Output Pin Equivalent Circuit Diagrams



Lead Definitions

PIN	Symbol	Description
1	NC	No connection
2	INA	Logic input for gate driver output (OUTA), in phase
3	COM	Ground
4	INB	Logic input for gate driver output (OUTB), in phase
5	OUTB	Gate drive output B
6	V _{CC}	Supply voltage
7	OUTA	Gate drive output A
8	NC	No connection

Lead Assignments



Application Information and Additional Details

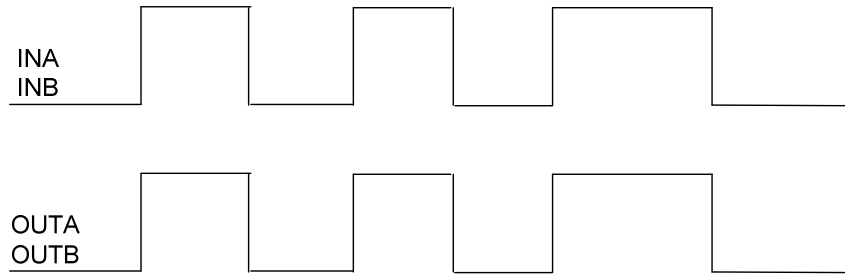


Figure 1: Input/output Timing Diagram

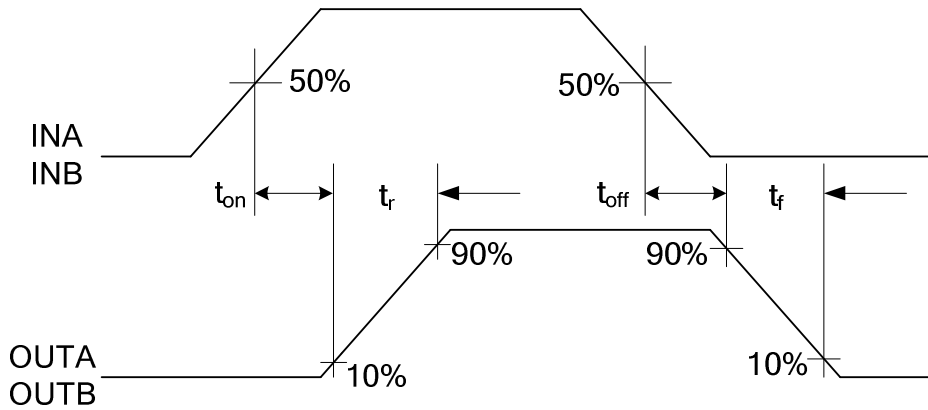


Figure 2: Switching Time Waveform Definitions

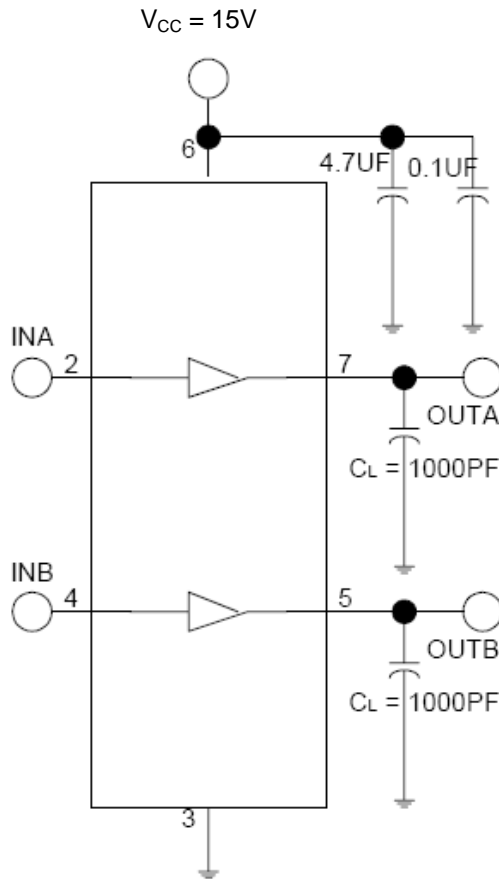


Figure 3: Switching Time Test Circuit

Package Details, SOIC8N

RECOMMENDED FOOTPRINT

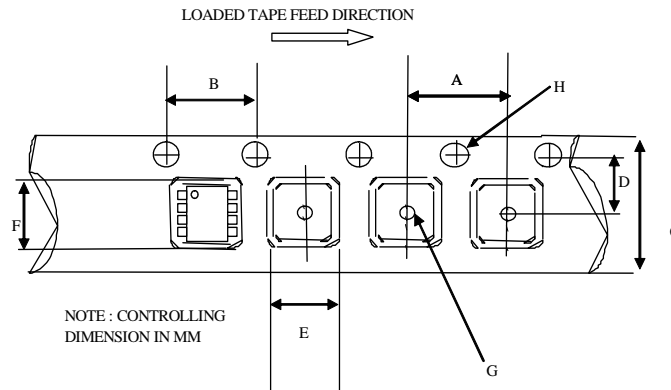
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
B	.014	.018	0.36	0.46
C	.0075	.0098	0.19	0.25
D	.189	.196	4.80	4.98
E	.150	.157	3.81	3.99
e	.050	BASIC	1.27	BASIC
e1	.025	BASIC	0.635	BASIC
H	.2284	.2440	5.80	6.20
K	.011	.019	0.28	0.48
L	.016	.050	0.41	1.27
y	0°	8°	0°	8°

NOTES:

1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.
5. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 [0.006].
6. DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

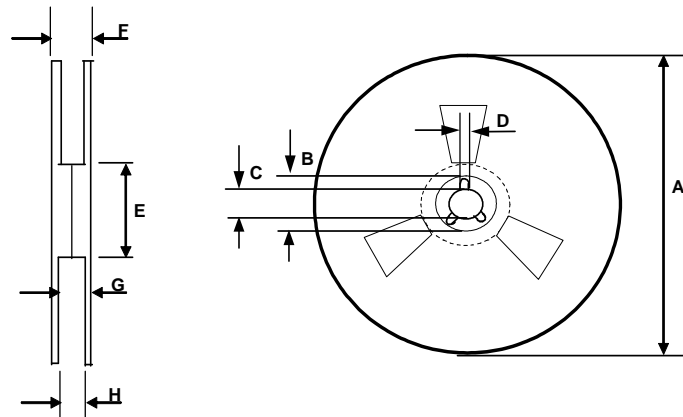
8 Lead SOIC

Package details: SOIC8N, Tape and Reel



CARRIER TAPE DIMENSION FOR 8SOICN

Code	Metric		Imperial	
	Min	Max	Min	Max
A	7.90	8.10	0.311	0.318
B	3.90	4.10	0.153	0.161
C	11.70	12.30	0.46	0.484
D	5.45	5.55	0.214	0.218
E	6.30	6.50	0.248	0.255
F	5.10	5.30	0.200	0.208
G	1.50	n/a	0.059	n/a
H	1.50	1.60	0.059	0.062



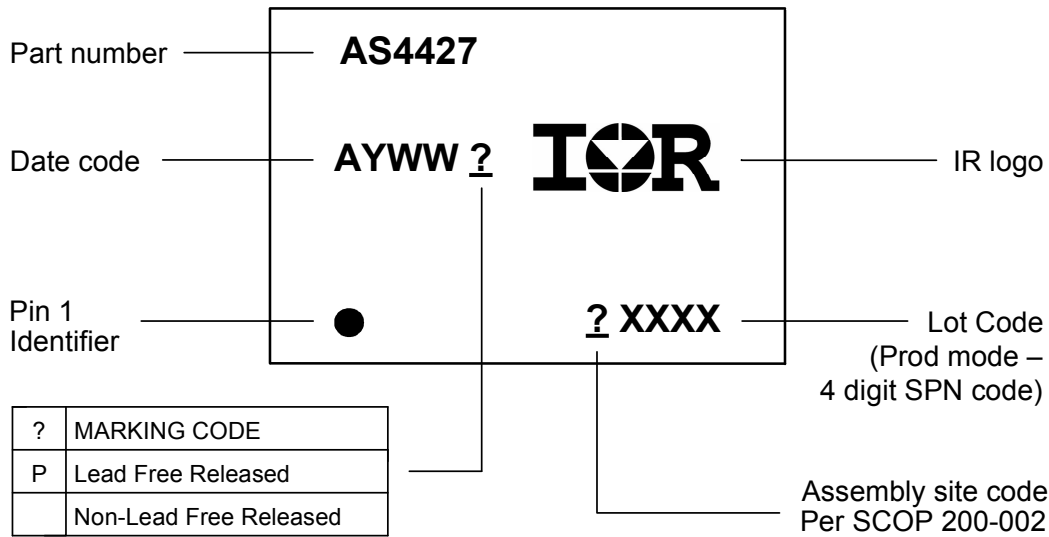
REEL DIMENSIONS FOR 8SOICN

Code	Metric		Imperial	
	Min	Max	Min	Max
A	329.60	330.25	12.976	13.001
B	20.95	21.45	0.824	0.844
C	12.80	13.20	0.503	0.519
D	1.95	2.45	0.767	0.096
E	98.00	102.00	3.858	4.015
F	n/a	18.40	n/a	0.724
G	14.50	17.10	0.570	0.673
H	12.40	14.40	0.488	0.566

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Part Marking Information



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Ordering Information

Base Part Number	Package Type	Standard Pack		Complete Part Number
		Form	Quantity	
AUIRS4427S	SOIC8N	Tube/Bulk	95	AUIRS4427S
		Tape and Reel	2500	AUIRS4427STR

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