Low-Voltage, Low r_{ON}, Single SPDT Analog Switch In SC-89 Package

DESCRIPTION

The DG2011 is a low on-resistance, single-pole/double-throw monolithic CMOS analog switch. It is designed for low voltage applications with guaranteed operation at 2 V. The DG2011 is ideal for portable and battery powered equipment, requiring high performance and efficient use of board space. In additional to the low on-resistance (1.8 Ω at 2.7 V), charge injection is less than 10 pC over the entire analog range.

The switch conducts equally well in both directions when on, and blocks up to the power supply level when off.

The DG2011 is built on Vishay Siliconix's low voltage JI2 process. An epitaxial layer prevents latchup.

Break-before-make is guaranteed.

The DG2011 represents a breakthrough in packaging development for analog switching products. The SC-89 package (1.6 x 1.6 mm^2) – also know as SOT-666 in the industry – reduces board spacing by approximately 40 % while obtaining performance comparable to SC-70 analog switch devices available today.

As a committed partner to the community and the environment, Vishay Siliconix manufactures this product with the lead (Pb)-free device terminations. For analog switching products manufactured with 100 % matte tin device terminations, the lead (Pb)-free "-E3" suffix is being used as a designator.

FEATURES

- Low Voltage Operation (1.8 V to 5.5 V)
- Low On-Resistance - r_{ON}: 1.8 Ω at 2.7 V
- Low Charge Injection
- Low Voltage Logic Compatible
- SC-89 Package (1.6 x 1.6 mm)

Pb-free
Available
RoHS*
COMPLIANT

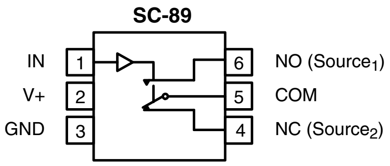
BENEFITS

- Reduced Power Consumption
- Simple Logic Interface
- High Accuracy
- Reduce Board Space
- Guaranteed 2 V Operation

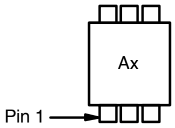
APPLICATIONS

- Cellular Phones
- Communication Systems
- Portable Test Equipment
- Battery Operated Systems
- Sample and Hold Circuits
- ADC and DAC Applications
- Low Voltage Data Acquisition Systems

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



Top View



Device Marking: Ax
x = Date/Lot Traceability Code

TRUTH TABLE

Logic	NC	NO
0	ON	OFF
1	OFF	ON

COMMERCIAL ORDERING INFORMATION

Temp Range	Package	Part Number
- 40 to 85 °C	SC-89 (SOT-666) with Tape and Reel	DG2011DX-T1**
	SC-89 (SOT-666) Lead (Pb)-free with Tape and Reel	DG2011DX-T1-E3** DG2011DXA-T1-E3

** Note:
DG2011DX-T1 and DG2011DX-T1-E3 are not recommended for new designs.

* Pb containing terminations are not RoHS compliant, exemptions may apply.

ABSOLUTE MAXIMUM RATINGS T_A = 25 °C, unless otherwise noted

Parameter		Symbol	Limit	Unit
Reference V+ to GND			- 0.3 to + 6	V
IN, COM, NC, NO[a]			- 0.3 to (V+ + 0.3 V)	
Continuous Current (NO, NC, COM pins)			± 150	mA
Peak Current (Pulsed at 1 ms, 10 % duty cycle)			± 300	
Storage Temperature	D Suffix		- 65 to 150	°C
Power Dissipation (Packages)[b]	SC-89[c]		172	mW

Notes:

a. Signals on NC, NO, or COM or IN exceeding V+ will be clamped by internal diodes. Limit forward diode current to maximum current ratings.

b. All leads welded or soldered to PC Board.

c. Derate 2.15 mW/°C above 70 °C.

SPECIFICATIONS (V+ = 2.0 V)

Parameter	Symbol	Test Conditions Otherwise Unless Specified V+ = 2.0 V, V_{IN} = 0.4 V or 1.6 V[e]	Temp[a]	Limits - 40 to 85 °C			Unit
				Min[b]	Typ[c]	Max[b]	
Analog Switch							
Analog Signal Range[d]	V_{NO}, V_{NC}, V_{COM}		Full	0		V+	V
On-Resistance	r_{ON}	V+ = 2.0 V, V_{COM} = 0.2 V/0.9 V I_{NO}, I_{NC} = 20 mA	Room Full		3.5	5.5 5.5	Ω
Switch Off Leakage Current[f]	$I_{NO(off)}$ $I_{NC(off)}$	V+ = 2.2 V, V_{NO}, V_{NC}= 0.5 V/1.5 V, V_{COM} = 1.5 V/0.5 V	Room Full	- 1 - 10		1 10	nA
	$I_{COM(off)}$		Room Full	- 1 - 10		1 10	
Channel-On Leakage Current[f]	$I_{COM(on)}$	V+ = 2.2 V, V_{NO}, V_{NC} = V_{COM} = 0.5 V/1.5 V	Room Full	- 1 - 10		1 10	
Digital Control							
Input High Voltage	V_{INH}		Full	1.5			V
Input Low Voltage	V_{INL}		Full			0.4	
Input Capacitance	C_{in}		Full		4		pF
Input Current	I_{INL} or I_{INH}	V_{IN} = 0 or V+	Full	1		1	µA
Dynamic Characteristics							
Turn-On Time	t_{ON}	V_{NO} or V_{NC} = 1.5 V, R_L = 300 Ω, C_L = 35 pF	Room Full		75	110 113	ns
Turn-Off Time	t_{OFF}		Room Full		37	71 76	
Break-Before-Make Time	t_{BBM}		Room	1	37		
Charge Injection[d]	Q_{INJ}	C_L = 1 nF, V_{GEN} = 0 V, R_{GEN} = 0 Ω	Room		7		pC
Off-Isolation[d]	OIRR	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz	Room		- 62		dB
Crosstalk[d]	X_{TALK}		Room		- 69		
N_O, N_C Off Capacitance[d]	$C_{NO(off)}$ $C_{NC(off)}$	V_{IN} = 0 or V+, f = 1 MHz	Room		29		pF
Channel-On Capacitance[d]	C_{ON}		Room		85		
Power Supply							
Positive Supply Range	V+	V_{IN} = 0 or V+		1.8		5.5	V
Negative Supply Current	I+				0.01	1.0	µA

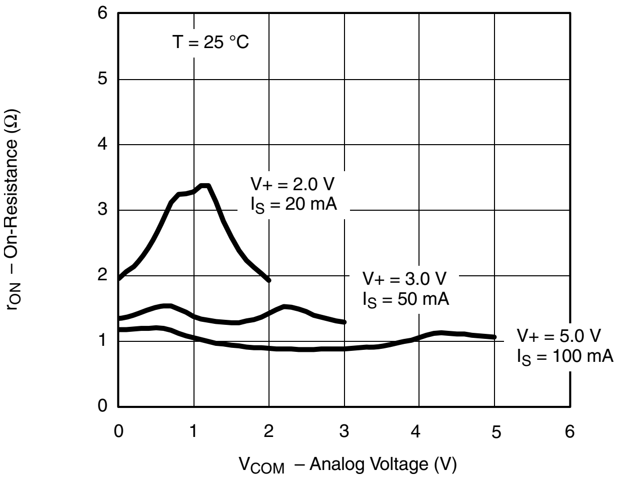
SPECIFICATIONS (V+ = 3 V)

Parameter	Symbol	Test Conditions Otherwise Unless Specified V+ = 3 V, ±10 %, V_{IN} = 0.4 V or 2.0 V[e]	Temp[a]	Limits –40 to 85 °C			Unit
				Min[b]	Typ[c]	Max[b]	
Analog Switch							
Analog Signal Range[d]	V_{NO}, V_{NC}, V_{COM}		Full	0		V+	V
On-Resistance	r_{ON}	V+ = 2.7 V, V_{COM} = 0.9 V/1.5 V I_{NO}, I_{NC} = 50 mA	Room Full		1.8	2.7 2.9	Ω
r_{ON} Match	Δr_{ON}		Room			0.2	
r_{ON} Flatness	r_{ON} Flatness		Room		0.2	0.5	
Switch Off Leakage Current	$I_{NO(off)}$ $I_{NC(off)}$	V+ = 3.3 V, V_{NO}, V_{NC}= 1 V/3 V, V_{COM} = 3 V/1 V	Room Full	- 1 - 10		1 10	nA
	$I_{COM(off)}$		Room Full	- 1 - 10		1 10	
Channel-On Leakage Current[f]	$I_{COM(on)}$	V+ = 3.3 V, V_{NO}, V_{NC} = V_{COM} = 1 V/3 V	Room Full	- 1 - 10		1 10	
Digital Control							
Input High Voltage	V_{INH}		Full	1.6			V
Input Low Voltage	V_{INL}		Full			0.4	
Input Capacitance	C_{in}		Full		4		pF
Input Current	I_{INL} or I_{INH}	V_{IN} = 0 or V+	Full	1		1	µA
Dynamic Characteristics							
Turn-On Time	t_{ON}	V_{NO} or V_{NC} = 2.0 V, R_L = 300 Ω, C_L = 35 pF	Room Full		45	75 77	ns
Turn-Off Time	t_{OFF}		Room Full		29	59 62	
Break-Before-Make Time	t_{BBM}		Room	1	16		
Charge Injection[d]	Q_{INJ}	C_L = 1 nF, V_{GEN} = 0 V, R_{GEN} = 0 Ω	Room		2		pC
Off-Isolation[d]	OIRR	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz	Room		- 62		dB
Crosstalk[d]	X_{TALK}		Room		- 68		
N_O, N_C Off Capacitance[d]	$C_{NO(off)}$ $C_{NC(off)}$	V_{IN} = 0 or V+, f = 1 MHz	Room		28		pF
Channel-On Capacitance[d]	C_{ON}		Room		84		
Power Supply							
Power Supply Range	V+			1.8		5.5	V
Power Supply Current	I+	V_{IN} = 0 or V+			0.01	1.0	µA
Power Consumption	P_C					3.3	µW

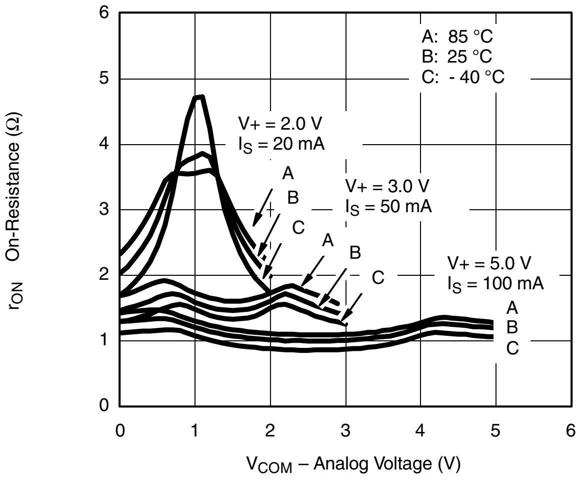
Notes:
a. Room = 25 °C, Full = as determined by the operating suffix.
b. Typical values are for design aid only, not guaranteed nor subject to production testing.
c. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
d. Guarantee by design, nor subjected to production test.
e. V_{IN} = input voltage to perform proper function.
f. Guaranteed by 5 V leakage testing, not production tested.

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

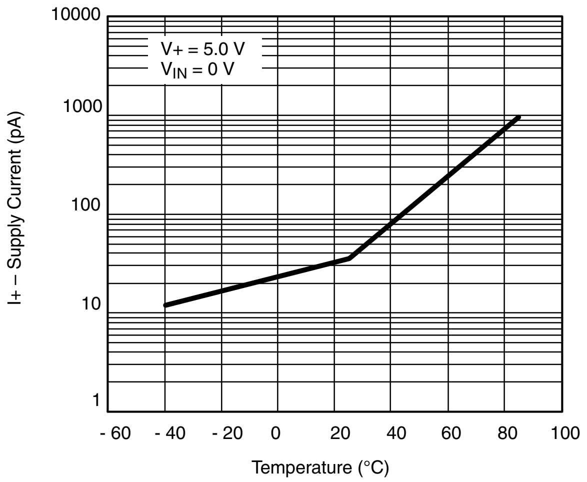
TYPICAL CHARACTERISTICS T_A = 25 °C, unless otherwise noted



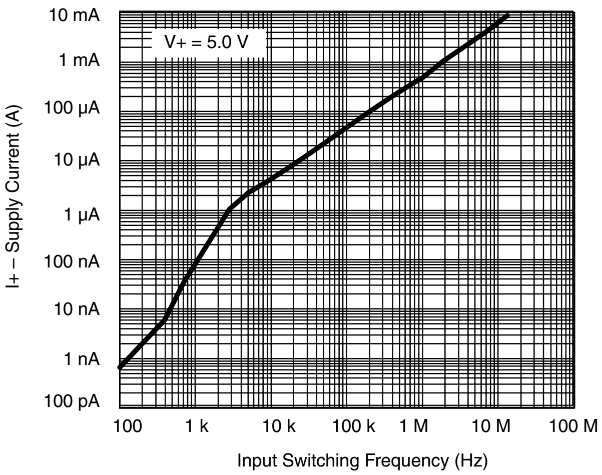
r_{ON} vs. V_{COM} and Supply Voltage



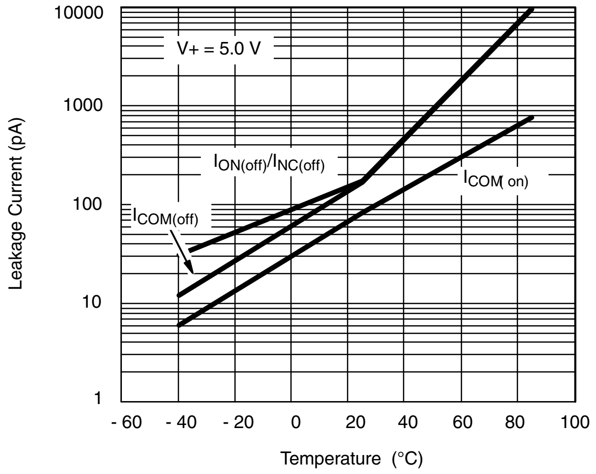
r_{ON} vs. Analog Voltage and Temperature



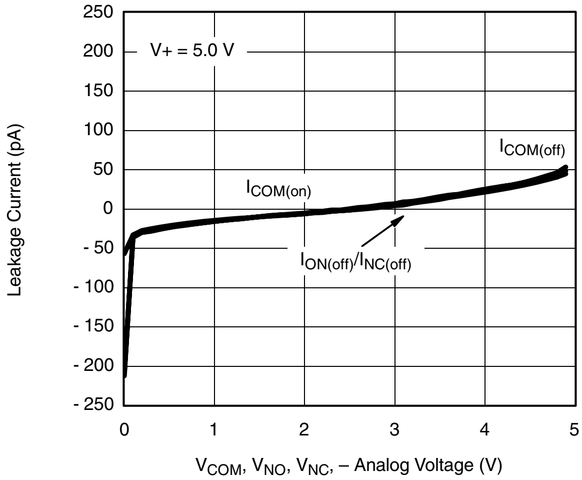
Supply Current vs. Temperature



Supply Current vs. Input Switching Frequency

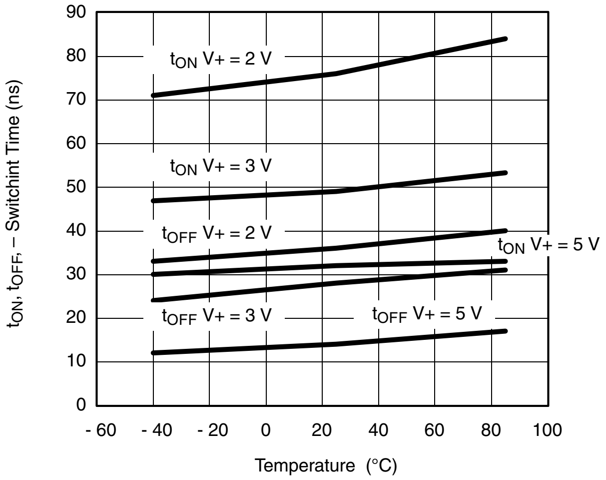


Leakage Current vs. Temperature

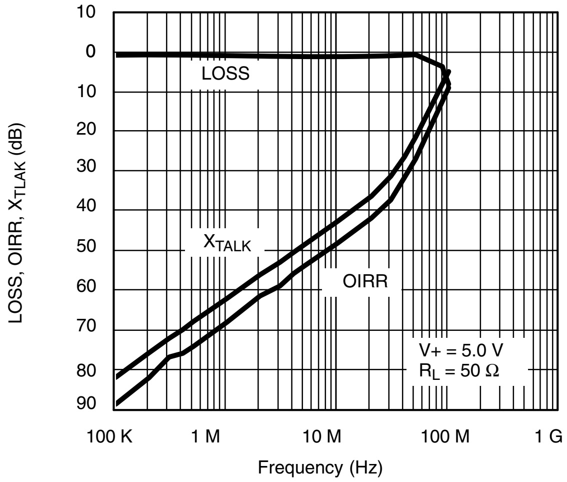


Leakage vs. Analog Voltage

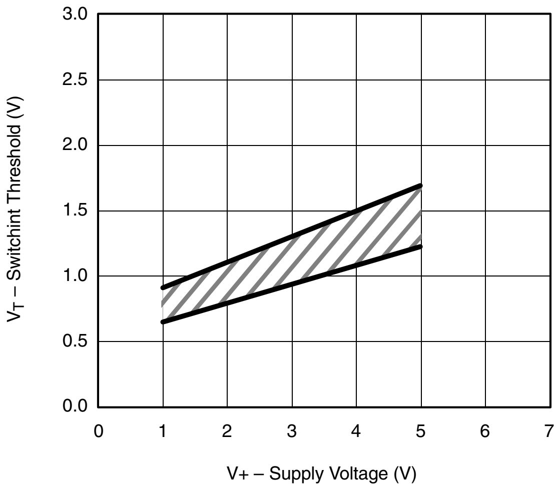
TYPICAL CHARACTERISTICS T_A = 25 °C, unless otherwise noted



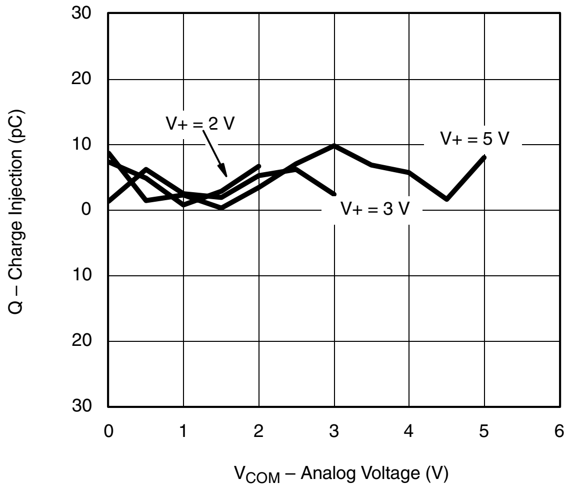
Switching Time vs. Temperature and Supply Voltage



Insertion Loss, Off-Isolation, Crosstalk vs. Frequency

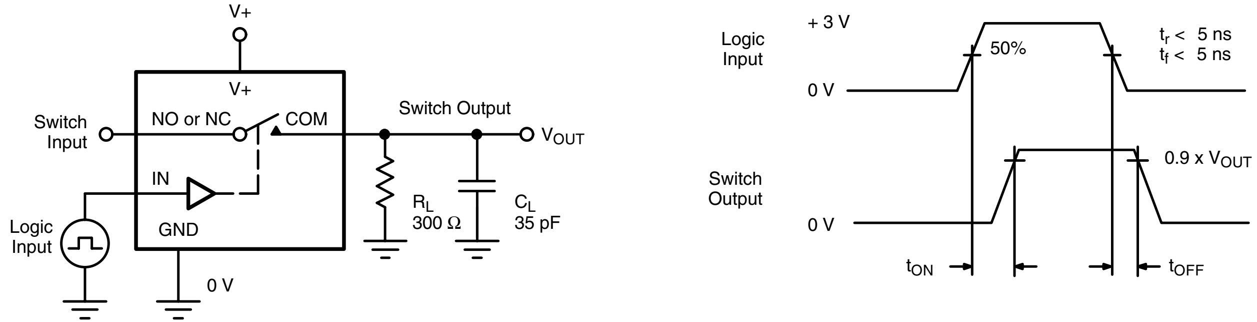


Switching Threshold vs. Supply Voltage



Charge Injection vs. Analog Voltage

TEST CIRCUITS

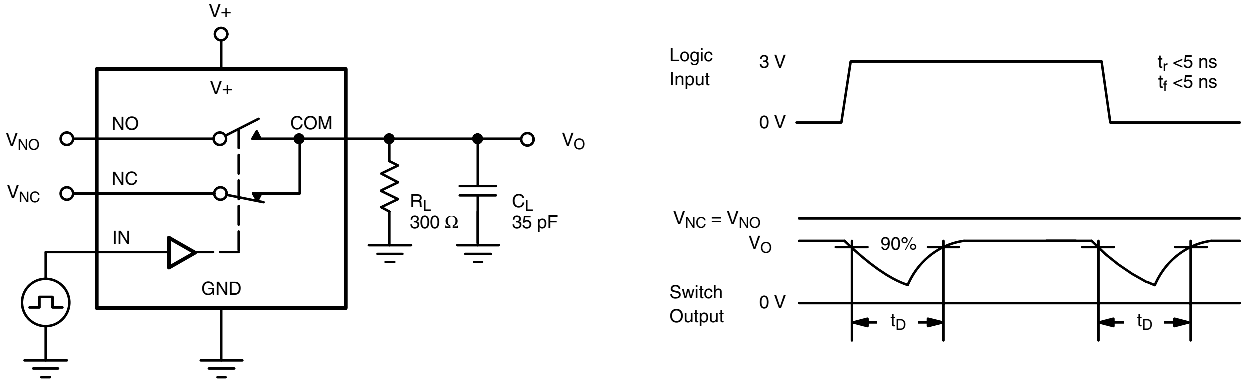


C_L (includes fixture and stray capacitance)

$$V_{OUT} = V_{COM}\left(\frac{R_L}{R_L + R_{ON}}\right)$$

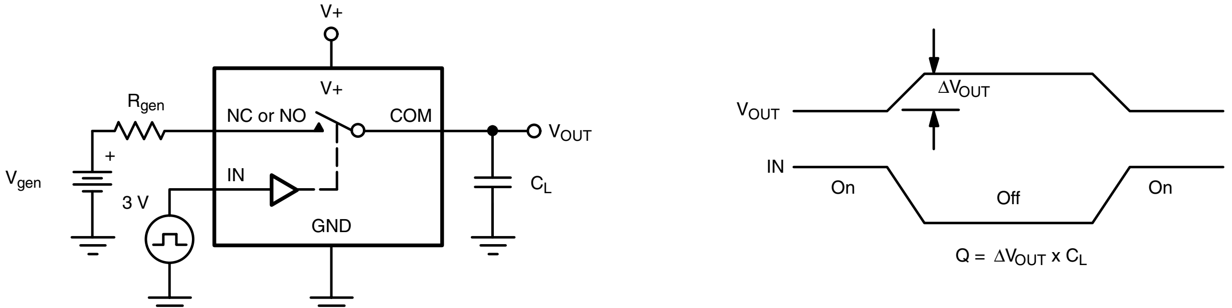
Logic "1" = Switch On
Logic input waveforms inverted for switches that have the opposite logic sense.

Figure 1. Switching Time



C_L (includes fixture and stray capacitance)

Figure 2. Break-Before-Make Interval



$Q = \Delta V_{OUT} \times C_L$

IN depends on switch configuration: input polarity determined by sense of switch.

Figure 3. Charge Injection

TEST CIRCUITS

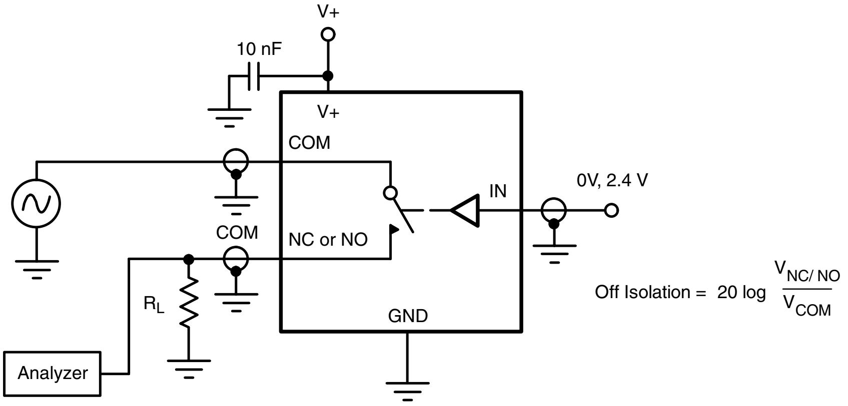


Figure 4. Off-Isolation

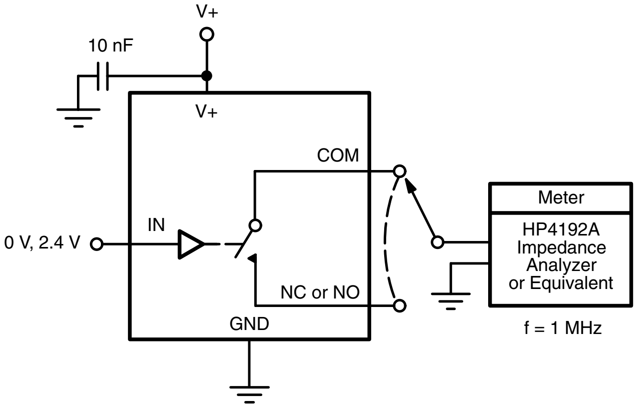


Figure 5. Channel Off/On Capacitance

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