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[DG2753DN-T1-E4](#)

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## Low Voltage, 0.7 Ω, Triple SPDT Analog Switch

### DESCRIPTION

The DG2753 is a low voltage, low on-resistance, triple single-pole/double-throw (SPDT) monolithic CMOS analog switch. The device is designed for operation from 1.65 V to 4.3 V single supply. The device is 1.8 V logic compatible within the full operation voltage range to interface with low voltage DSP or MCU control logic. These traits make it ideal for one cell Li-ion battery direct power in portable applications.

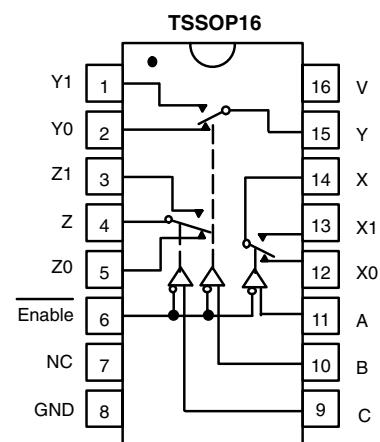
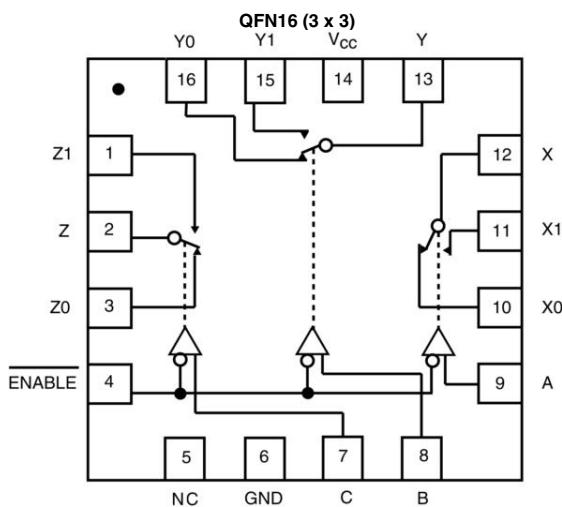
The DG2753 fully guarantees operation when V+ is as low as 1.8 V. When powered from a 3 V power supply, it has a 0.9 Ω on-resistance, with 0.1 Ω  $R_{ON}$  matching between channels, and 0.2 Ω (Max)  $R_{ON}$  flatness.

Each switch conducts signals across power rails equally well in both directions when on, and blocks up to the power supply level when off. It offers 30 nS  $T_{on}$  and 10 nS  $T_{off}$ . Break-before-make is guaranteed.

The DG2753 is built on Vishay Siliconix's low voltage process. An epitaxial layer prevents latchup.

It is available in QFN16 3 x 3 mm and TSSOP16 packages. As a committed partner to the community and the environment, Vishay Siliconix manufactures this product with lead (Pb)-free device terminations. For analog switching products manufactured in QFN packages, the lead (Pb)-free "-E4" suffix is being used as a designator for nickel-palladium-gold. The TSSOP-16 package is offered in lead (Pb)-free with 100 % matte Tin terminations. The "-E3" suffix is the designator. Both the 100 % matte Tin and nickel-palladium gold device terminations meet all JEDEC standards for reflow and MSL ratings.

### FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



### ORDERING INFORMATION

| Temp Range    | Package                              | Part Number    |
|---------------|--------------------------------------|----------------|
| - 40 to 85 °C | TSSOP-16                             | DG2753DQ-T1-E3 |
| - 40 to 85 °C | 16-Pin QFN (3 mm x 3 mm) Variation 2 | DG2753DN-T1-E4 |

## DG2753

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### TRUTH TABLE

| Enable Input | Select Inputs |   |   | ON Switches       |
|--------------|---------------|---|---|-------------------|
|              | C             | B | A | DG2753            |
| H            | X             | X | X | All switches open |
| L            | X             | X | L | X - X0            |
| L            | X             | X | H | X - X1            |
| L            | X             | L | X | Y - Y0            |
| L            | X             | H | X | Y - Y1            |
| L            | L             | X | X | Z - Z0            |
| L            | H             | X | X | Z - Z1            |

X = Do not care

### ABSOLUTE MAXIMUM RATINGS $T_A = 25^\circ\text{C}$ , unless otherwise noted

| Parameter                                      | Limit                        |                     | Unit |
|--|------------------------------|---------------------|------|
| Reference to GND                               | V+                           | - 0.3 to 5.0        | V    |
|  | IN, COM, NC, NO <sup>a</sup> | - 0.3 to (V+ + 0.3) |      |
| Current (Any terminal except NO, NC or COM)    | 30                           | mA                  |      |
| Continuous Current (NO, NC, or COM)            | $\pm 300$                    |                     |      |
| Peak Current (Pulsed at 1 ms, 10 % duty cycle) | $\pm 500$                    |                     |      |
| Storage Temperature (D Suffix)                 | - 65 to 150                  | °C                  |      |
| Package Solder Reflow Conditions <sup>d</sup>  | 250                          |                     |      |
| Power Dissipation (Packages) <sup>b</sup>      | 1385                         | mW                  |      |

Notes:

- a. Signals on NC, NO, or COM or IN exceeding V+ will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
- b. All leads welded or soldered to PC Board.
- c. Derate 17.3 mW/°C above 70 °C.
- d. Manual soldering with iron is not recommended for leadless components. The QFN is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper lip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

### SPECIFICATIONS

| Parameter                        | Symbol                          | Test Conditions<br>Otherwise Unless Specified<br>V+, $\pm 10\%$ , $V_{IN} = 0.4$ or $1.8\text{ V}^e$          | Temp <sup>a</sup> | Limits           |                  |                  | Unit        |
|----------------------------------|---------------------------------|---|-------------------|------------------|------------------|------------------|-------------|
|                                  |                                 |   |                   | Min <sup>b</sup> | Typ <sup>c</sup> | Max <sup>b</sup> |             |
| <b>Analog Switch</b>             |                                 |   |                   |                  |                  |                  |             |
| Analog Signal Range <sup>d</sup> | $V_{NO}$ , $V_{NC}$ , $V_{COM}$ |   | Full              | 0                |                  | $V_+$            | V           |
| On-Resistance                    | $r_{DS(on)}$                    | $V_+ = 2.7\text{ V}$ , $I_{NO/NC} = 100\text{ mA}$ , $V_{COM} = 1.7\text{ V}$                                 | Room              |                  | 0.9              | 1.3              | $\Omega$    |
|                                  |                                 | $V_+ = 2.7\text{ V}$ , $I_{NO/NC} = 100\text{ mA}$ , $V_{COM} = 1.7\text{ V}$                                 | Full              |                  |                  | 1.5              |             |
|                                  |                                 | $V_+ = 4.2\text{ V}$ , $I_{NO/NC} = 100\text{ mA}$ , $V_{COM} = 2.1\text{ V}$                                 | Room              |                  | 0.7              | 1.2              |             |
|                                  |                                 | $V_+ = 4.2\text{ V}$ , $I_{NO/NC} = 100\text{ mA}$ , $V_{COM} = 2.1\text{ V}$                                 | Full              |                  |                  | 1.4              |             |
| $r_{ON}$ Match                   | $\Delta r_{(on)}$               | $V_+ = 2.7\text{ V}$ , $I_{NO/NC} = 100\text{ mA}$ , $V_{COM} = 1.7\text{ V}$                                 | Room              |                  |                  | 0.4              |             |
|                                  |                                 | $V_+ = 4.3\text{ V}$ , $I_{NO/NC} = 100\text{ mA}$ , $V_{COM} = 2.1\text{ V}$                                 | Room              |                  |                  | 0.6              |             |
| $r_{ON}$ Resistance Flatness     | $r_{(on)}$ Flatness             | $V_+ = 2.7\text{ V}$ , $I_{NO/NC} = 100\text{ mA}$ , $V_{COM} = 1.7\text{ V}$                                 | Room              |                  |                  | 0.2              |             |
| Switch Off Leakage Current       | $I_{NO(off)}$                   | $V_+ = 4.3\text{ V}$ , $V_{NO}$ , $V_{NC} = 4\text{ V}/0.3\text{ V}$ ,<br>$V_{COM} = 0.3\text{ V}/4\text{ V}$ | Room              | - 2              |                  | 2                | $\text{nA}$ |
|                                  |                                 |   | Full              | - 25             |                  | 25               |             |
| Channel-On Leakage Current       | $I_{COM(on)}$                   | $V_+ = 4.3\text{ V}$ , $V_{COM} = V_{NO}$ , $V_{NC} = 0.3\text{ V}/4\text{ V}$                                | Room              | - 2              |                  | 2                |             |
|                                  |                                 |   | Full              | - 10             |                  | 10               |             |



| <b>SPECIFICATIONS</b>                   |                    |   |      |                         |                        |                        |                        |
|---|--------------------|---|------|-------------------------|------------------------|------------------------|------------------------|
| <b>Parameter</b>                        | <b>Symbol</b>      | <b>Test Conditions<br/>Otherwise Unless Specified</b>   |      | <b>Temp<sup>a</sup></b> | <b>Limits</b>          |                        |                        |
|   |                    | $V_+ \pm 10\%, V_{IN} = 0.4 \text{ or } 1.8 \text{ V}^e$  |      |                         | <b>Min<sup>b</sup></b> | <b>Typ<sup>c</sup></b> | <b>Max<sup>b</sup></b> |
| <b>Digital Control</b>                  |                    |   |      |                         |                        |                        |                        |
| Input High Voltage                      | $V_{INH}$          | $V_+ = 1.8 \text{ V}$   | Full | 1                       |                        |                        | $\text{V}$             |
|   |                    | $V_+ = 3 \text{ V}$   | Full | 1.4                     |                        |                        |                        |
|   |                    | $V_+ = 4.3 \text{ V}$   | Full | 1.8                     |                        |                        |                        |
| Input Low Voltage                       | $V_{INL}$          | $V_+ = 1.8 \text{ V}$   | Full |                         |                        | 0.4                    |                        |
|   |                    | $V_+ = 3 \text{ V}$   | Full |                         |                        | 0.5                    |                        |
|   |                    | $V_+ = 4.3 \text{ V}$   | Full |                         |                        | 0.5                    |                        |
| Input Current                           | $I_{INL}, I_{INH}$ | $V_{IN} = 0 \text{ V or } V_+$  | Full | - 1                     |                        | 1                      | $\mu\text{A}$          |
| <b>Dynamic Characteristics</b>          |                    |   |      |                         |                        |                        |                        |
| Turn-On Time                            | $t_{ON}$           | $V_+ = 2.7 \text{ V}$<br>$V_{NO}, V_{NC} = 1.5 \text{ V}, R_L = 50 \Omega, C_L = 35 \text{ pF}$   | Room |                         | 30                     | 60                     | $\text{ns}$            |
| Turn-Off Time                           | $t_{OFF}$          |   | Room |                         | 10                     | 30                     |                        |
| Break-Before-Make                       | $t_{OPEN}$         | $V_+ = 2.7 \text{ V}$<br>$V_{NO}, V_{NC} = 1.5 \text{ V}, R_L = 50 \Omega, C_L = 35 \text{ pF}$   | Full | 5                       | 30                     |                        | $\text{pC}$            |
| Address Transition Time                 | $t_{TRANS}$        |   | Full |                         | 40                     | 80                     |                        |
| Charge Injection <sup>d</sup>           | $Q_{INJ}$          | $V_+ = 2.7 \text{ V}, C_L = 1 \text{ nF}, R_{GEN} = 0 \Omega, f = 500 \text{ kHz}$<br>$V_{NC}, V_{NO} = 2 \text{ V}$ (test at COM side) | Room |                         | - 25                   |                        | $\text{dB}$            |
| Off-Isolation <sup>d</sup>              | $O_{IRR}$          | $V_+ = 2.7 \text{ V}, C_L = 1 \text{ nF}, R_{GEN} = 0 \Omega, f = 500 \text{ kHz}$<br>$V_{NC}, V_{NO} = 2 \text{ V}$ (test at COM side) | Room |                         | - 90                   |                        |                        |
| Crosstalk <sup>d</sup>                  | $X_{TALK}$         | $V_+ = 2.7 \text{ V}, C_L = 1 \text{ nF}, R_{GEN} = 0 \Omega$<br>$V_{NC}, V_{NO} = 2 \text{ V}$ (test at COM side)                      | Room |                         | - 90                   |                        | $\text{pF}$            |
| $N_O, N_C$ Off Capacitance <sup>d</sup> | $C_{NO(off)}$      | $V_{IN} = 0 \text{ or } V_+, f = 1 \text{ MHz}$   | Room |                         | 35                     |                        |                        |
|   | $C_{NC(off)}$      |   | Room |                         | 35                     |                        |                        |
| Channel/On Capacitance <sup>d</sup>     | $C_{NO(on)}$       |   | Room |                         | 80                     |                        |                        |
|   | $C_{NC(on)}$       |   | Room |                         | 80                     |                        |                        |
| <b>Power Supply</b>                     |                    |   |      |                         |                        |                        |                        |
| Power Supply Current                    | $I_+$              | $V_{IN} = 0 \text{ or } V_+$  | Full |                         |                        | 1                      | $\mu\text{A}$          |

Notes:

- Room = 25 °C, Full = as determined by the operating suffix.
- Typical values are for design aid only, not guaranteed nor subject to production testing.
- The algebraic convention where by the most negative value is a minimum and the most positive a maximum, is used in this datasheet.
- Guarantee by design, not subjected to production test.
- $V_{IN}$  = input voltage to perform proper function.

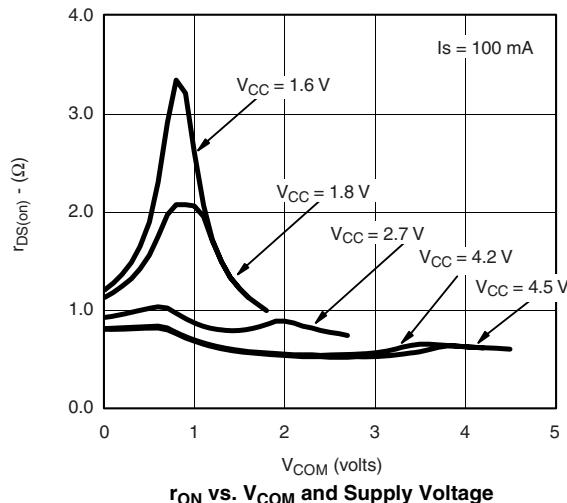
*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

# DG2753

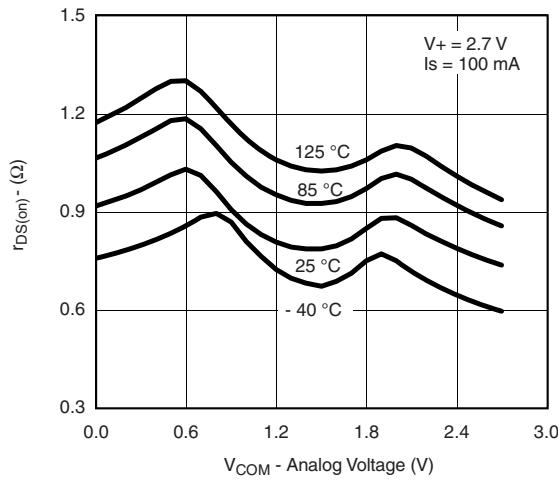
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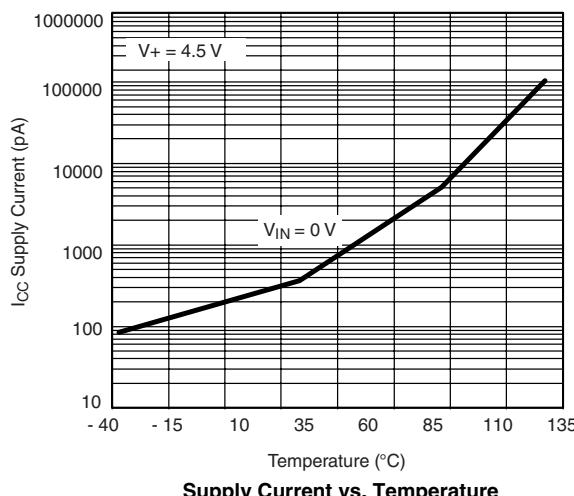
**TYPICAL CHARACTERISTICS**  $T_A = 25^\circ\text{C}$ , unless otherwise noted



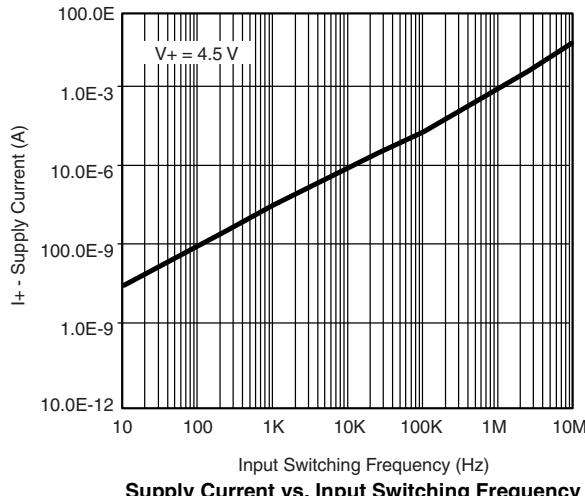
**$r_{\text{ON}}$  vs.  $V_{\text{COM}}$  and Supply Voltage**



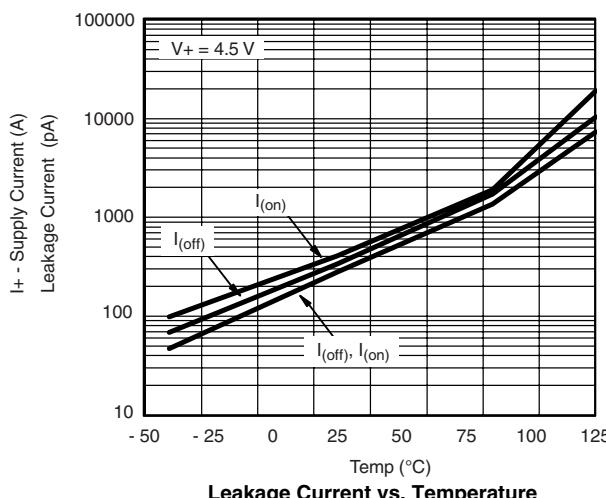
**$r_{\text{ON}}$  vs. Analog Voltage and Temperature**



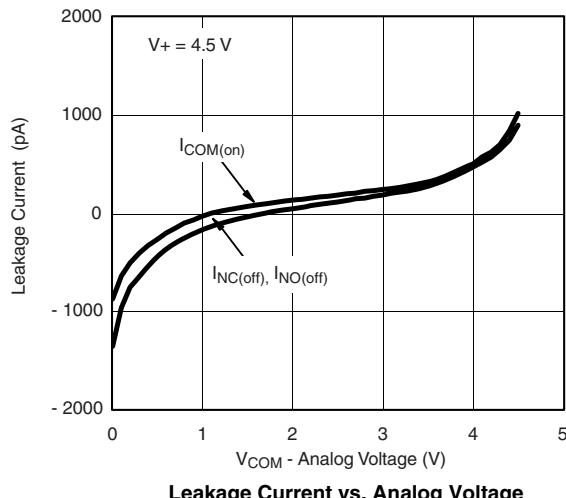
**Supply Current vs. Temperature**



**Supply Current vs. Input Switching Frequency**



**Leakage Current vs. Temperature**



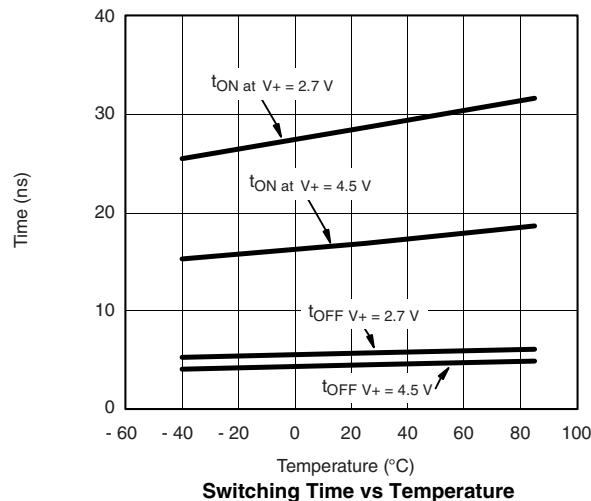
**Leakage Current vs. Analog Voltage**



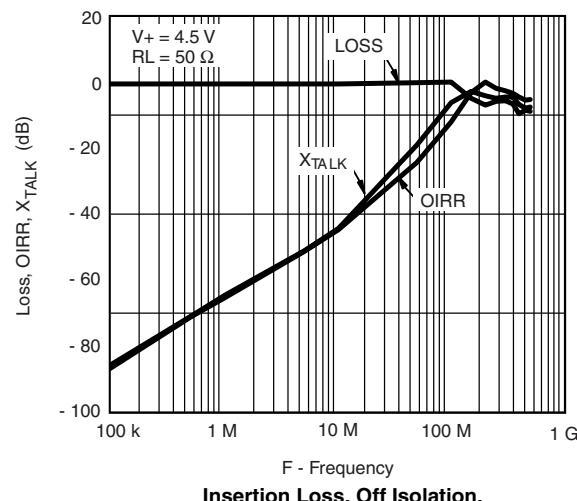
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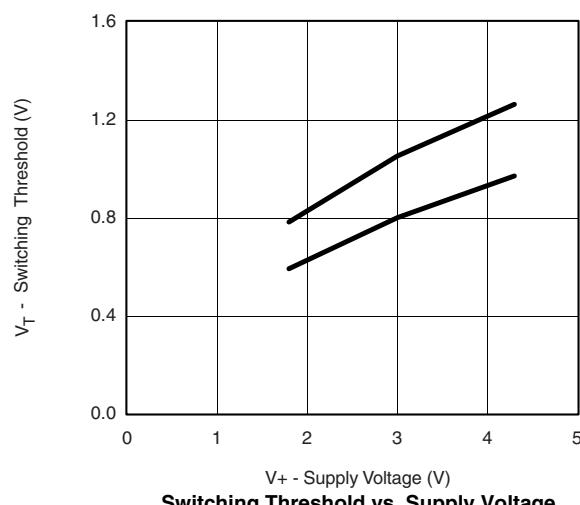
**TYPICAL CHARACTERISTICS**  $T_A = 25^\circ\text{C}$ , unless otherwise noted



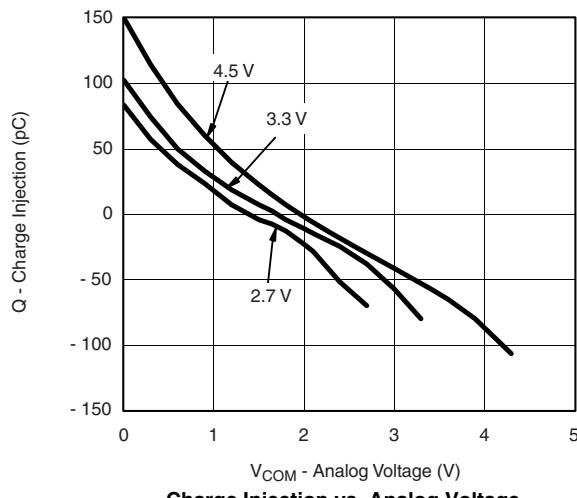
Switching Time vs Temperature



Insertion Loss, Off Isolation,  
Cross Talk vs. Frequency



Switching Threshold vs. Supply Voltage



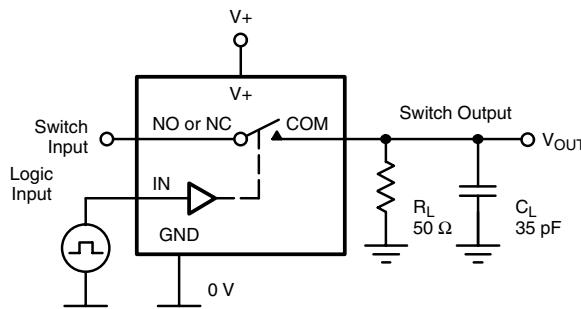
Charge Injection vs. Analog Voltage

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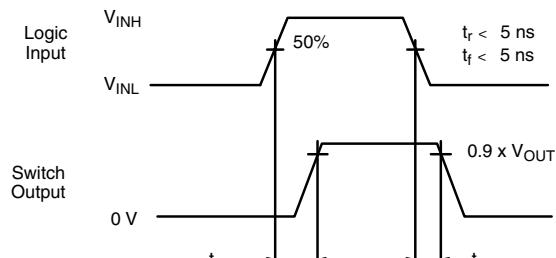


### TEST CIRCUITS



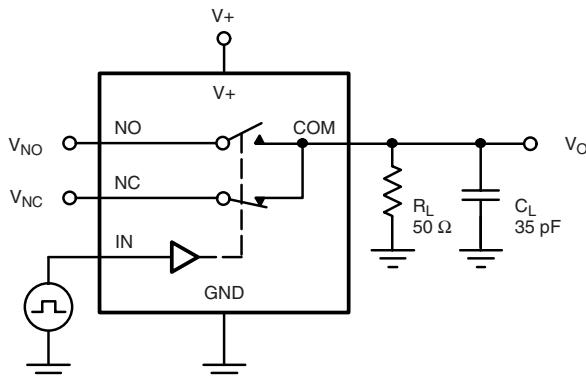
$C_L$  (includes fixture and stray capacitance)

$$V_{OUT} = V_{COM} \left( \frac{R_L}{R_L + R_{ON}} \right)$$



Logic "1" = Switch On  
Logic input waveforms inverted for switches that have the opposite logic sense.

Figure 1. Switching Time



$C_L$  (includes fixture and stray capacitance)

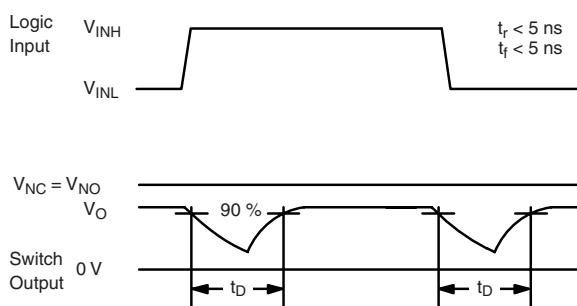
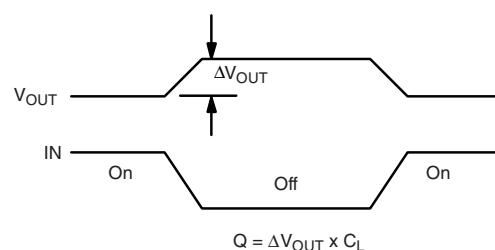
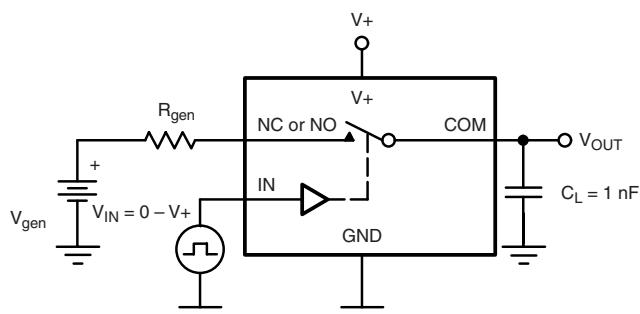


Figure 2. Break-Before-Make Interval



IN depends on switch configuration: input polarity determined by sense of switch.

Figure 3. Charge Injection



**TEST CIRCUITS**

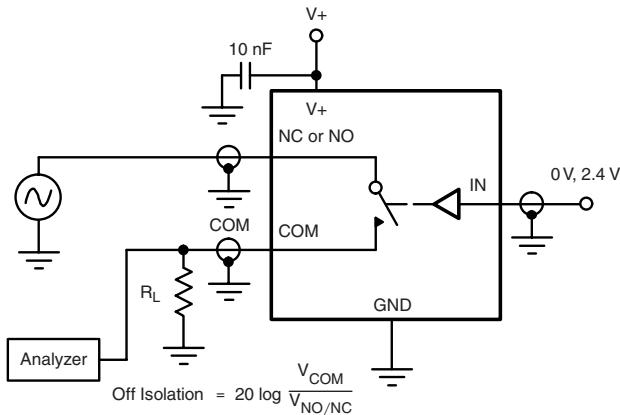


Figure 4. Off-Isolation

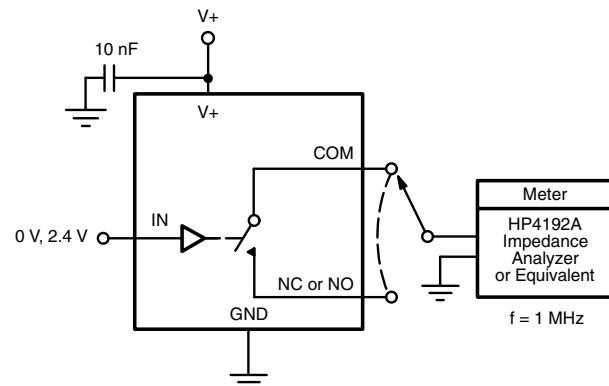


Figure 5. Channel Off/On Capacitance

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