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Vishay/Siliconix
DG458DJ-E3

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Fault-Protected Single 8-Ch/Differential 4-Ch Analog Multiplexers

DESCRIPTION

The DG458 and DG459 are 8-channel single-ended and 4-channel differential analog multiplexers, respectively, incorporating fault protection. A series n-p-n MOSFET structure provides device and signal-source protection in the event of power loss or overvoltages. Under fault conditions the multiplexer input (or output) appears as an open circuit and only a few nanoamperes of leakage current will flow. This protects not only the multiplexer and the circuitry following it, but also protects the sensors or signal sources which drive the multiplexer.

The DG458 and DG459 can withstand continuous overvoltage inputs up to ± 35 V. All digital inputs have TTL compatible logic thresholds. Break-before-make operation prevents channel-to-channel interference.

The DG458 and DG459 are improved pin-compatible replacements for HI-508A/509A and MAX358/359 multiplexers.

FEATURES

- Fault and Overvoltage Protection
- All Channels Off When Power Off
- Latchup-Proof
- Fast Switching - t_A: 200 ns
- Break-Before-Make Switching
- Low On-Resistance: 180 W
- Low Power Consumption: 3 mW
- TTL and CMOS Compatible Inputs

Pb-free Available

RoHS* COMPLIANT

BENEFITS

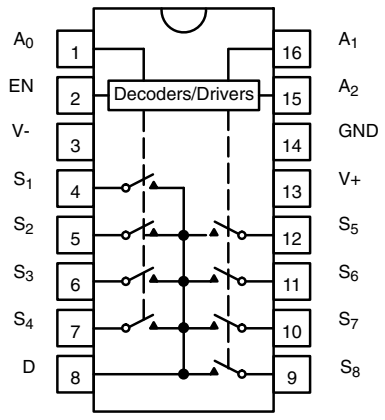
- Improved Ruggedness
- Power Loss Protection
- Prevents Adjacent Channel Crosstalk
- Standard Logic Interface
- Superior Accuracy
- Fast Settling Time

APPLICATIONS

- Data Acquisition Systems
- Industrial Process Control Systems
- Avionics Test Equipment
- High-Rel Control Systems
- Telemetry

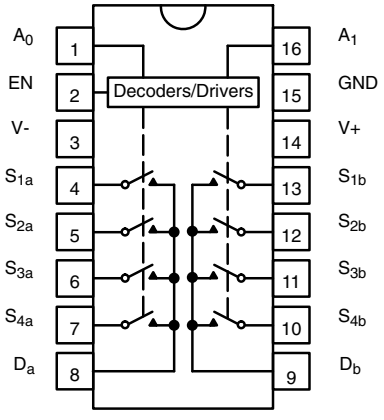
FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

DG458
Dual-In-Line



Top View

DG459
Dual-In-Line



Top View

* Pb containing terminations are not RoHS compliant, exemptions may apply

THRU TABLES AND ORDERING INFORMATION

TRUTH TABLE - DG458

A_2	A_1	A_0	EN	On Switch
X	X	X	0	None
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

TRUTH TABLE - DG459

A_1	A_0	EN	On Switch
X	X	0	None
0	0	1	1
0	1	1	2
1	0	1	3
1	1	1	4

Logic "0" = $V_{AL} \leq 0.8$ V
Logic "1" = $V_{AH} \geq 2.4$ V
X = Don't Care

ORDERING INFORMATION

Temp Range	Package	Part Number
- 40 to 85 °C	16-pin Plastic DIP	DG458DJ DG458DJ-E3
		DG459DJ DG459DJ-E3

ABSOLUTE MAXIMUM RATINGS

Parameter		Limit	Unit
V+ to V-		44	V
V+ to GND		22	
V- to GND		- 25	
V_{EN}, V_A Digital Input		(V-) - 4 to (V+) + 4	
V_S, Analog Input Overvoltage with Power On		(V-) - 20 to (V+) + 20	
V_S, Analog Input Overvoltage with Power Off		- 35 to + 35	
Continuous Current, S or D		20	mA
Peak Current, S or D (Pulsed at 1 ms, 10 % duty cycle max)		40	
Storage Temperature	(AK Suffix)	- 65 to 150	°C
	(DJ Suffix)	- 65 to 125	
Power Dissipation (Package)[a]	16-pin Plastic DIP[B]	600	mW
	16-pin CerDIP[C]	1000	
	LCC-20[d]	1000	

Notes:
a. All leads soldered or welded to PC board.
b. Derate 6.3 mW/°C above 75 °C.
c. Derate 12 mW/°C above 75 °C.
d. Derate 10 mW/°C above 75 °C.

SPECIFICATIONS[a]

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V- = - 15 V V_{AL} = 0.8 V, V_{AH} = 2.4 V[f]		Temp.[b]	Typ.[c]	A Suffix - 55 °C to 125 °C Min.[d]	A Suffix - 55 °C to 125 °C Max.[d]	D Suffix - 40 °C to 85 °C Min.[d]	D Suffix - 40 °C to 85 °C Max.[d]	Unit
Analog Switch										
Analog Signal Range[e]	V_{ANALOG}			Full		- 10	10	- 10	10	V
Drain-Source On-Resistance	$R_{DS(on)}$	V_D = ± 9.5 V, I_S = - 400 µA		Room Full	0.45		1.2 1.5		1.5 1.8	kΩ
		V_D = ± 5 V, I_S = - 400 µA		Room	180		400		400	Ω
$R_{DS(on)}$ Matching Between Channels[h]	$\Delta R_{DS(on)}$	V_D = 0 V, I_S = - 400 µA		Room	6					%
Source Off Leakage Current	$I_{S(off)}$	V_{EN} = 0 V, V_D = ± 10 V V_S = ± 10 V		Room Full	0.03	- 0.5 - 50	0.5 50	- 1 - 20	1 20	nA
Drain Off Leakage Current	$I_{D(off)}$	V_{EN} = 0 V V_D = ± 10 V V_S = ± 10 V	DG458	Room Full	0.1	- 1 - 200	1 200	- 1 - 50	1 50	
			DG459	Room Full	0.1	- 1 - 100	1 100	- 2 - 25	2 25	
Differential Off Drain Leakage Current	I_{DIFF}	DG459 Only		Room		- 50	50	- 20	20	
Drain On Leakage Current	$I_{D(on)}$	V_S = V_D = ± 10 V	DG458	Room Full	0.1	- 2 - 200	2 200	- 5 - 50	5 50	
			DG459	Room Full	0.05	- 2 - 100	2 100	- 5 - 25	5 25	
Fault										
Output Leakage Current (with Overvoltage)	$I_{D(off)}$	V_S = ± 33 V, V_D = 0 V See Figure 1		Room	0.02					nA
Input Leakage Current (with Overvoltage)	$I_{S(off)}$	V_S = ± 25 V, V_D = 10 V, See Figure 1		Room	0.005	- 5	5	- 10	10	µA
Input Leakage Current (with Power Supplies Off)		V_S = ± 25 V, V_{SUPS} = 0 V V_D = A_0, A_1, A_2, EN = 0 V		Room	0.001	- 2	2	- 5	5	
Digital Control										
Input Low Threshold	V_{AI}			Full			0.8		0.8	V
Input Low Threshold	V_{AL}			Full		2.4		2.4		
Logic Input Control	I_A	V_A = 2.4 V or 0.8 V		Full		- 1	1	- 1	1	µA

SPECIFICATIONS[a]

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V- = - 15 V V_{AL} = 0.8 V, V_{AH} = 2.4 V[f]		Temp.[b]	Typ.[c]	A Suffix - 55 °C to 125 °C Min.[d]	A Suffix - 55 °C to 125 °C Max.[d]	D Suffix - 40 °C to 85 °C Min.[d]	D Suffix - 40 °C to 85 °C Max.[d]	Unit
Dynamic Characteristics										
Transition Time	t_A	See Figure 3		Room	200		500		500	ns
Break-Before-Make Interval	t_{OPEN}	See Figure 4		Room	45	10		10		ns
Enable Turn-On Time	$t_{ON(EN)}$	See Figure 5		Room Full	140		250 500		250 500	ns
Enable Turn-Off Time	$t_{OFF(EN)}$	See Figure 5		Room Full	50		250 500		250 500	ns
Settling Time	t_s	To 0.1 %		Room	0.5					µs
		To 0.01 %		Room	1.5					µs
Off Isolation	OIRR	V_{EN} = 0 V, R_L = 1 kΩ C_L = 15 pF, V_S = 3 V_{RMS} f = 100 kHz		Room	90					dB
Logic Input Capacitance	C_{in}	f = 1 MHz		Room	5					pF
Source Off Capacitance	$C_{S(off)}$			Room	5					pF
Drain Off Capacitance	$C_{D(off)}$		DG458	Room	15					pF
			DG459	Room	10					pF
Drain On Capacitance	$C_{D(on)}$		DG458	Room	40					pF
			DG459	Room	35					pF
Power Supplies										
Positive Supply Current	I+	V_{EN} = 5 or 0 V, V_A = 0 V		Room Full	0.05		0.1 0.2		0.1 0.2	mA
Negative Supply Current	I-	V_{EN} = 5 or 0 V, V_A = 0 V		Room Full	- 0.01	- 0.1 - 0.2		- 0.1 - 0.2		mA
Power Supply Range for Continuous Operation				Room		± 4.5	± 18	± 4.5	± 18	V

Notes:

a. Refer to PROCESS OPTION FLOWCHART.

b. Room = 25 °C, Full = as determined by the operating temperature suffix.

c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.

e. Guaranteed by design, not subject to production test.

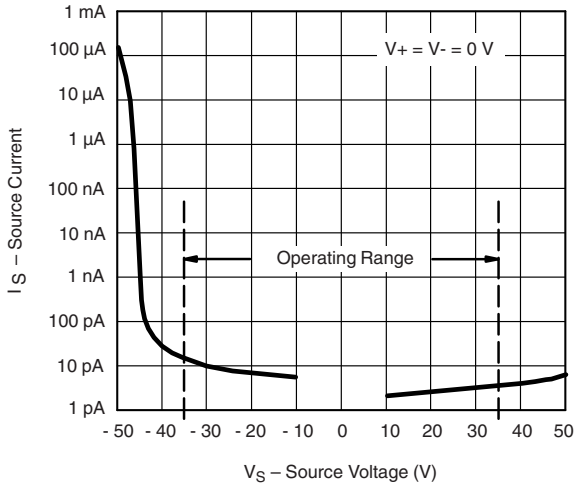
f. V_{IN} = input voltage to perform proper function.

g. When the analog signal exceeds the + 13.5 V or - 12 V, $R_{DS(on)}$ starts to rise until only leakage currents flow.

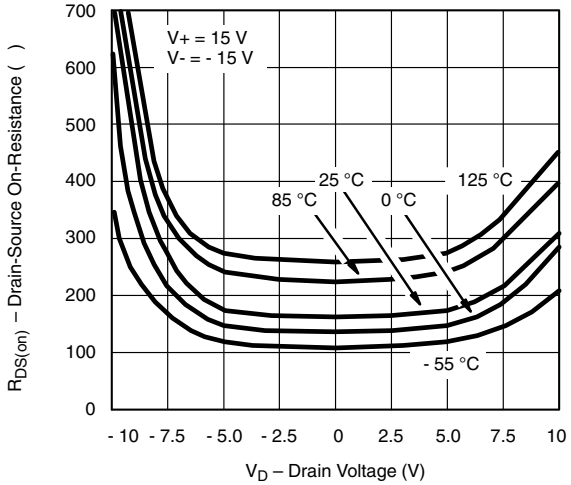
h. $\Delta R_{DS(on)} = \left(\frac{R_{DS(on)}\ MAX - R_{DS(on)}\ MIN}{Rr_{DS(on)}\ AVE} \right) x\ 100\ \%$

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

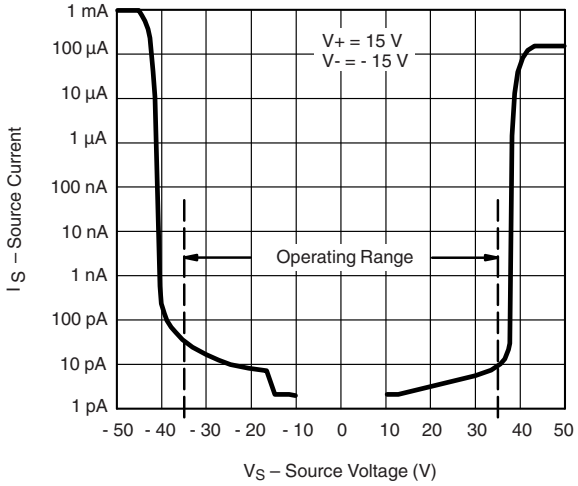
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



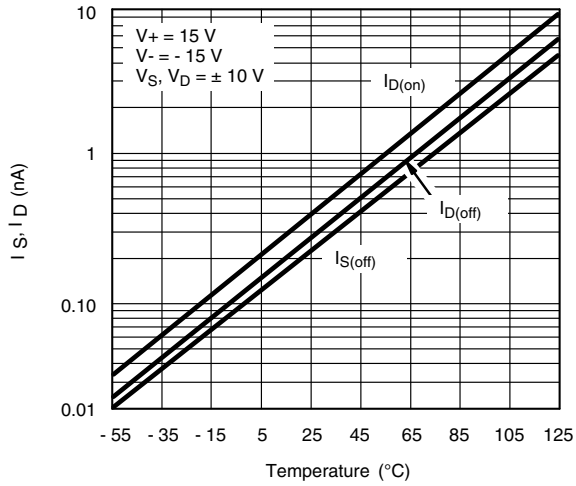
Input Leakage vs. Input Voltage



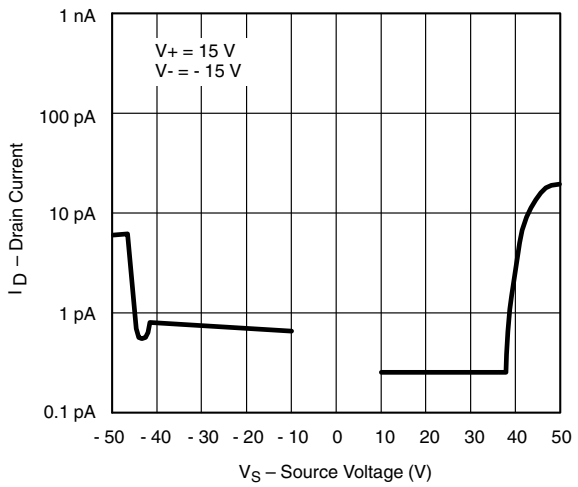
$R_{DS(on)}$ vs. V_D and Temperature



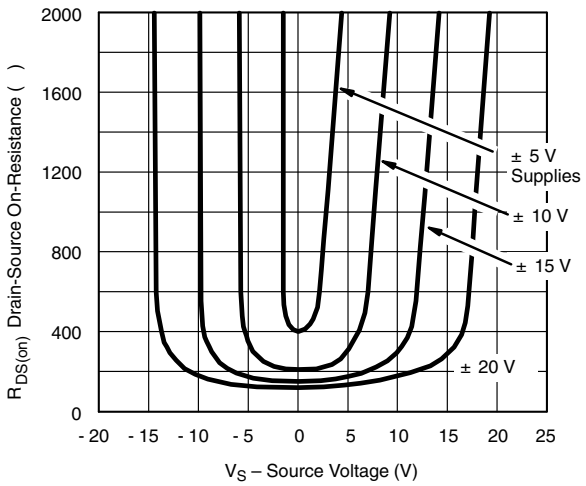
Off-Channel Leakage Currents vs. Input Voltage



Leakage Currents vs. Temperature

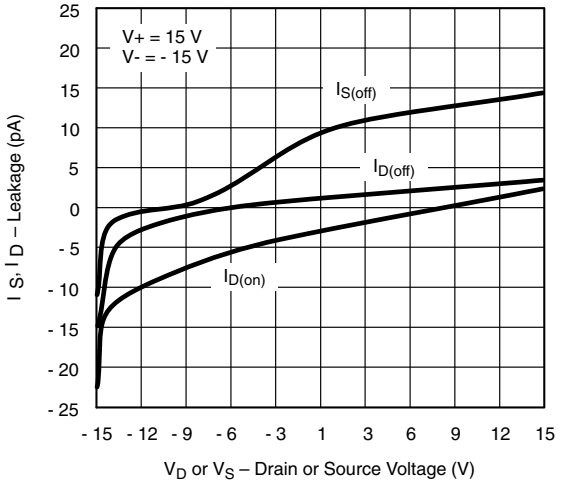


Output Leakage vs. Off-Channel Overvoltage

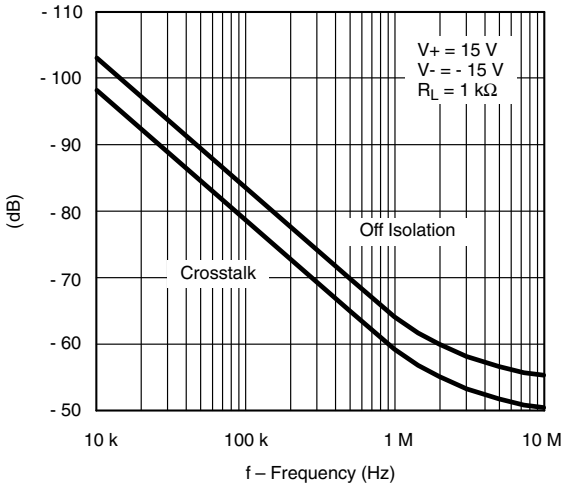


$R_{DS(on)}$ vs. Input Voltage

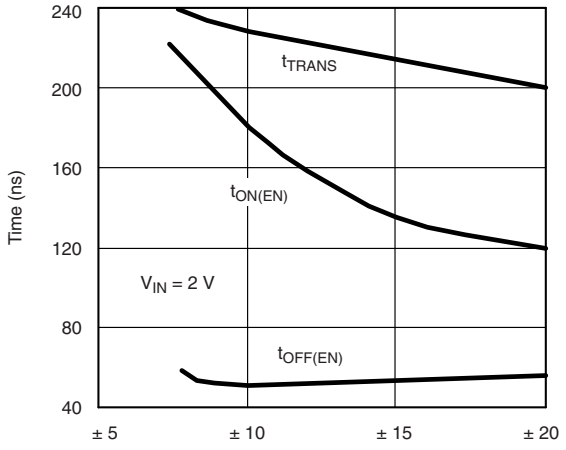
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



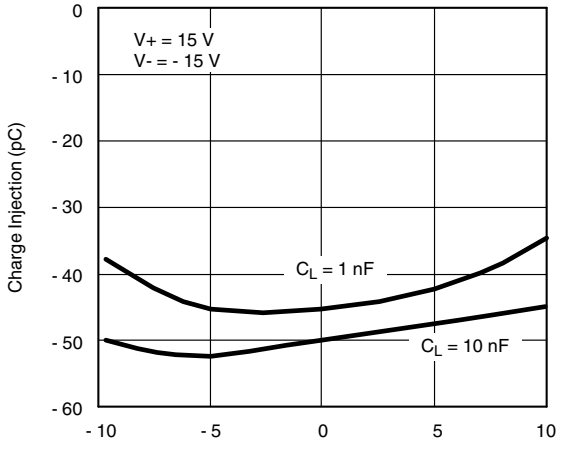
Leakage Current vs. V_S, V_D



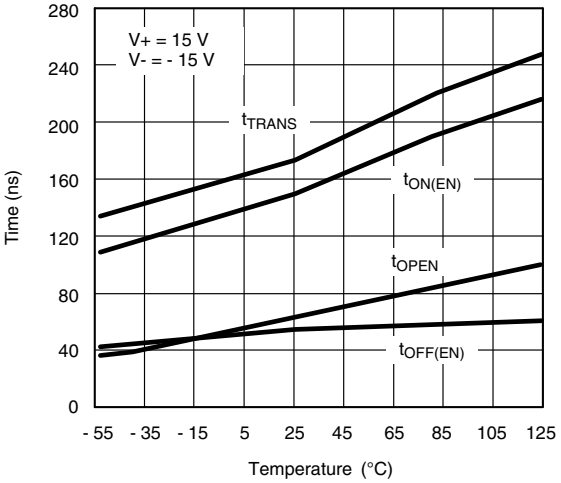
Off Isolation and X_{TALK} vs. Frequency



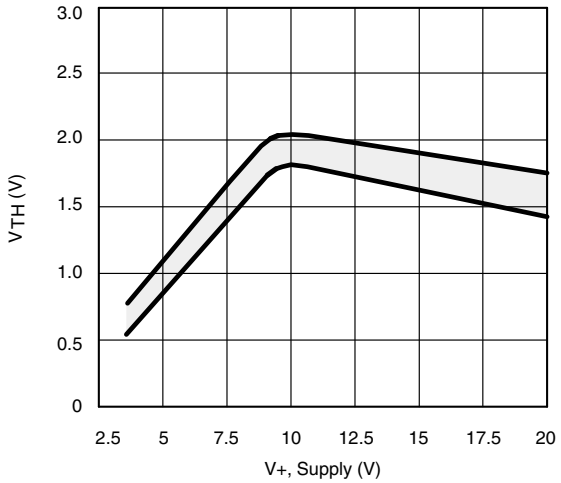
Switching Times (t_{TRANS}, t_{ON}, t_{OFF}) vs. ± $V_{SUPPLIES}$



Q_{INJ} vs. V_S

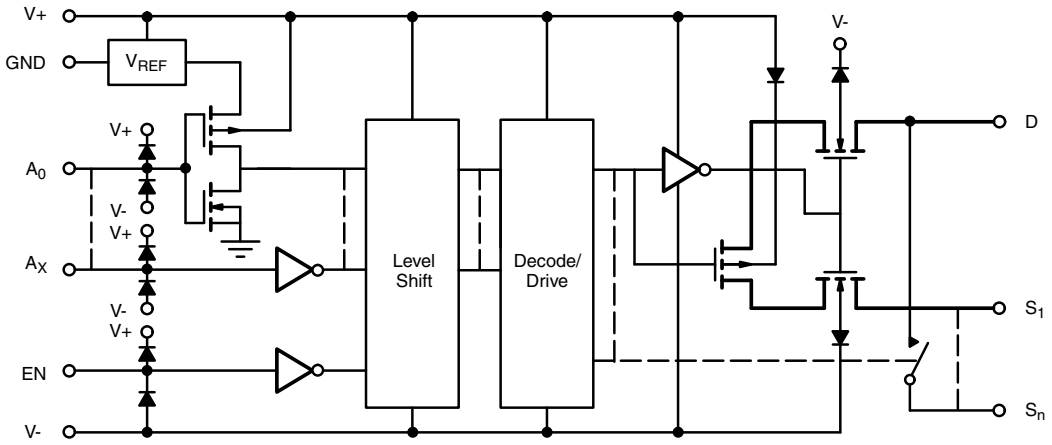


Switching Times vs. Temperature



Logic Input Switching Threshold vs. ± $V_{SUPPLIES}$

SCHEMATIC DIAGRAM (TYPICAL CHANNEL)



TEST CIRCUITS

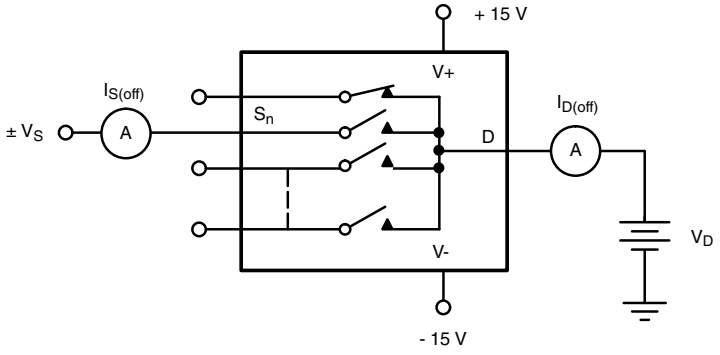
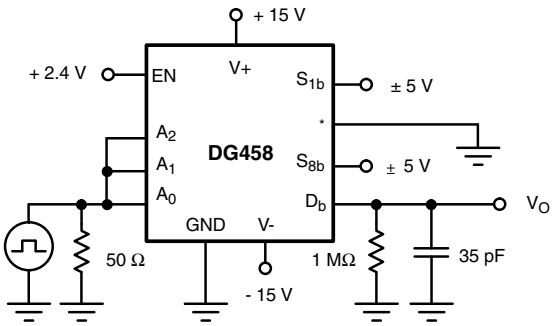


Figure 2. Analog Input Overvoltage



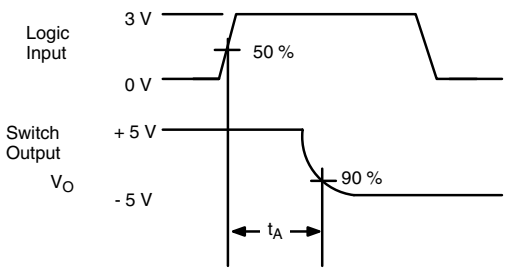


Figure 3. Transition Time

TEST CIRCUITS

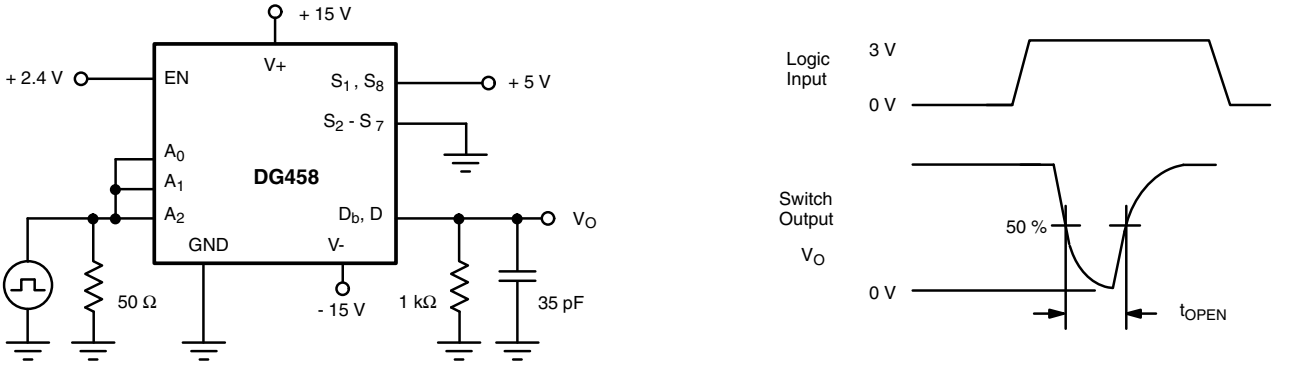


Figure 4. Break-Before-Make Time

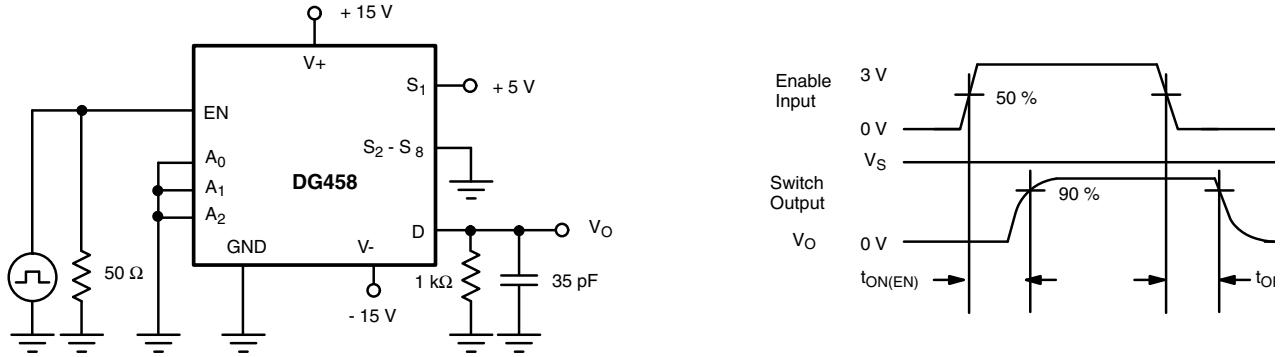


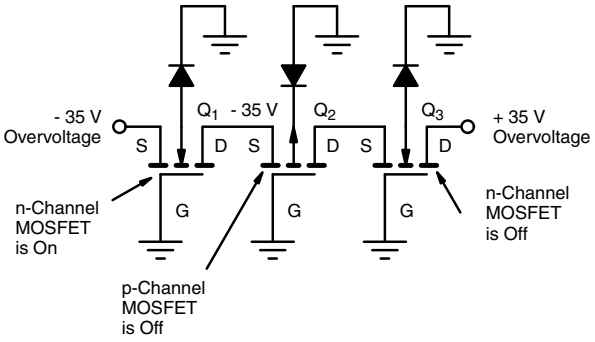
Figure 5. Enable Delay

DETAILED DESCRIPTION

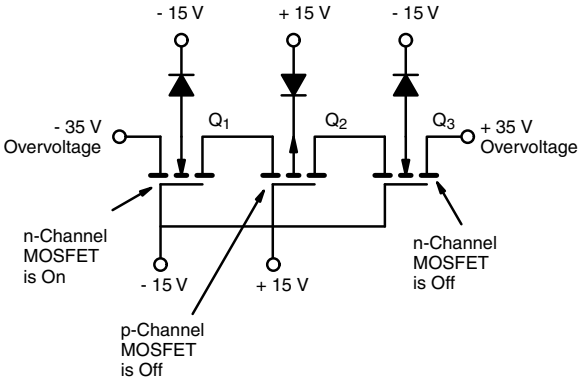
The Vishay Siliconix DG458 and DG459 multiplexers are fully fault- and overvoltage-protected for continuous input voltages up to ± 35 V whether or not voltage is applied to the power supply pins (V+, V-). These multiplexers are built on a high-voltage junction-isolated silicon-gate CMOS process. Two n-channel and one p-channel MOSFETs are connected in series to form each channel (Figure 1).

Within the normal analog signal range (± 10 V), the $R_{DS(on)}$ variation as a function of analog signal voltage is comparable to that of the classic parallel N-MOS and P-MOS switches.

When the analog signal approaches or exceeds either supply rail, even for an on-channel, one of the three series MOSFETs gets cut-off, providing inherent protection against overvoltages even if the multiplexer power supply voltages are lost. This protection is good up to the breakdown voltage of the respective series MOSFETs. Under fault conditions only sub microamp leakage currents can flow in or out of the multiplexer. This not only provides protection for the multiplexer and succeeding circuitry, but it allows normal, undisturbed operation of all other channels. Additionally, in case of power loss to the multiplexer, the loading caused on the transducers and signal sources is insignificant, therefore redundant multiplexers can be used on critical applications such as telemetry and avionics.



(a) Overvoltage with Multiplexer Power Off



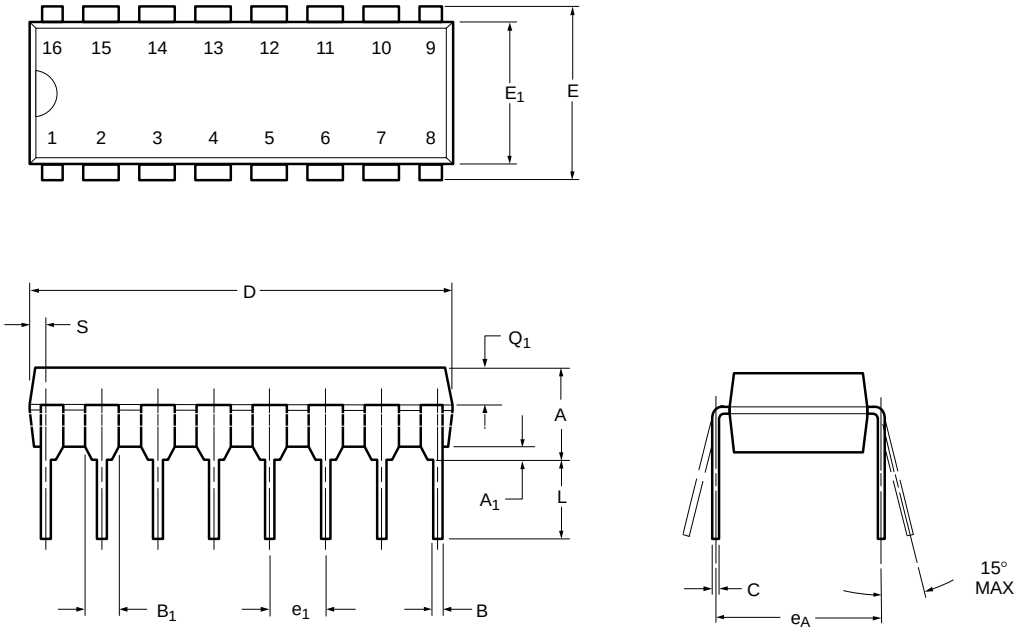
(b) Overvoltage with Multiplexer Power On

Figure 5. Overvoltage Protection

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see http://www.vishay.com/ppg?70064.

Package Information
Vishay Siliconix

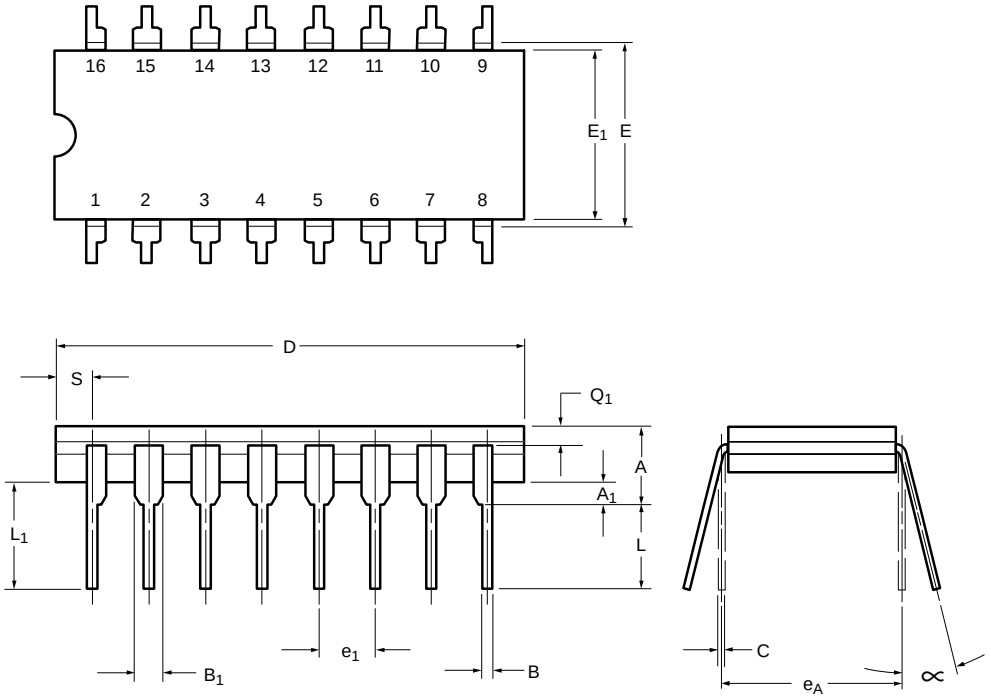
PDIP: 16-LEAD



Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	3.81	5.08	0.150	0.200
A_1	0.38	1.27	0.015	0.050
B	0.38	0.51	0.015	0.020
B_1	0.89	1.65	0.035	0.065
C	0.20	0.30	0.008	0.012
D	18.93	21.33	0.745	0.840
E	7.62	8.26	0.300	0.325
E_1	5.59	7.11	0.220	0.280
e_1	2.29	2.79	0.090	0.110
e_A	7.37	7.87	0.290	0.310
L	2.79	3.81	0.110	0.150
Q_1	1.27	2.03	0.050	0.080
S	0.38	1.52	.015	0.060
ECN: S-03946—Rev. D, 09-Jul-01 DWG: 5482				

Package Information
Vishay Siliconix

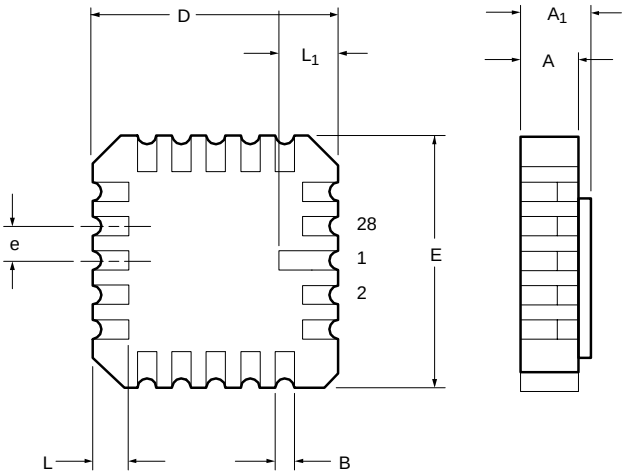
CERDIP: 16-LEAD



Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	4.06	5.08	0.160	0.200
A_1	0.51	1.14	0.020	0.045
B	0.38	0.51	0.015	0.020
B_1	1.14	1.65	0.045	0.065
C	0.20	0.30	0.008	0.012
D	19.05	19.56	0.750	0.770
E	7.62	8.26	0.300	0.325
E_1	6.60	7.62	0.260	0.300
e_1	2.54 BSC		0.100 BSC	
e_A	7.62 BSC		0.300 BSC	
L	3.18	3.81	0.125	0.150
L_1	3.81	5.08	0.150	0.200
Q_1	1.27	2.16	0.050	0.085
S	0.38	1.14	0.015	0.045
∝	0°	15°	0°	15°

ECN: S-03946—Rev. G, 09-Jul-01
DWG: 5403

20-LEAD LCC



Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.37	2.24	0.054	0.088
A_1	1.63	2.54	0.064	0.100
B	0.56	0.71	0.022	0.028
D	8.69	9.09	0.342	0.358
E	8.69	9.09	0.442	0.358
e	1.27 BSC		0.050 BSC	
L	1.14	1.40	0.045	0.055
L_1	1.96	2.36	0.077	0.093

ECN: S-03946—Rev. B, 09-Jul-01
DWG: 5321

Disclaimer

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