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[SI4162DY-T1-GE3](#)

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Si4162DY
Vishay Siliconix

N-Channel 30-V (D-S) MOSFET

PRODUCT SUMMARY			
V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A)	Q _g (Typ.)
30	0.0079 at V _{GS} = 10 V	19.3 ^a	8.8 nC
	0.010 at V _{GS} = 4.5 V	17.1 ^a	

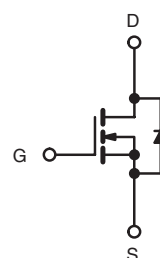
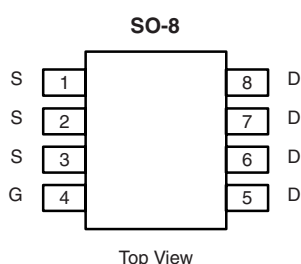
FEATURES

- Halogen-free
- TrenchFET® Power MOSFET
- 100 % R_g Tested
- 100 % UIS Tested



APPLICATIONS

- DC/DC
 - High Side
 - VRM
 - POL
 - Server



Ordering Information: Si4162DY-T1-GE3 (Lead (Pb)-free and Halogen-free)

N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS T _A = 25 °C, unless otherwise noted				
Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V _{DS}	30	V
Gate-Source Voltage		V _{GS}	± 20	
Continuous Drain Current (T _J = 150 °C)	T _C = 25 °C	I _D	19.3 ^a	A
	T _C = 70 °C		15.4	
	T _A = 25 °C		13.6 ^{b, c}	
	T _A = 70 °C		10.9 ^{b, c}	
Pulsed Drain Current		I _{DM}	70	mJ
Avalanche Current		I _{AS}	31	
Avalanche Energy		E _{AS}	48	
Continuous Source-Drain Diode Current	T _C = 25 °C	I _S	4.2 ^a	A
	T _A = 25 °C		2.1 ^{b, c}	
Maximum Power Dissipation	T _C = 25 °C	P _D	5	W
	T _C = 70 °C		3.2	
	T _A = 25 °C		2.5 ^{b, c}	
	T _A = 70 °C		1.6 ^{b, c}	
Operating Junction and Storage Temperature Range		T _J , T _{stg}	- 55 to 150	°C
Soldering Recommendations (Peak Temperature)			260	

THERMAL RESISTANCE RATINGS				
Parameter		Symbol	Typical	Maximum
Maximum Junction-to-Ambient ^{b, d}	t ≤ 10 s	R _{thJA}	38	50
Maximum Junction-to-Case (Drain)	Steady State	R _{thJC}	20	25

Notes:

- Based on T_C = 25 °C.
- Surface Mounted on 1" x 1" FR4 board.
- t = 10 s.
- Maximum under Steady State conditions is 85 °C/W.

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SPECIFICATIONS T _J = 25 °C, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA	30			V
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	I _D = 250 μA		32		mV/°C
V _{GS(th)} Temperature Coefficient	ΔV _{GS(th)} /T _J			- 5.5		
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	1		3	V
Gate-Source Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 30 V, V _{GS} = 0 V			1	μA
		V _{DS} = 30 V, V _{GS} = 0 V, T _J = 55 °C			5	
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 10 V	50			A
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = 10 V, I _D = 20 A		0.0065	0.0079	Ω
		V _{GS} = 4.5 V, I _D = 14 A		0.0082	0.010	
Forward Transconductance ^a	g _{fs}	V _{DS} = 15 V, I _D = 20 A		70		S
Dynamic ^b						
Input Capacitance	C _{iss}	V _{DS} = 15 V, V _{GS} = 0 V, f = 1 MHz		1155		pF
Output Capacitance	C _{oss}			260		
Reverse Transfer Capacitance	C _{rss}			95		
Total Gate Charge	Q _g	V _{DS} = 15 V, V _{GS} = 10 V, I _D = 20 A		20	30	nC
		V _{DS} = 15 V, V _{GS} = 4.5 V, I _D = 20 A		8.8	14	
Gate-Source Charge	Q _{gs}			3.5		
Gate-Drain Charge	Q _{gd}			2.2		
Gate Resistance	R _g	f = 1 MHz		1.0	2.0	Ω
Turn-On Delay Time	t _{d(on)}	V _{DD} = 15 V, R _L = 15 Ω I _D ≅ 1.0 A, V _{GEN} = 4.5 V, R _g = 17 Ω		20	30	ns
Rise Time	t _r			15	25	
Turn-Off Delay Time	t _{d(off)}			25	40	
Fall Time	t _f			10	15	
Turn-On Delay Time	t _{d(on)}	V _{DD} = 15 V, R _L = 15 Ω I _D ≅ 1.0 A, V _{GEN} = 10 V, R _g = 1 Ω		14	20	
Rise Time	t _r			9	15	
Turn-Off Delay Time	t _{d(off)}			25	40	
Fall Time	t _f			9	15	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C			30	A
Pulse Diode Forward Current	I _{SM}				70	
Body Diode Voltage	V _{SD}	I _S = 4.0 A, V _{GS} = 0 V		0.8	1.2	V
Body Diode Reverse Recovery Time	t _{rr}	I _F = 4.0 A, dI/dt = 100 A/μs, T _J = 25 °C		21	42	ns
Body Diode Reverse Recovery Charge	Q _{rr}			15	30	nC
Reverse Recovery Fall Time	t _a			12.6		ns
Reverse Recovery Rise Time	t _b			8.4		

Notes:

a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

b. Guaranteed by design, not subject to production testing.

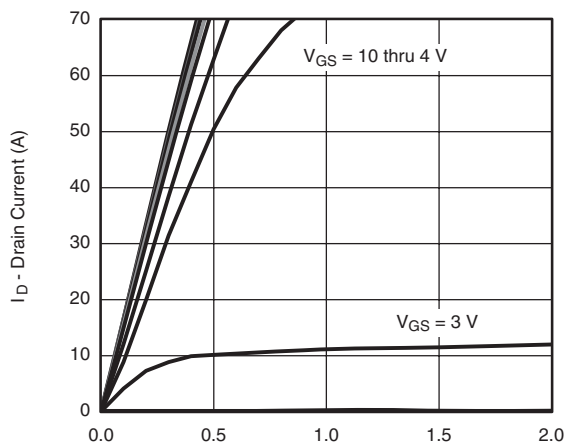
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



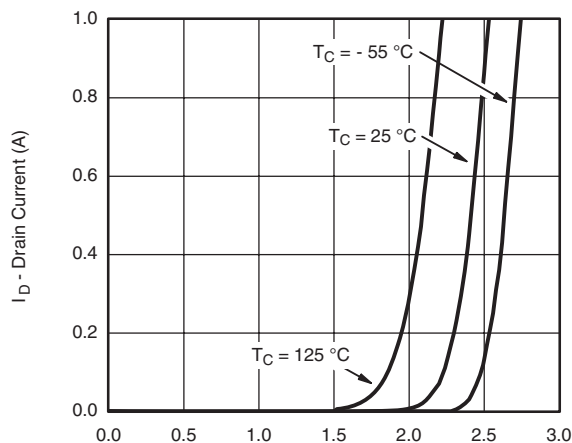
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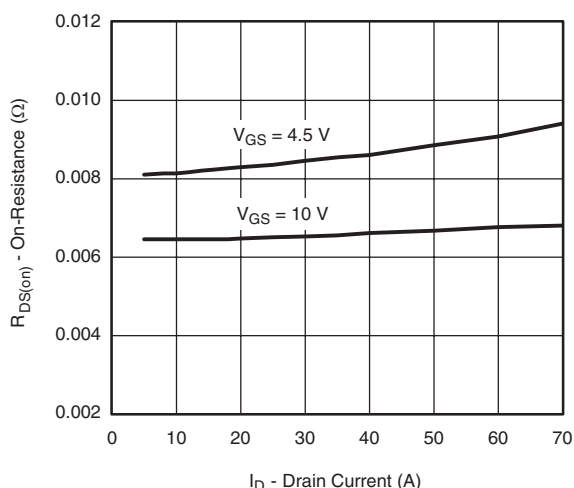
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



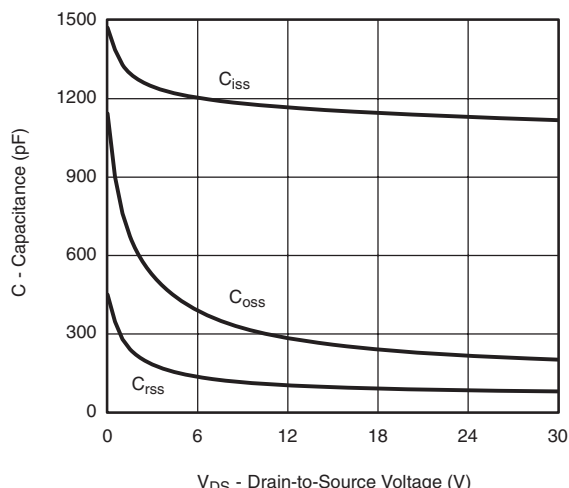
Output Characteristics



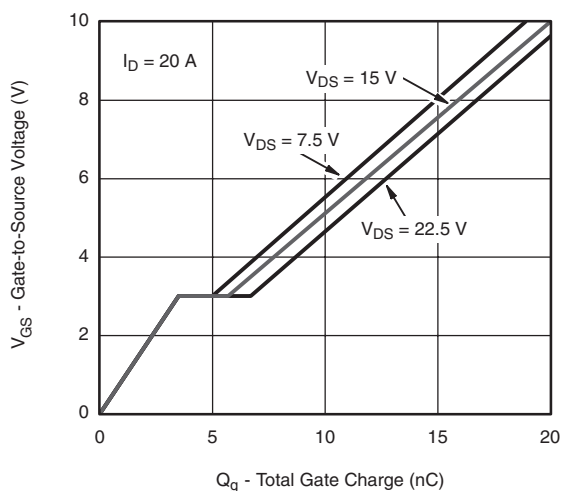
Transfer Characteristics



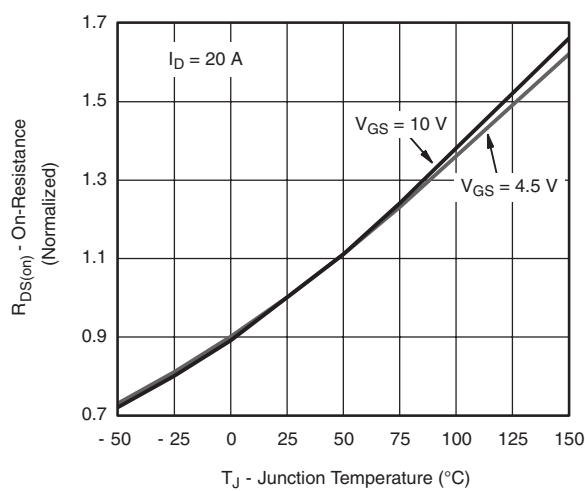
On-Resistance vs. Drain Current and Gate Voltage



Capacitance



Gate Charge



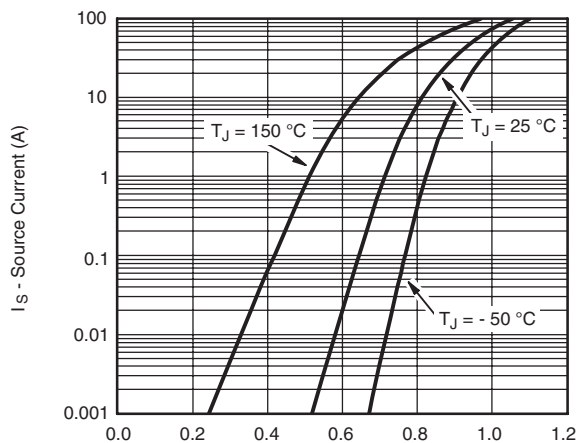
On-Resistance vs. Junction Temperature

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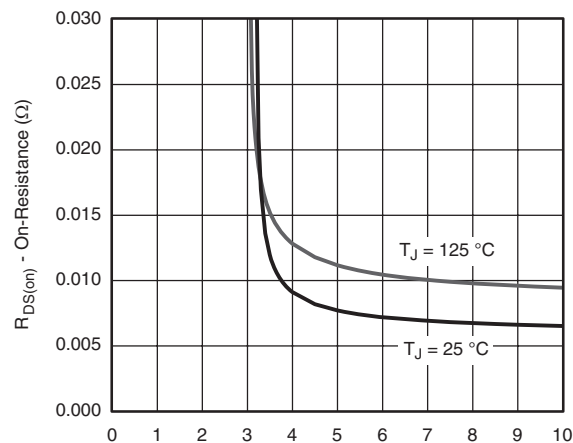
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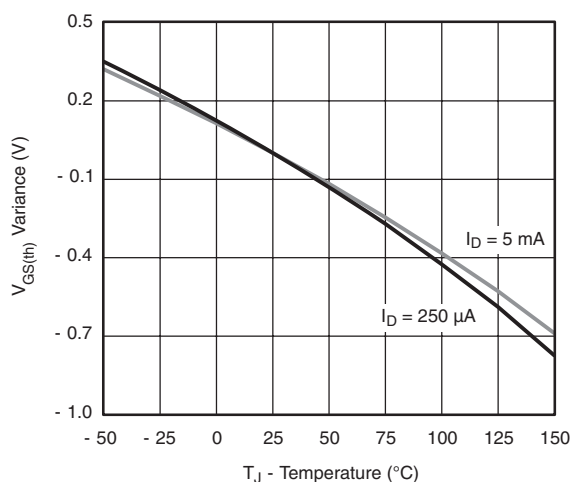
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



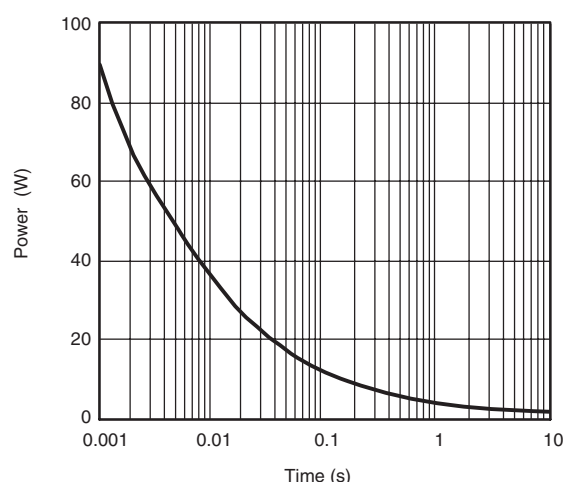
V_{SD} - Source-to-Drain Voltage (V)
Source-Drain Diode Forward Voltage



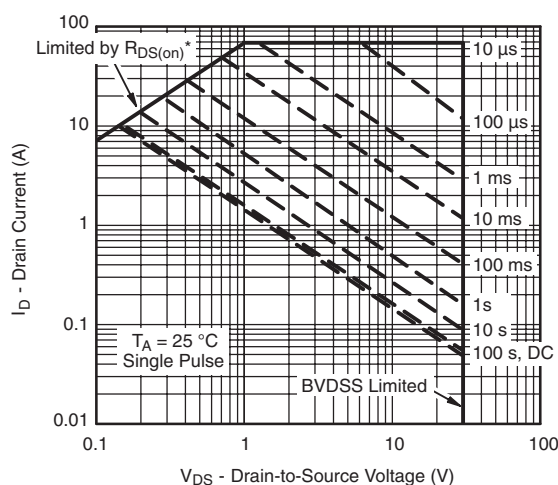
V_{GS} - Gate-to-Source Voltage (V)
On-Resistance vs. Gate-to-Source Voltage



T_J - Temperature ($^\circ\text{C}$)
Threshold Voltage



Single Pulse Power (Junction-to-Ambient)



* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

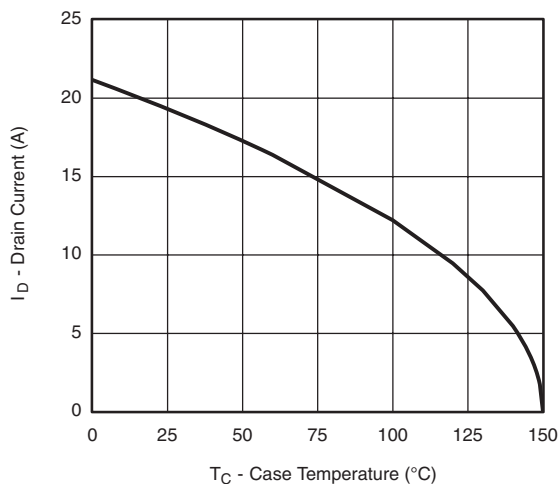
Safe Operating Area, Junction-to-Ambient



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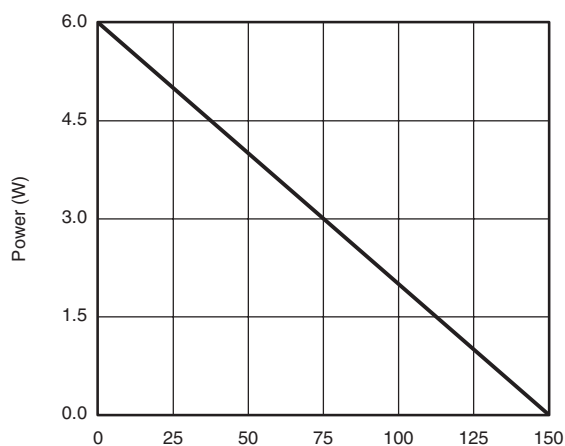
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TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



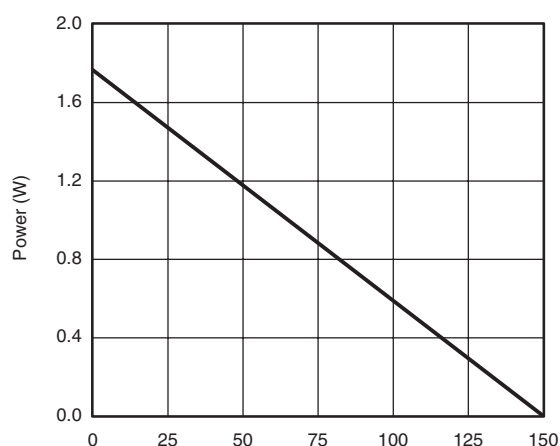
T_C - Case Temperature (°C)

Current Derating*



T_C - Case Temperature (°C)

Power, Junction-to-Case



T_A - Ambient Temperature (°C)

Power, Junction-to-Ambient

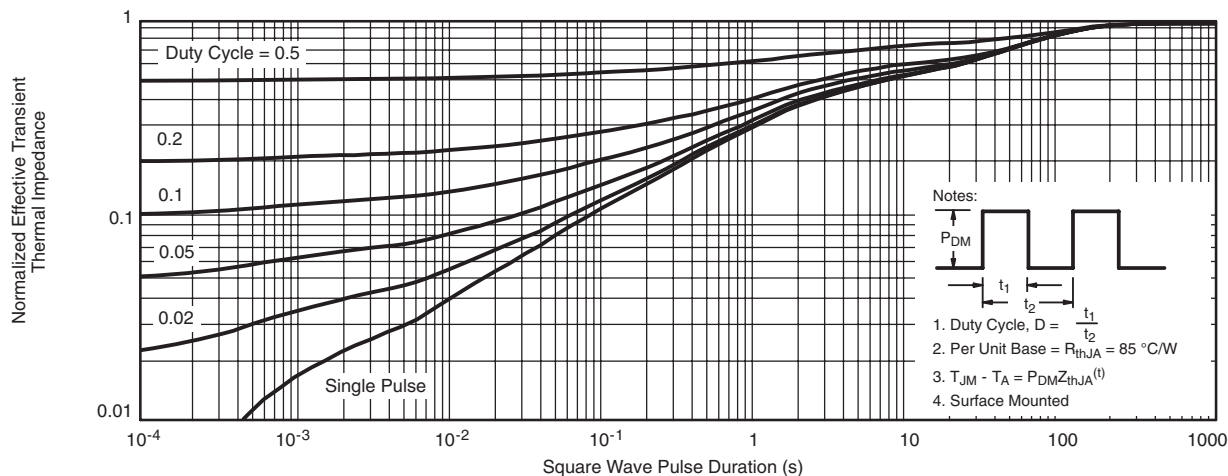
* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

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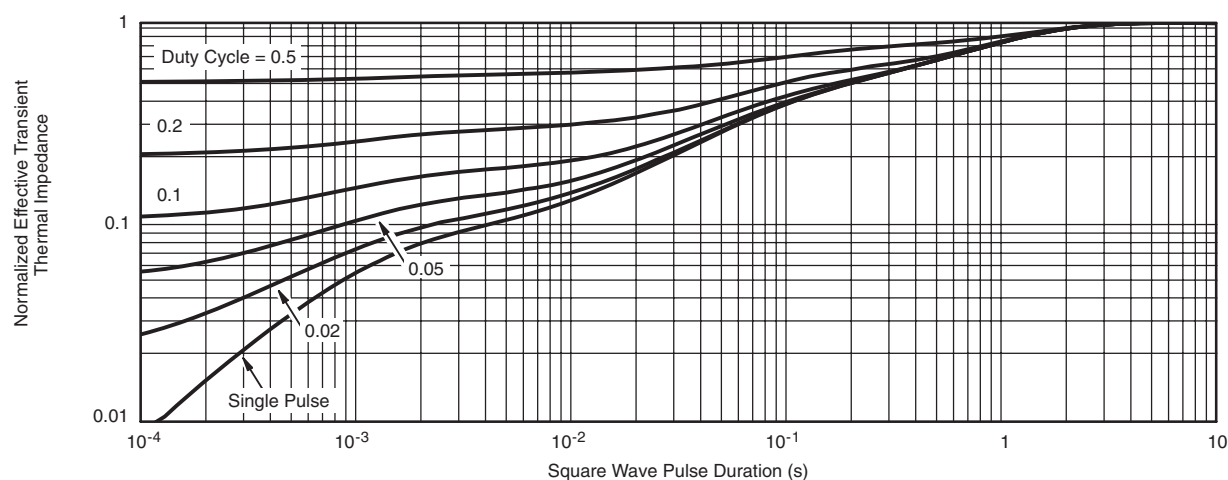
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TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Foot

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <http://www.vishay.com/ppg?68967>.

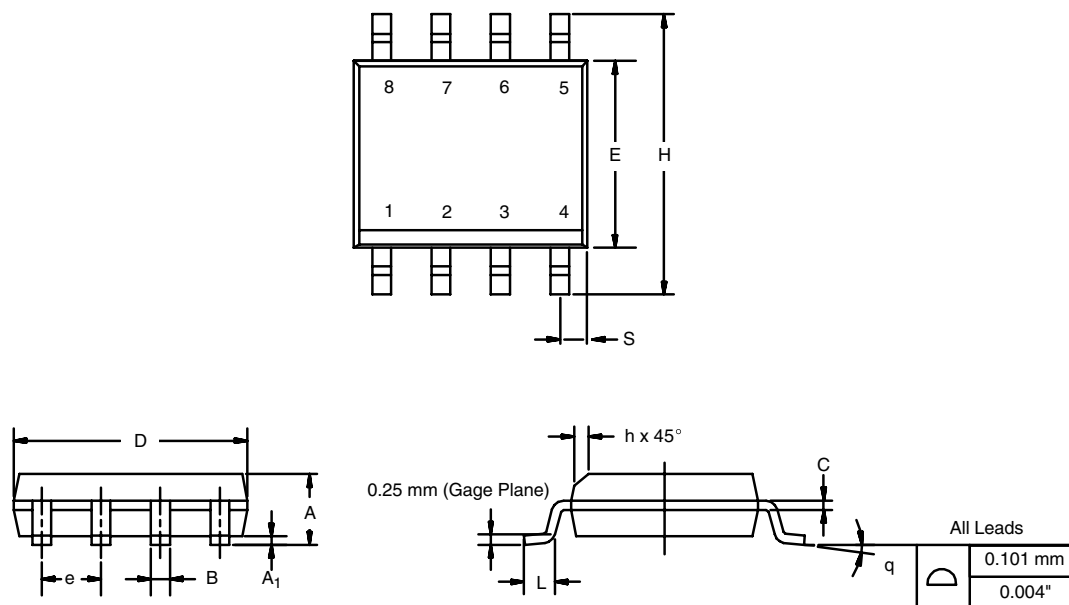


Package Information

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SOIC (NARROW): 8-LEAD

JEDEC Part Number: MS-012



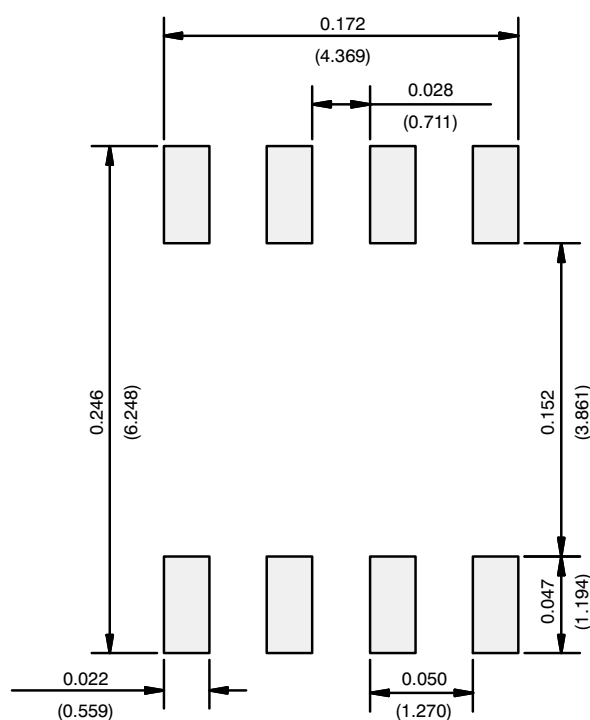
DIM	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A ₁	0.10	0.20	0.004	0.008
B	0.35	0.51	0.014	0.020
C	0.19	0.25	0.0075	0.010
D	4.80	5.00	0.189	0.196
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.020
L	0.50	0.93	0.020	0.037
q	0°	8°	0°	8°
S	0.44	0.64	0.018	0.026
ECN: C-06527-Rev. I, 11-Sep-06				
DWG: 5498				

Application Note 826

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RECOMMENDED MINIMUM PADS FOR SO-8



Recommended Minimum Pads
Dimensions in Inches/(mm)

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