

Excellent Integrated System Limited

Stocking Distributor

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Vishay/Siliconix SI4438DY-T1-E3

For any questions, you can email us directly: sales@integrated-circuit.com





Vishay Siliconix

N-Channel 30-V (D-S) MOSFET

PRODUCT SUMMARY					
V _{DS} (V)	$R_{DS(on)}(\Omega)$	I _D (A) ^a	Q _g (Typ.)		
30	0.0027 at V _{GS} = 10 V	36	41 nC		
	0.004 at V _{GS} = 4.5 V	29	41110		

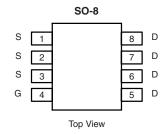
FEATURES

- Halogen-free According to IEC 61249-2-21 **Available**
- TrenchFET® Power MOSFET
- 100 % R_g Tested

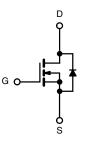


APPLICATIONS

• DC-to-DC and AC-to-DC Oring Diode Applications



Ordering Information: Si4438DY-T1-E3 (Lead (Pb)-free) Si4438DY-T1-GE3 (Lead (Pb)-free and Halogen-free)



N-Channel MOSFET

Parameter		Symbol	Limit	Unit	
Drain-Source Voltage	V _{DS}	30	.,		
Gate-Source Voltage		V _{GS}	± 20	V	
	T _C = 25 °C		36		
Ocation and Ducin Orange (T. 450.00)	T _C = 70 °C		29		
Continuous Drain Current (T _J = 150 °C)	T _A = 25 °C	I _D	24 ^{b, c}		
	T _A = 70 °C		19 ^{b, c}	А	
Pulsed Drain Current		I _{DM}	70		
Outline Outline Daily Birds Outline	T _C = 25 °C		7.0		
Continuous Source-Drain Diode Current	T _A = 25 °C	I _S	3.0 ^{b, c}		
Maximum Power Dissipation	T _C = 25 °C		7.8		
	T _C = 70 °C		5.0		
	T _A = 25 °C	P _D	3.5 ^{b, c}	W	
	T _A = 70 °C		2.2 ^{b, c}		
Operating Junction and Storage Temperature Ra	T _J , T _{stq}	- 55 to 150	°C		

THERMAL RESISTANCE RATINGS						
Parameter		Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient ^{b, d}	t ≤ 10 s	R _{thJA}	29	35	°C/W	
Maximum Junction-to-Foot (Drain)	Steady State	R _{thJF}	13	16		

Notes:

- a. Based on T_C = 25 °C.
- b. Surface Mounted on 1" x 1" FR4 board.
- d. Maximum under Steady State conditions is 80 °C/W.

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Datasheet of SI4438DY-T1-E3 - MOSFET N-CH 30V 36A 8-SOIC

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Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static	_						
Drain-Source Breakdown Voltage	V _{DS}	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	30			V	
V _{DS} Temperature Coefficient	$\Delta V_{DS}/T_{J}$	L 050A		31		mV/°C	
V _{GS(th)} Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	I _D = 250 μA		- 6.7			
Gate-Source Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	1.4		2.6	٧	
Gate-Source Leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			± 100	nA	
Zero Gate Voltage Drain Current	I _{DSS}	$V_{DS} = 30 \text{ V}, V_{GS} = 0 \text{ V}$			1		
		$V_{DS} = 30 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 55 ^{\circ}\text{C}$			10	μΑ	
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \ge 5 \text{ V}, V_{GS} = 10 \text{ V}$	30			Α	
Drain-Source On-State Resistance ^a	5	$V_{GS} = 10 \text{ V}, I_D = 20 \text{ A}$		0.0022	0.0027		
	R _{DS(on)}	$V_{GS} = 4.5 \text{ V}, I_D = 15 \text{ A}$		0.0033	0.004	Ω	
Forward Transconductance ^a	9 _{fs}	$V_{DS} = 15 \text{ V}, I_D = 20 \text{ A}$		86		S	
Dynamic ^b							
Input Capacitance	C _{iss}			4645		pF	
Output Capacitance	C _{oss}	$V_{DS} = 15 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$		900			
Reverse Transfer Capacitance	C _{rss}			555			
Total Gate Charge	Qg	V _{DS} = 15 V, V _{GS} = 10 V, I _D = 20 A		84	126	nC	
		20 00 2		41	62		
Gate-Source Charge	Q _{gs}	$V_{DS} = 15 \text{ V}, V_{GS} = 4.5 \text{ V}, I_D = 20 \text{ A}$		14.6			
Gate-Drain Charge	Q _{gd}			16.5			
Gate Resistance	R _g	f = 1 MHz		1.3	2	Ω	
Turn-On Delay Time	t _{d(on)}			36	55	ns	
Rise Time	t _r	V_{DD} = 15 V, R_L = 1.5 Ω		210	320		
Turn-Off Delay Time	t _{d(off)}	$I_D\cong$ 10 A, V_{GEN} = 4.5 V, R_g = 1 Ω		39	60		
Fall Time	t _f			18	30		
Turn-On Delay Time	t _{d(on)}			17	26		
Rise Time	t _r	V_{DD} = 15 V, R_L = 1.5 Ω		86	130		
Turn-Off Delay Time	t _{d(off)}	$I_D\cong 10$ A, V_{GEN} = 10 V, R_g = 1 Ω		47	75		
Fall Time	t _f			10	16		
Drain-Source Body Diode Characteristic	cs						
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C			7	Λ.	
Pulse Diode Forward Current ^a	I _{SM}				70	Α	
Body Diode Voltage	V _{SD}	I _S = 3 A		0.73	1.1	V	
Body Diode Reverse Recovery Time	t _{rr}			43	65	ns	
Body Diode Reverse Recovery Charge	Q _{rr}			45	70	nC	
Reverse Recovery Fall Time	t _a	$I_F = 20 \text{ A}, \text{ dI/dt} = 100 \text{ A/}\mu\text{s}, T_J = 25 ^{\circ}\text{C}$		22		T	
Reverse Recovery Rise Time	t _b			21		ns	

- a. Pulse test; pulse width $\leq 300~\mu s,$ duty cycle $\leq 2~\%.$
- b. Guaranteed by design, not subject to production testing.

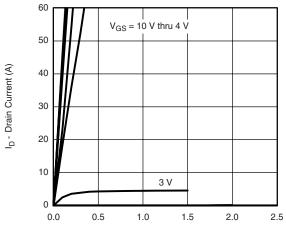
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



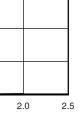


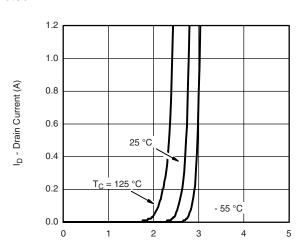
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TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



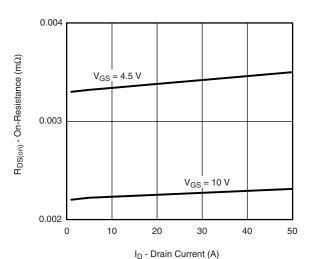
V_{DS} - Drain-to-Source Voltage (V)



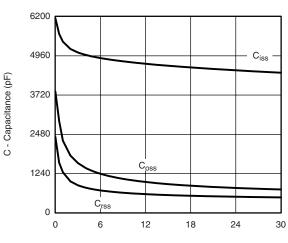


V_{GS} - Gate-to-Source Voltage (V) **Transfer Characteristics**



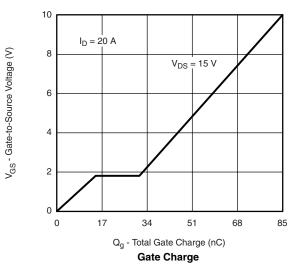


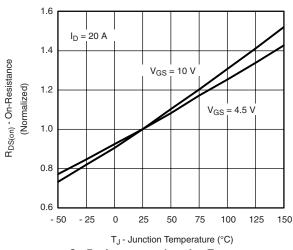
On-Resistance vs. Drain Current and Gate Voltage



V_{DS} - Drain-to-Source Voltage (V)

Capacitance





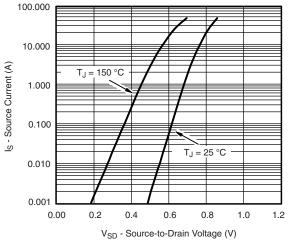
On-Resistance vs. Junction Temperature

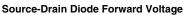
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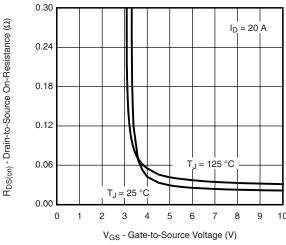


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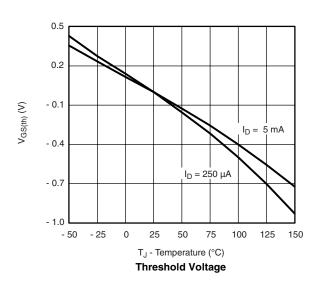
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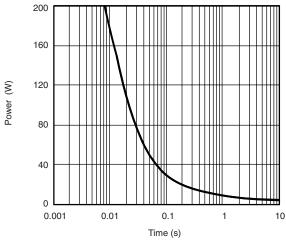




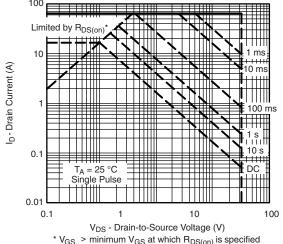


On-Resistance vs. Gate-to-Source Voltage





Single Pulse Power, Junction-to-Ambient



* V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

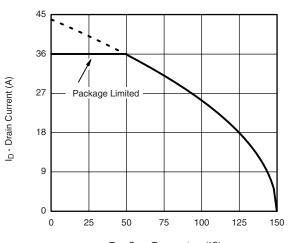
Safe Operating Area, Junction-to-Ambient





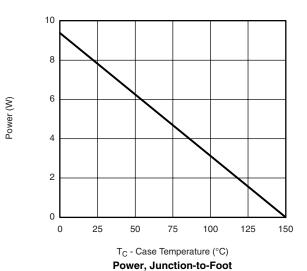
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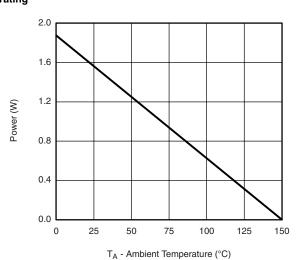
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T_C - Case Temperature (°C)

Current Derating*





Power, Junction-to-Ambient

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^{*} The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

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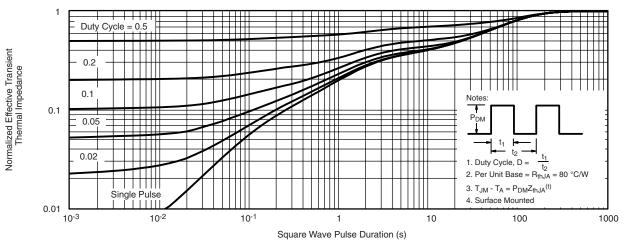
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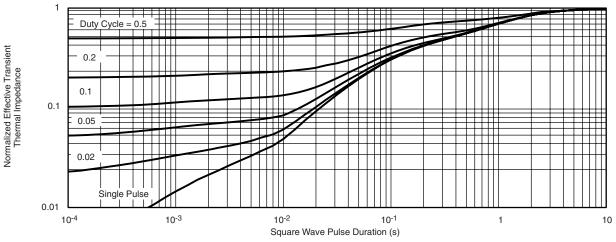
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TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?73581.



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