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[Vishay/Siliconix](#)
[SI4451DY-T1-E3](#)

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Si4451DY
Vishay Siliconix

P-Channel 12-V (D-S) MOSFET

PRODUCT SUMMARY

V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)
- 12	0.00825 at $V_{GS} = - 4.5$ V	- 14
	0.01025 at $V_{GS} = - 2.5$ V	- 13
	0.013 at $V_{GS} = - 1.8$ V	- 12

FEATURES

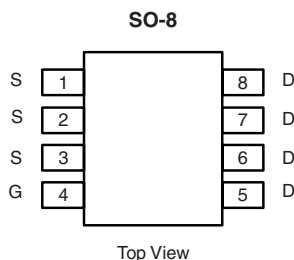
- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET® Power MOSFET
- Compliant to RoHS Directive 2002/95/EC



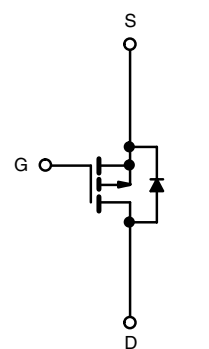
RoHS
COMPLIANT
HALOGEN
FREE
Available

APPLICATIONS

- Load Switch
- Battery Switch



Ordering Information: Si4451DY-T1-E3 (Lead (Pb)-free)
Si4451DY-T1-GE3 (Lead (Pb)-free and Halogen-free)



P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS $T_A = 25^\circ\text{C}$, unless otherwise noted

Parameter		Symbol	10 s	Steady State	Unit
Drain-Source Voltage		V _{DS}	- 12		V
Gate-Source Voltage		V _{GS}	± 8		
Continuous Drain Current (T _J = 150 °C) ^a	T _A = 25 °C	I _D	- 14	- 10	A
	T _A = 70 °C		- 11	- 8	
Pulsed Drain Current		I _{DM}	- 40		
Continuous Source Current (Diode Conduction) ^a		I _S	- 2.7	- 1.35	
Maximum Power Dissipation ^a	T _A = 25 °C	P _D	3.0	1.5	W
	T _A = 70 °C		1.9	0.95	
Operating Junction and Storage Temperature Range		T _J , T _{stg}	- 55 to 150		°C

THERMAL RESISTANCE RATINGS

Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^a	$t \leq 10$ s	R_{thJA}	33	42	$^\circ\text{C/W}$
	Steady State		70	85	
Maximum Junction-to-Foot (Drain)	Steady State	R_{thJF}	17	21	

Notes:

a. Surface Mounted on 1" x 1" FR4 board.

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SPECIFICATIONS $T_J = 25\text{ }^{\circ}\text{C}$, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = -850\text{ }\mu\text{A}$	-0.40		-0.8	V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 8\text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -12\text{ V}$, $V_{GS} = 0\text{ V}$			-1	μA
		$V_{DS} = -12\text{ V}$, $V_{GS} = 0\text{ V}$, $T_J = 70\text{ }^{\circ}\text{C}$			-5	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} = -5\text{ V}$, $V_{GS} = -4.5\text{ V}$	-30			A
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = -4.5\text{ V}$, $I_D = -14\text{ A}$		0.0065	0.00825	Ω
		$V_{GS} = -2.5\text{ V}$, $I_D = -13\text{ A}$		0.008	0.01025	
		$V_{GS} = -1.8\text{ V}$, $I_D = -12\text{ A}$		0.0105	0.013	
Forward Transconductance ^a	g_{fs}	$V_{DS} = -10\text{ V}$, $I_D = -14\text{ A}$		55		S
Diode Forward Voltage ^a	V_{SD}	$I_S = -2.7\text{ A}$, $V_{GS} = 0\text{ V}$		-0.6	-1.1	V
Dynamic^b						
Total Gate Charge	Q_g	$V_{DS} = -6\text{ V}$, $V_{GS} = -4.5\text{ V}$, $I_D = -14\text{ A}$		81	120	nC
Gate-Source Charge	Q_{gs}			8.6		
Gate-Drain Charge	Q_{gd}			23.4		
Gate Resistance	R_g			3.0		Ω
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -6\text{ V}$, $R_L = 6\text{ }\Omega$ $I_D \cong -1\text{ A}$, $V_{GEN} = -4.5\text{ V}$, $R_g = 6\text{ }\Omega$		55	85	ns
Rise Time	t_r			125	190	
Turn-Off Delay Time	$t_{d(off)}$			315	480	
Fall Time	t_f			235	360	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = -2.7\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$		185	300	

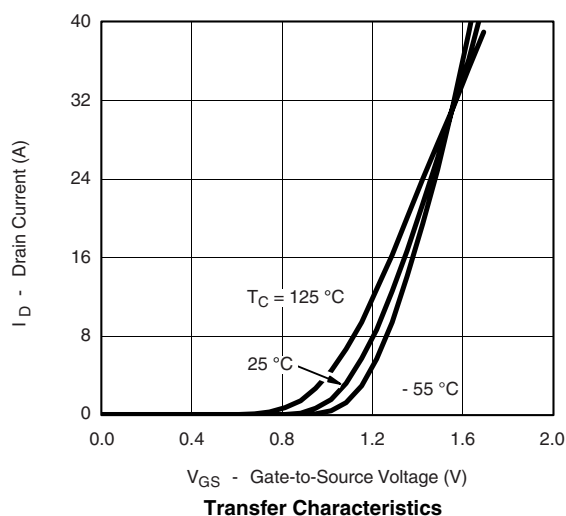
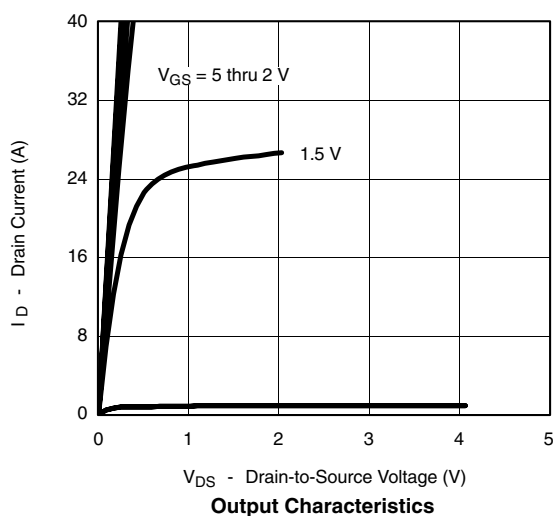
Notes:

a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS $25\text{ }^{\circ}\text{C}$, unless otherwise noted

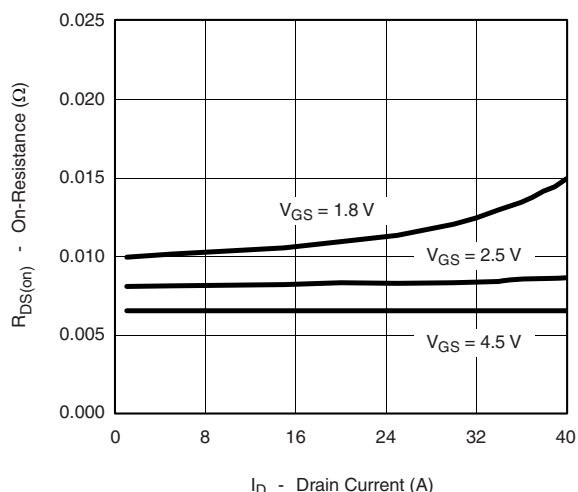




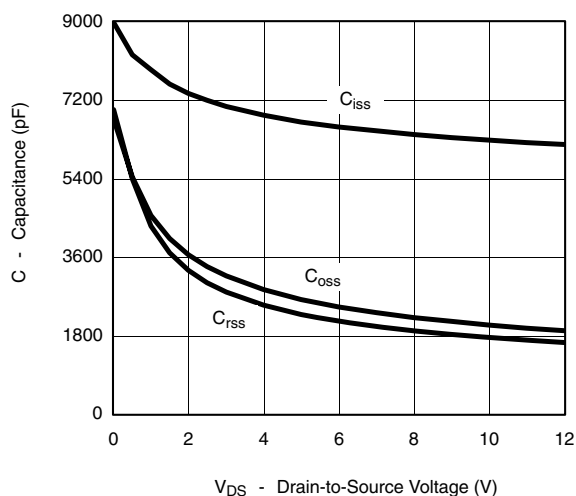
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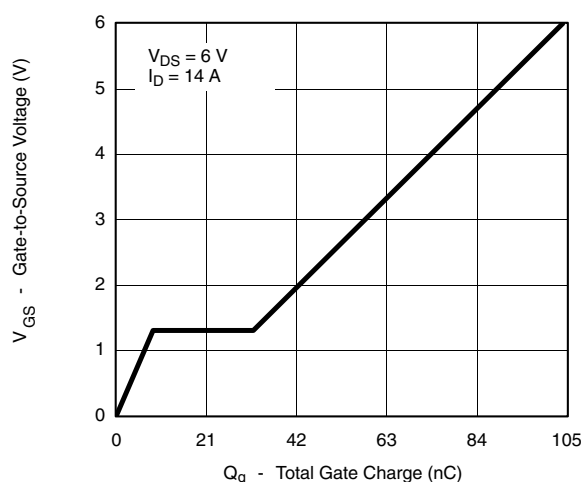
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



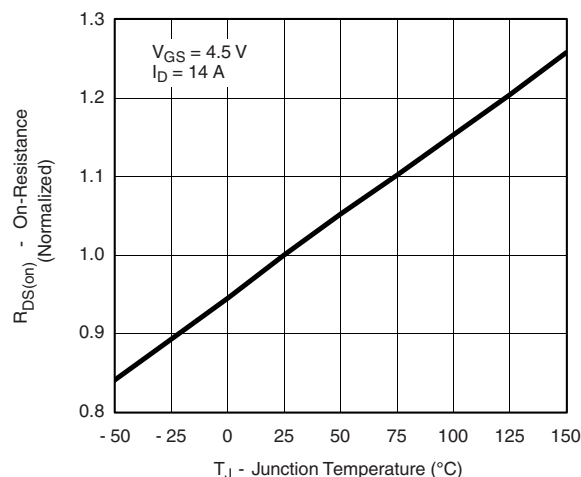
On-Resistance vs. Drain Current



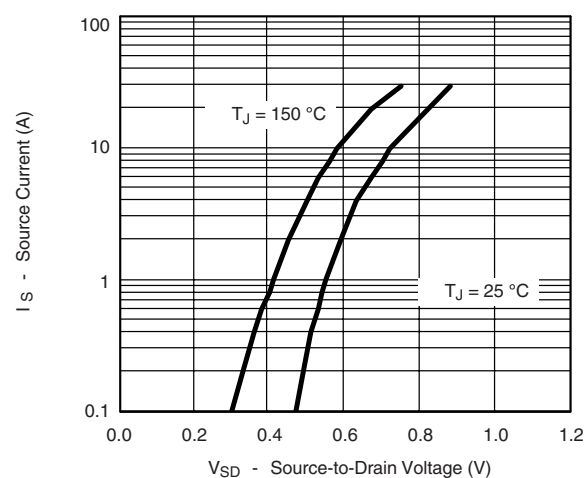
Capacitance



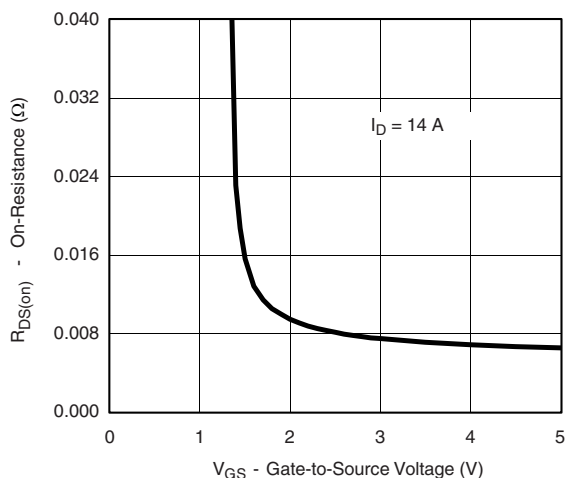
Gate Charge



On-Resistance vs. Junction Temperature



Source-Drain Diode Forward Voltage



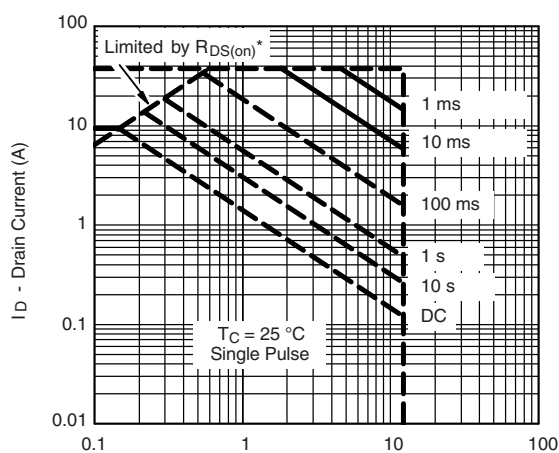
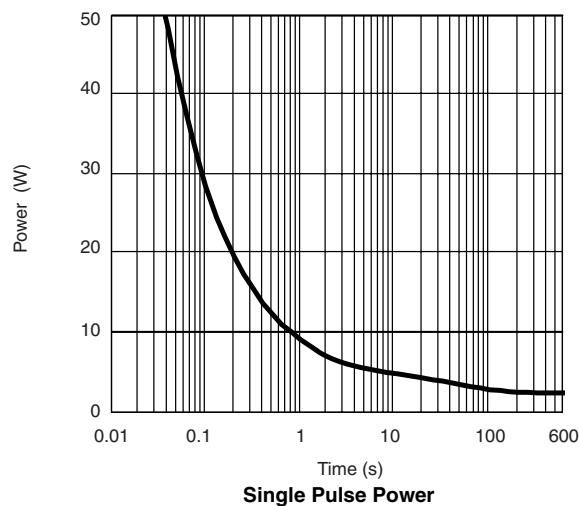
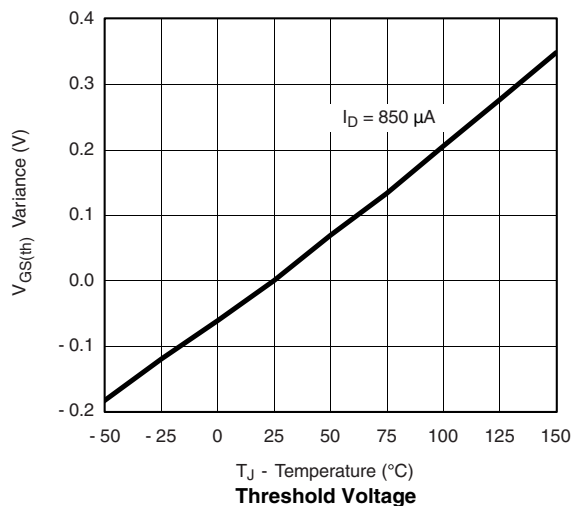
On-Resistance vs. Gate-to-Source Voltage

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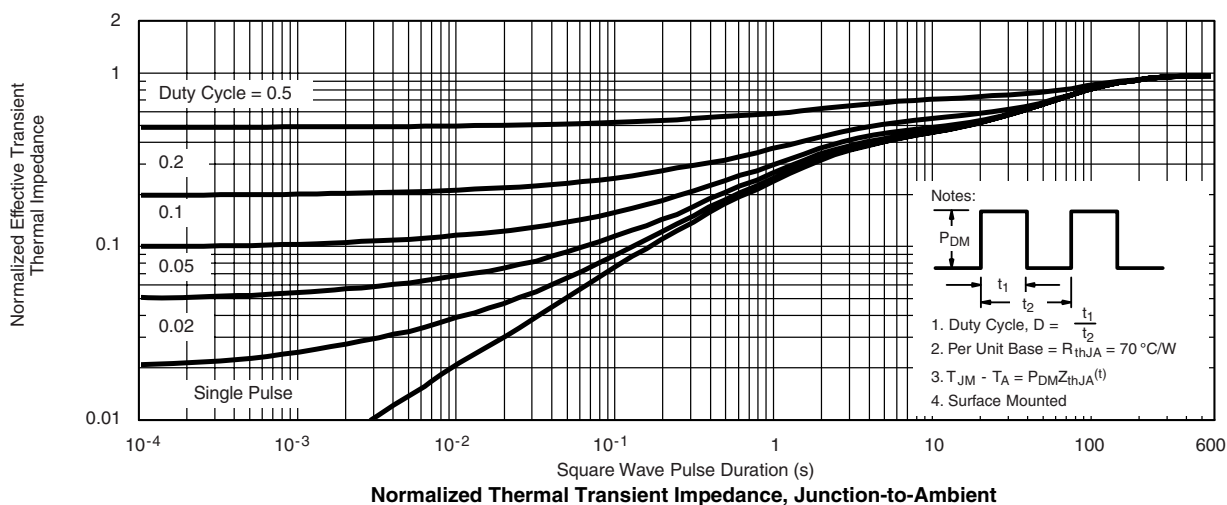


TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area, Junction-to-Case

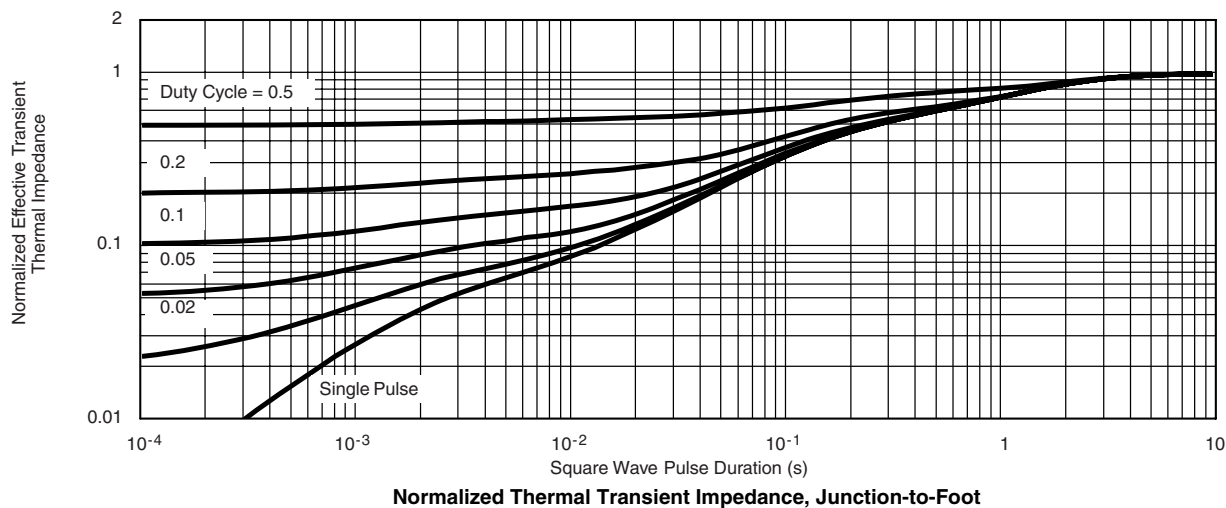




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TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?72115.

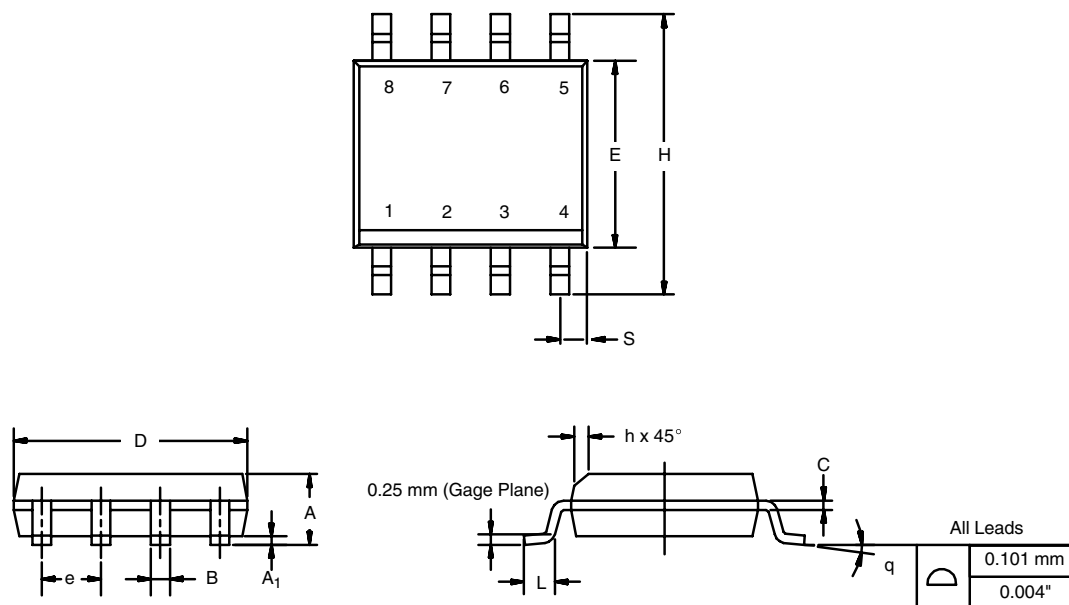


Package Information

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SOIC (NARROW): 8-LEAD

JEDEC Part Number: MS-012



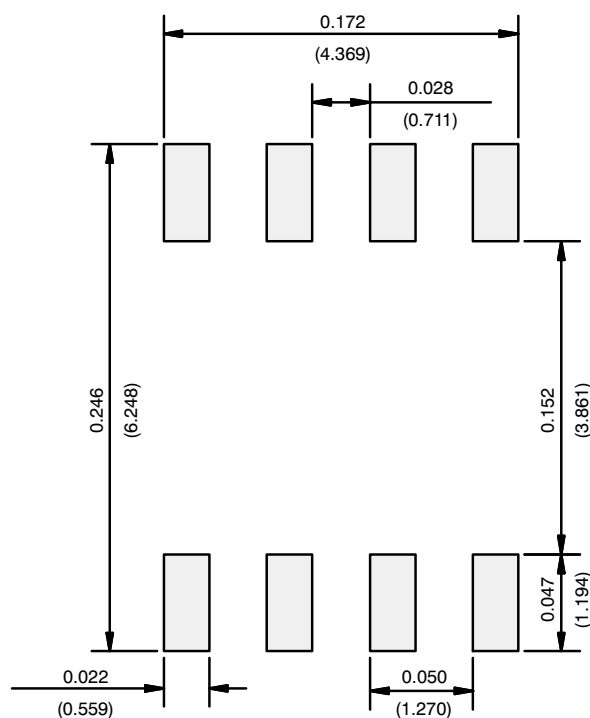
DIM	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A ₁	0.10	0.20	0.004	0.008
B	0.35	0.51	0.014	0.020
C	0.19	0.25	0.0075	0.010
D	4.80	5.00	0.189	0.196
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.020
L	0.50	0.93	0.020	0.037
q	0°	8°	0°	8°
S	0.44	0.64	0.018	0.026
ECN: C-06527-Rev. I, 11-Sep-06				
DWG: 5498				

Application Note 826

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RECOMMENDED MINIMUM PADS FOR SO-8



Recommended Minimum Pads
Dimensions in Inches/(mm)

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