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[Vishay/Siliconix](#)
[SI4532CDY-T1-GE3](#)

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Si4532CDY
 Vishay Siliconix

N- and P-Channel 30 V (D-S) MOSFET

PRODUCT SUMMARY				
	V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A) ^a	Q _g (Typ.)
N-Channel	30	0.047 at V _{GS} = 10 V	6.0	2.75
		0.065 at V _{GS} = 4.5 V	5.2	
P-Channel	- 30	0.089 at V _{GS} = - 10 V	- 4.3	4.1
		0.140 at V _{GS} = - 4.5 V	- 3.4	

FEATURES

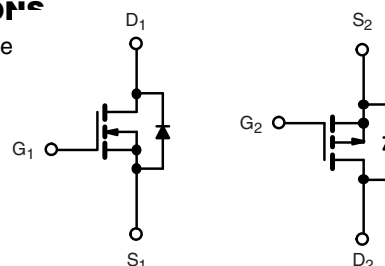
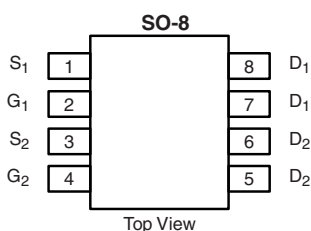
- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET[®] Power MOSFET
- 100 % R_g Tested
- 100 % UIS Tested
- Compliant to RoHS Directive 2002/95/EC



RoHS
 COMPLIANT
 HALOGEN
 FREE

APPLICATIONS

- DC/DC Converter
- Load Switch



Ordering Information: Si4532CDY-T1-GE3 (Lead (Pb)-free and Halogen-free)

N-Channel MOSFET P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C, unless otherwise noted)					
Parameter	Symbol	N-Channel	P-Channel	Unit	
Drain-Source Voltage	V _{DS}	30	- 30	V	
Gate-Source Voltage	V _{GS}	± 20			
Continuous Drain Current (T _J = 150 °C)	I _D	T _C = 25 °C	6.0	- 4.3	
		T _C = 70 °C	4.9	- 3.4	
		T _A = 25 °C	4.9 ^{b, c}	- 3.4 ^{b, c}	
		T _A = 70 °C	3.9 ^{b, c}	- 2.7 ^{b, c}	
Pulsed Drain Current (10 μs Pulse Width)	I _{DM}	24	- 15	A	
Source-Drain Current Diode Current	I _S	T _C = 25 °C	2.3		- 2.3
		T _A = 25 °C	1.5 ^{b, c}		- 1.5 ^{b, c}
Pulsed Source-Drain Current	I _{SM}	24	- 12		
Single Pulse Avalanche Current	L = 0.1 mH	I _{AS}	7	8	
Single Pulse Avalanche Energy		E _{AS}	2.5	3.2	mJ
Maximum Power Dissipation	P _D	T _C = 25 °C	2.78	2.78	
		T _C = 70 °C	1.78	1.78	
		T _A = 25 °C	1.78 ^{b, c}	1.78 ^{b, c}	
		T _A = 70 °C	1.14 ^{b, c}	1.14 ^{b, c}	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to 150		°C	

THERMAL RESISTANCE RATINGS							
Parameter	Symbol	N-Channel		P-Channel		Unit	
		Typ.	Max.	Typ.	Max.		
Maximum Junction-to-Ambient ^{b, d}	t ≤ 10 s	R _{thJA}	57	70	57	70	°C/W
Maximum Junction-to-Foot (Drain)	Steady State	R _{thJF}	37	45	37	45	

Notes:

- Based on T_C = 25 °C.
- Surface mounted on 1" x 1" FR4 board.
- t = 10 s.
- Maximum under steady state conditions is 120 °C/W (N-Channel) and 110 °C/W (P-Channel).

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SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)							
Parameter	Symbol	Test Conditions		Min.	Typ. ^a	Max.	Unit
Static							
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	N-Ch	30			V
		$V_{GS} = 0\text{ V}, I_D = -250\text{ }\mu\text{A}$	P-Ch	-30			
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 250\text{ }\mu\text{A}$	N-Ch		33		mV/ $^\circ\text{C}$
		$I_D = -250\text{ }\mu\text{A}$	P-Ch		-33		
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	$I_D = 250\text{ }\mu\text{A}$	N-Ch		-5.8		
		$I_D = -250\text{ }\mu\text{A}$	P-Ch		4.5		
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	N-Ch	1.0		3.0	V
		$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$	P-Ch	-1.0		-3.0	
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$	N-Ch			100	nA
			P-Ch			-100	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V}$	N-Ch			1	μA
		$V_{DS} = -30\text{ V}, V_{GS} = 0\text{ V}$	P-Ch			-1	
		$V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$	N-Ch			5	
		$V_{DS} = -30\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$	P-Ch			-5	
On-State Drain Current ^b	$I_{D(on)}$	$V_{DS} = 5\text{ V}, V_{GS} = 10\text{ V}$	N-Ch	20			A
		$V_{DS} = -5\text{ V}, V_{GS} = -10\text{ V}$	P-Ch	-12			
Drain-Source On-State Resistance ^b	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 3.5\text{ A}$	N-Ch		0.038	0.047	Ω
		$V_{GS} = -10\text{ V}, I_D = -3.5\text{ A}$	P-Ch		0.073	0.089	
		$V_{GS} = 4.5\text{ V}, I_D = 2.8\text{ A}$	N-Ch		0.052	0.065	
		$V_{GS} = -4.5\text{ V}, I_D = -2.5\text{ A}$	P-Ch		0.113	0.140	
Forward Transconductance ^b	g_{fs}	$V_{DS} = 15\text{ V}, I_D = 2.5\text{ A}$	N-Ch		7		S
		$V_{DS} = -15\text{ V}, I_D = -3.5\text{ A}$	P-Ch		7		
Dynamic^a							
Input Capacitance	C_{iss}	N-Channel $V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	N-Ch		305		pF
Output Capacitance	C_{oss}		P-Ch		340		
Reverse Transfer Capacitance	C_{rss}	P-Channel $V_{DS} = -15\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	N-Ch		65		
			P-Ch		67		
Total Gate Charge	Q_g	$V_{DS} = 15\text{ V}, V_{GS} = 10\text{ V}, I_D = 2.5\text{ A}$	N-Ch		6	9	nC
		$V_{DS} = -15\text{ V}, V_{GS} = -10\text{ V}, I_D = -2.5\text{ A}$	P-Ch		7.8	12	
Gate-Source Charge	Q_{gs}	N-Channel $V_{DS} = 15\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 2.5\text{ A}$	N-Ch		2.75	4.5	
			P-Ch		4.1	6.2	
		P-Channel $V_{DS} = -15\text{ V}, V_{GS} = -4.5\text{ V}, I_D = -2.5\text{ A}$	N-Ch		1.3		
			P-Ch		1.3		
Gate-Drain Charge	Q_{gd}	N-Channel $V_{DS} = -15\text{ V}, V_{GS} = -4.5\text{ V}, I_D = -2.5\text{ A}$	N-Ch		0.9		
			P-Ch		1.8		
Gate Resistance	R_g	$f = 1\text{ MHz}$	N-Ch	0.6	3.1	6.2	Ω
			P-Ch	2.0	10	20	



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SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)						
Parameter	Symbol	Test Conditions	Min.	Typ. ^a	Max.	Unit
Dynamic^a						
Turn-On Delay Time	$t_{d(on)}$	N-Channel $V_{DD} = 15\text{ V}, R_L = 15\text{ }\Omega$ $I_D \approx 1\text{ A}, V_{GEN} = 10\text{ V}, R_g = 1\text{ }\Omega$	N-Ch	7	11	ns
			P-Ch	5.5	10	
Rise Time	t_r		N-Ch	12	18	
			P-Ch	13	25	
Turn-Off Delay Time	$t_{d(off)}$	P-Channel $V_{DD} = -15\text{ V}, R_L = 15\text{ }\Omega$ $I_D \approx -1\text{ A}, V_{GEN} = -10\text{ V}, R_g = 1\text{ }\Omega$	N-Ch	14	25	
			P-Ch	17	30	
Fall Time	t_f		N-Ch	6	10	
			P-Ch	7.7	15	
Turn-On Delay Time	$t_{d(on)}$	N-Channel $V_{DD} = 15\text{ V}, R_L = 15\text{ }\Omega$ $I_D \approx 1\text{ A}, V_{GEN} = 4.5\text{ V}, R_g = 1\text{ }\Omega$	N-Ch	16	30	
			P-Ch	40	60	
Rise Time	t_r		N-Ch	16	30	
			P-Ch	40	60	
Turn-Off Delay Time	$t_{d(off)}$	P-Channel $V_{DD} = -15\text{ V}, R_L = 15\text{ }\Omega$ $I_D \approx -1\text{ A}, V_{GEN} = -4.5\text{ V}, R_g = 1\text{ }\Omega$	N-Ch	9	18	
			P-Ch	20	40	
Fall Time	t_f		N-Ch	9	18	
			P-Ch	17	30	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	$T_C = 25\text{ }^\circ\text{C}$	N-Ch		2.3	A
			P-Ch		-2.3	
Pulse Diode Forward Current ^a	I_{SM}		N-Ch		24	A
			P-Ch		-12	
Body Diode Voltage	V_{SD}	$I_S = 1.25\text{ A}$	N-Ch	0.8	1.2	V
		$I_S = -0.75\text{ A}$	P-Ch	-0.8	-1.2	
Body Diode Reverse Recovery Time	t_{rr}	N-Channel $I_F = 1.25\text{ A}, di/dt = 100\text{ A}/\mu\text{s}, T_J = 25\text{ }^\circ\text{C}$	N-Ch	14	21	ns
			P-Ch	17	30	
Body Diode Reverse Recovery Charge	Q_{rr}	P-Channel $I_F = -2.5\text{ A}, di/dt = -100\text{ A}/\mu\text{s}, T_J = 25\text{ }^\circ\text{C}$	N-Ch	6	10	nC
			P-Ch	11	20	
Reverse Recovery Fall Time	t_a		N-Ch	9		ns
			P-Ch	12		
Reverse Recovery Rise Time	t_b		N-Ch	5		
			P-Ch	5		

Notes:

a. Guaranteed by design, not subject to production testing.

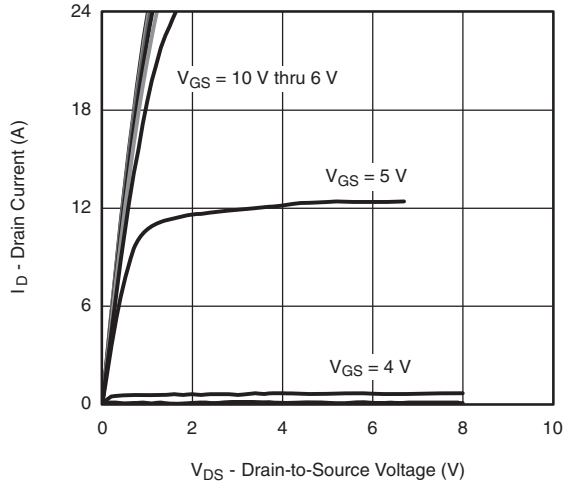
 b. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

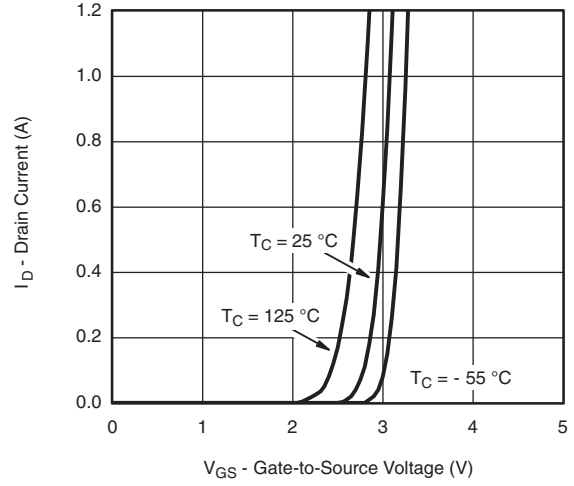
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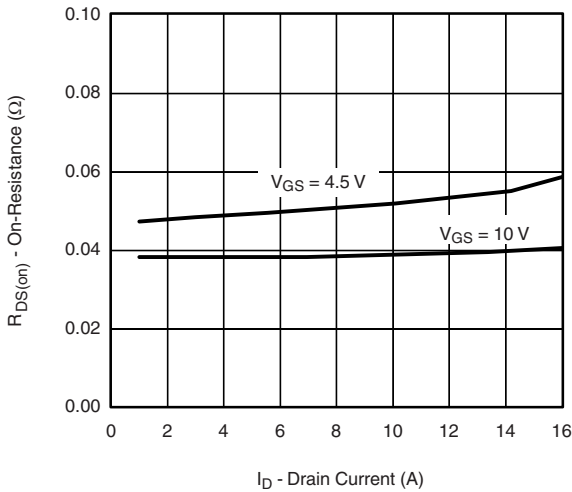
N-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



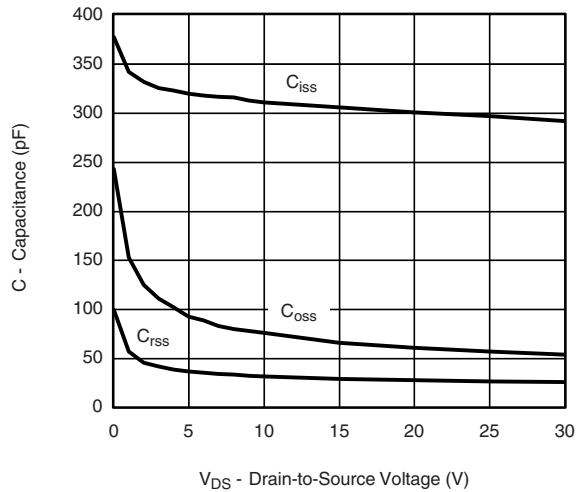
Output Characteristics



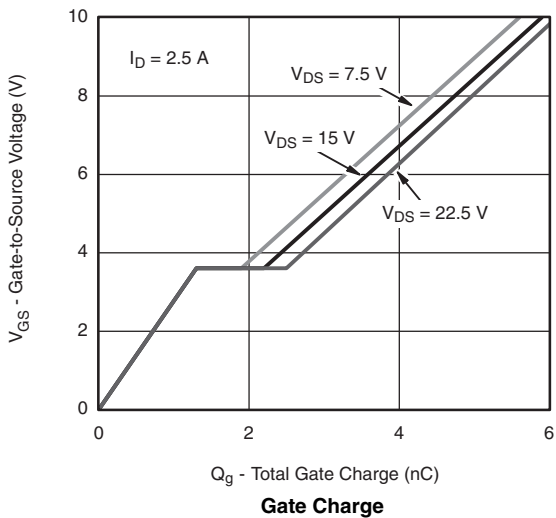
Transfer Characteristics



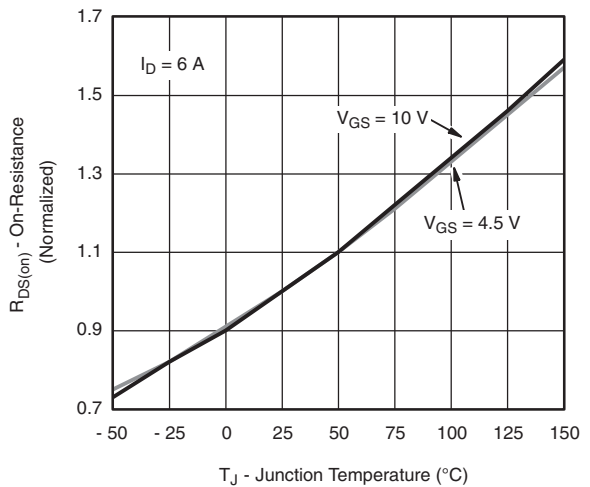
On-Resistance vs. Drain Current and Gate Voltage



Capacitance



Gate Charge

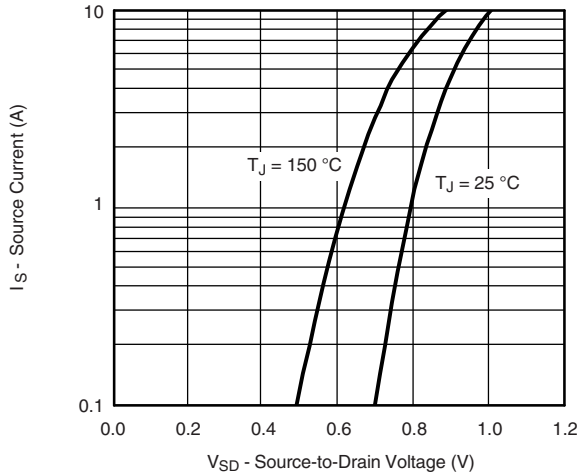


On-Resistance vs. Junction Temperature

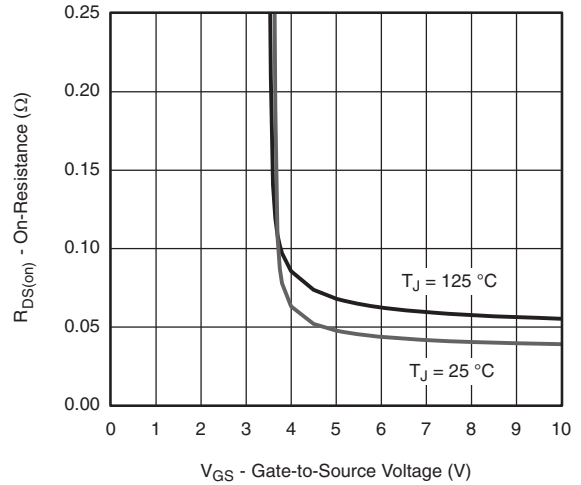


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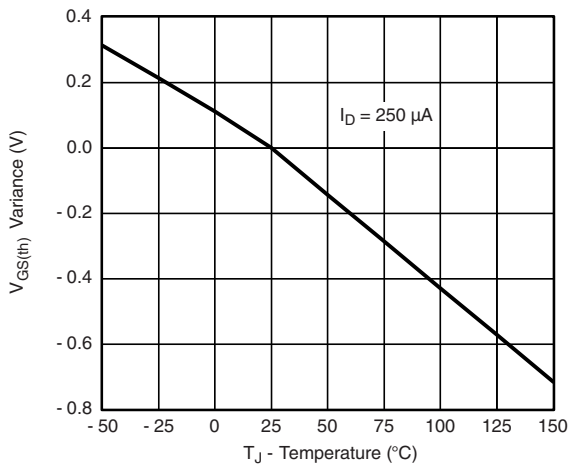
N-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



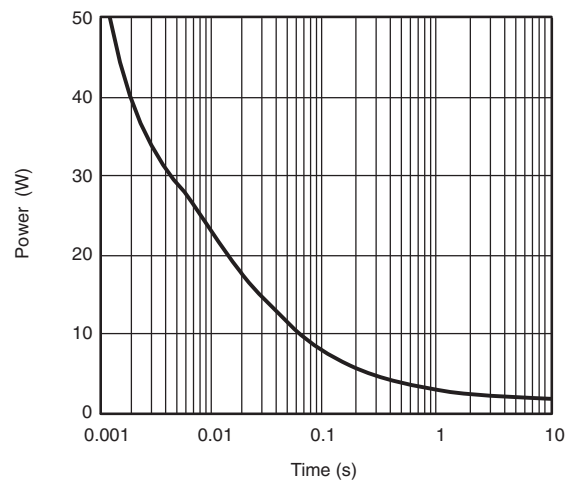
Source-Drain Diode Forward Voltage



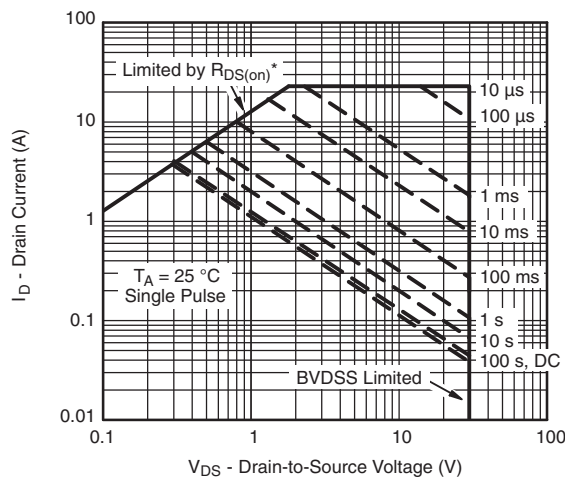
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



Single Pulse Power, Junction-to-Ambient

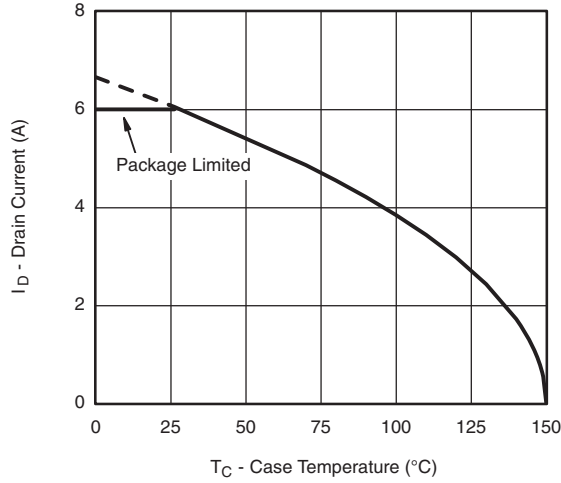


Safe Operating Area, Junction-to-Ambient

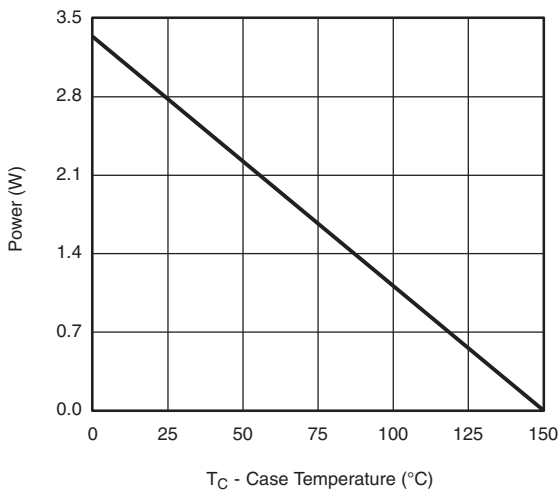
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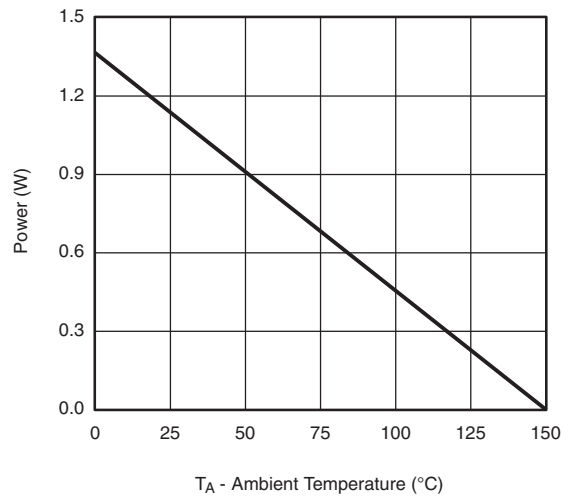
N-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Current Derating*



Power Derating, Junction-to-Foot



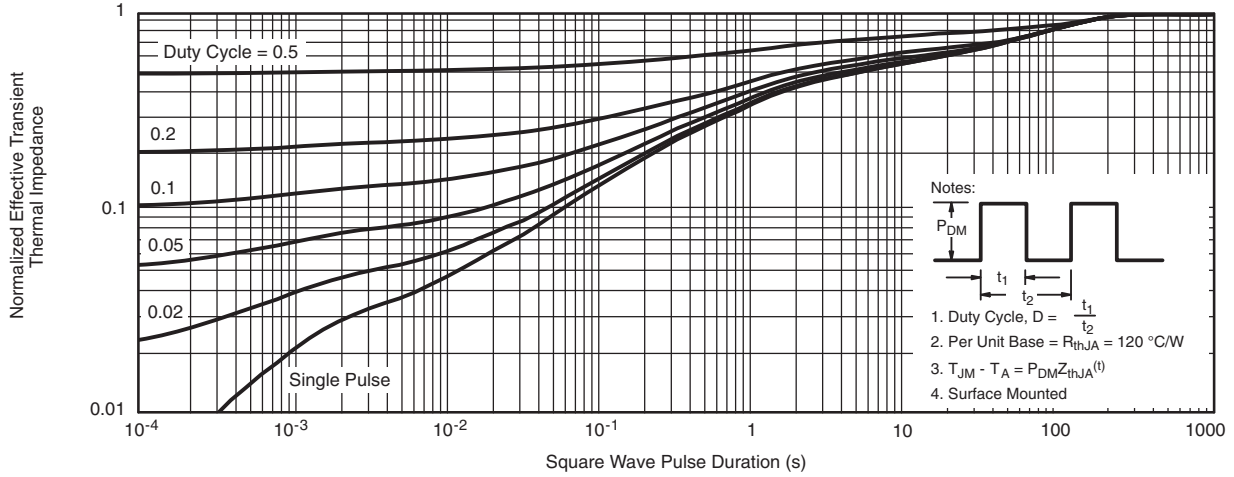
Power Derating, Junction-to-Ambient

* The power dissipation P_D is based on $T_{J(max)} = 150\text{ °C}$, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

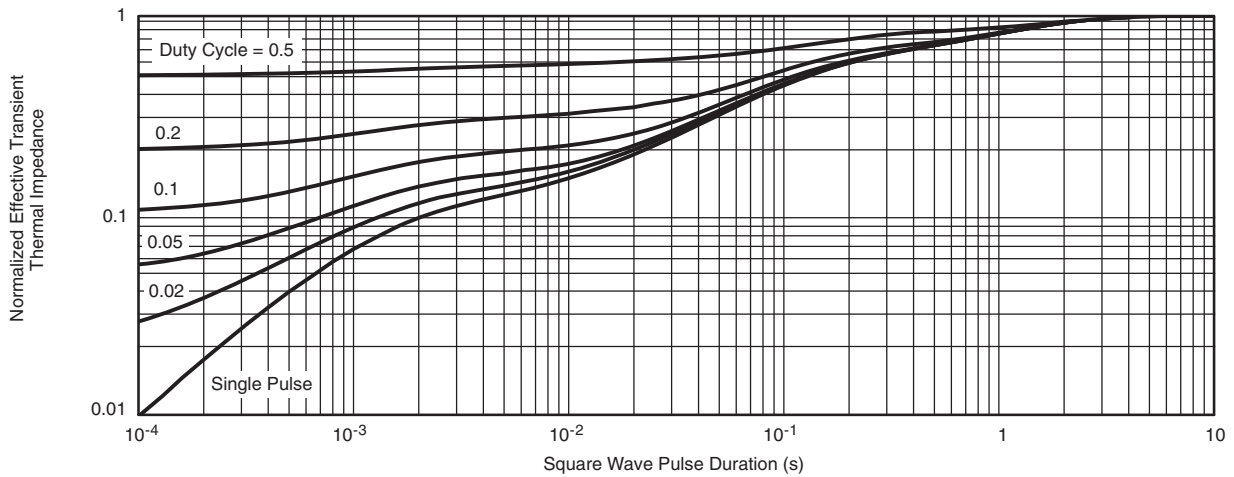


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N-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient

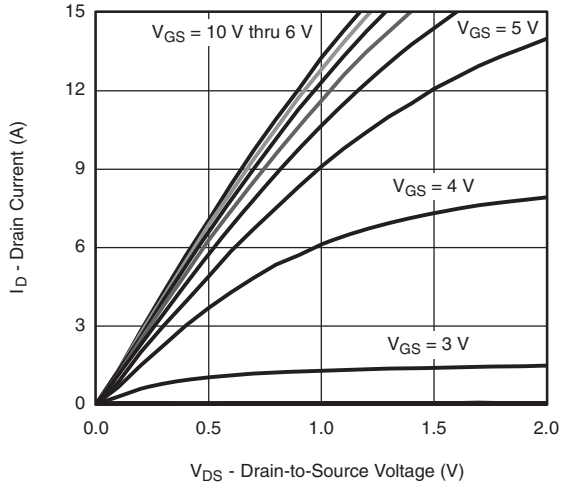


Normalized Thermal Transient Impedance, Junction-to-Foot

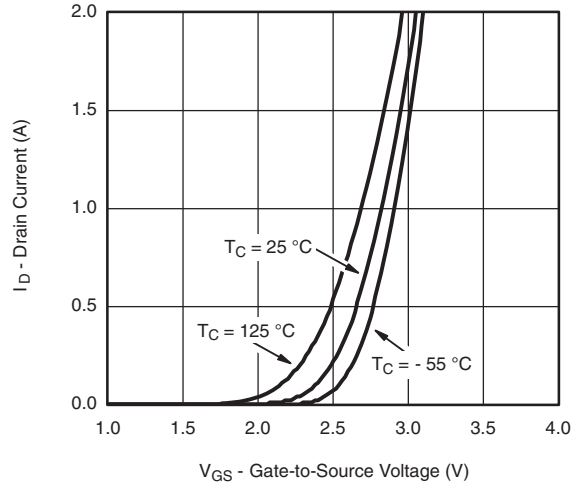
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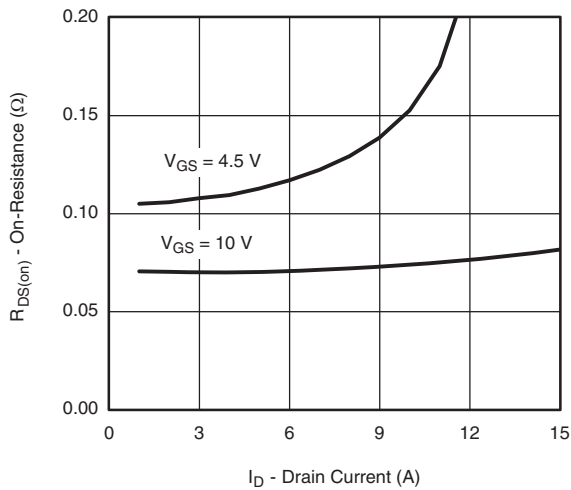
P-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



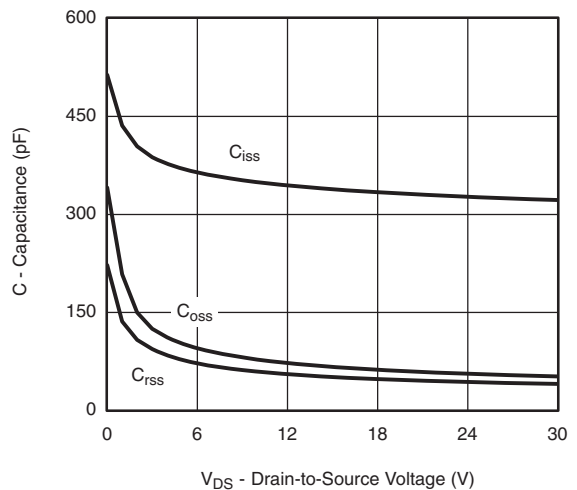
Output Characteristics



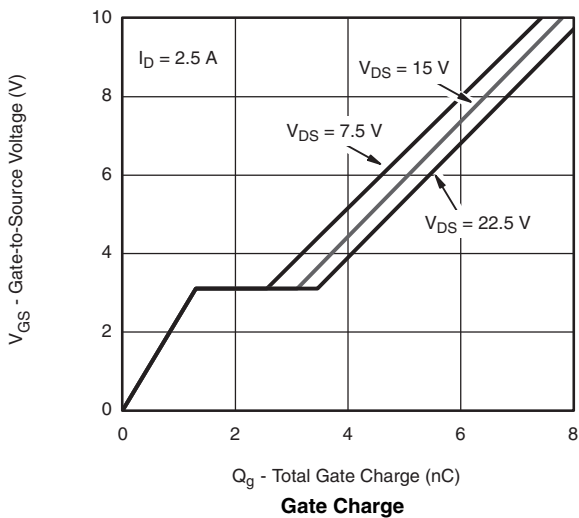
Transfer Characteristics



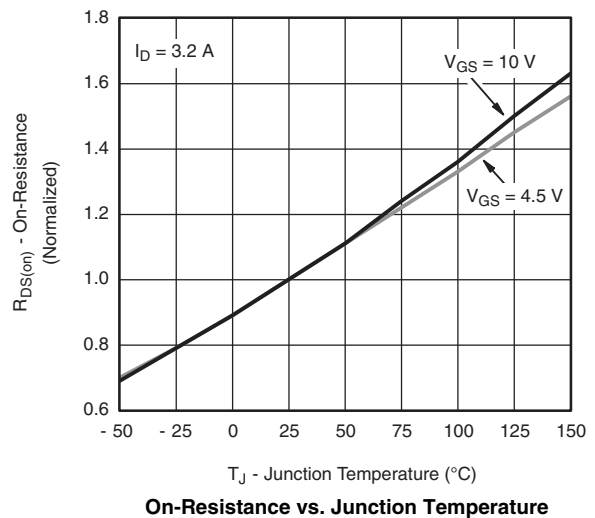
On-Resistance vs. Drain Current and Gate Voltage



Capacitance



Gate Charge

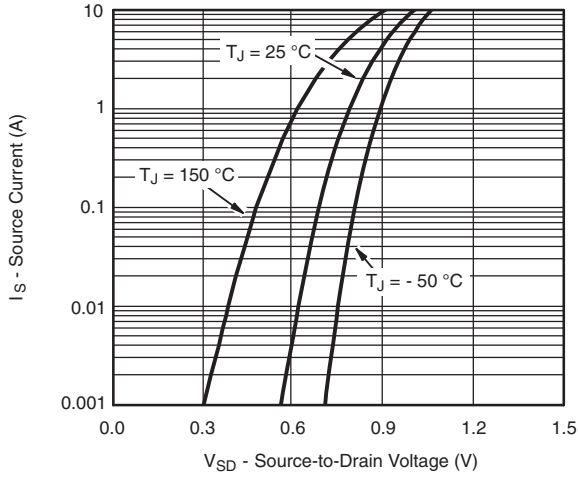


On-Resistance vs. Junction Temperature

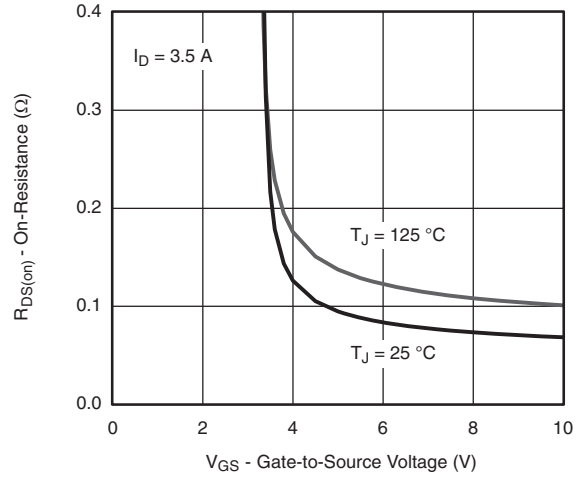


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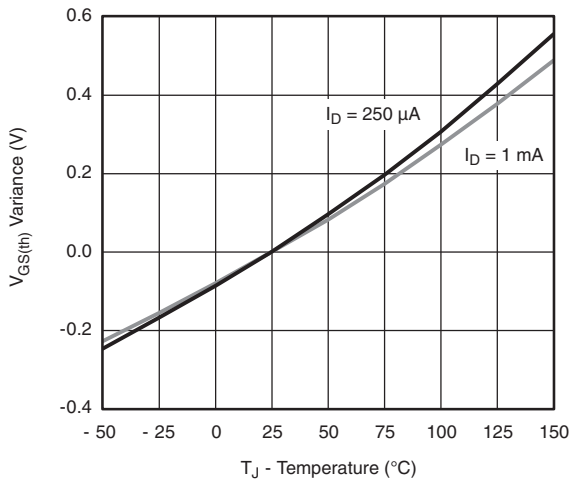
P-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



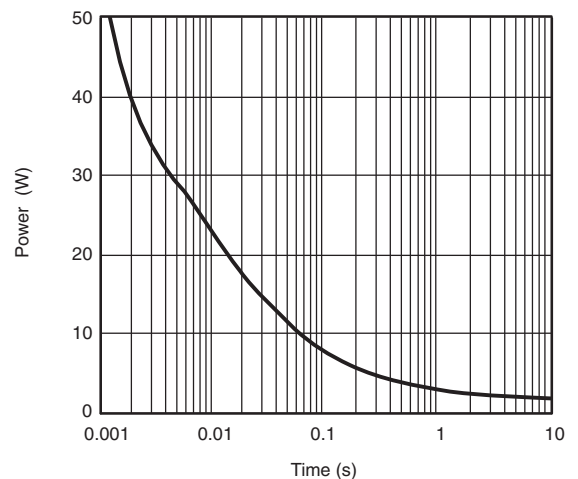
Source-Drain Diode Forward Voltage



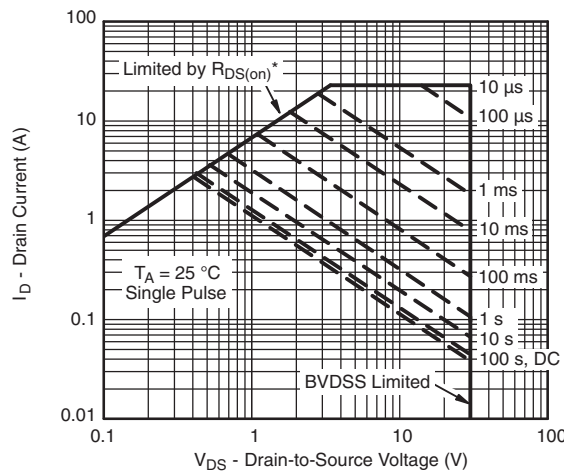
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



Single Pulse Power, Junction-to-Ambient



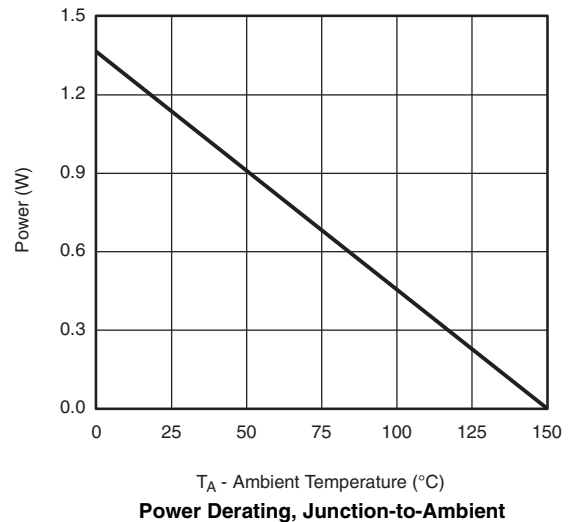
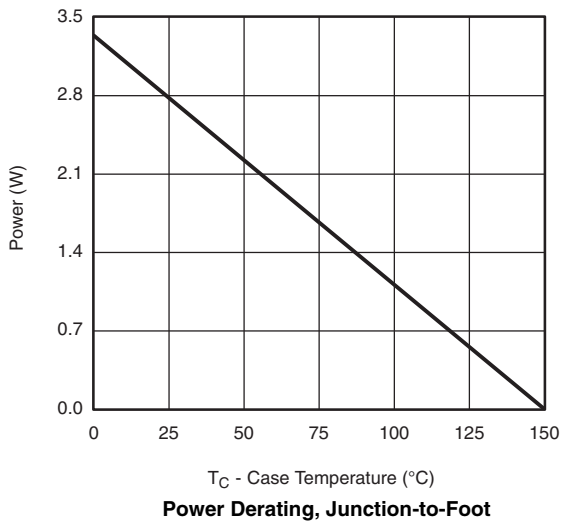
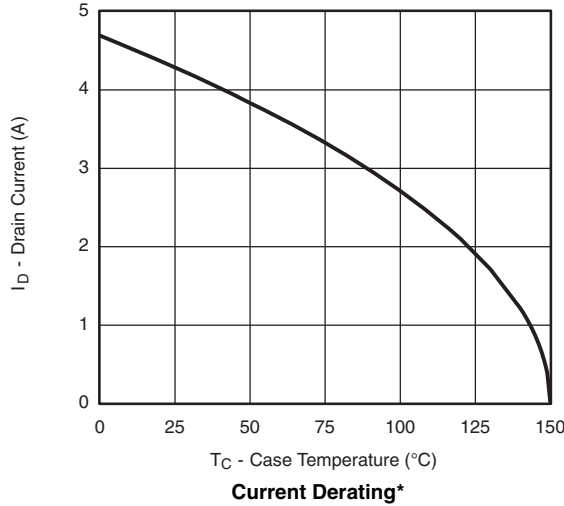
* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area, Junction-to-Ambient

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P-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

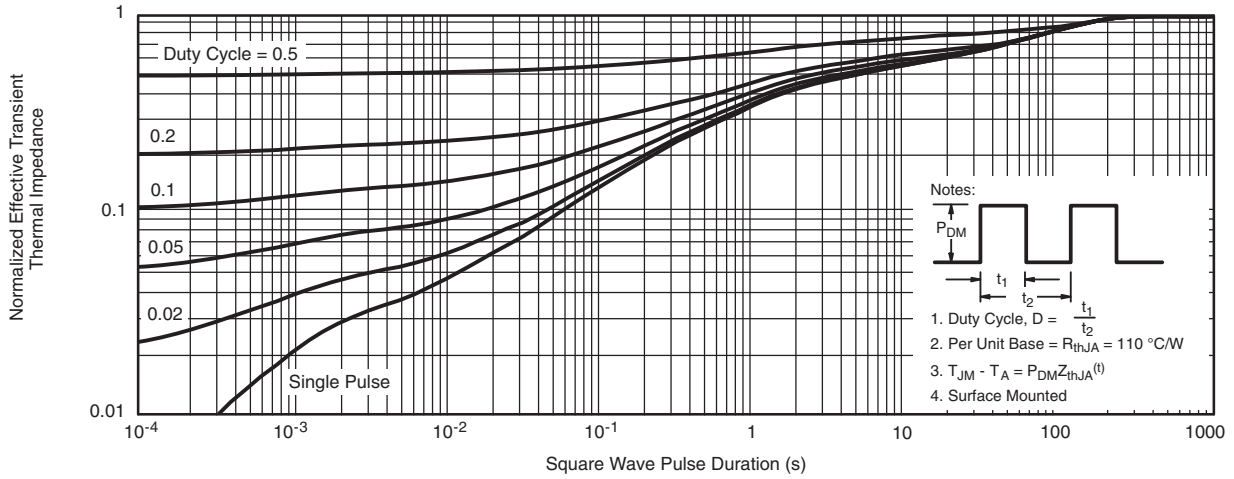


* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

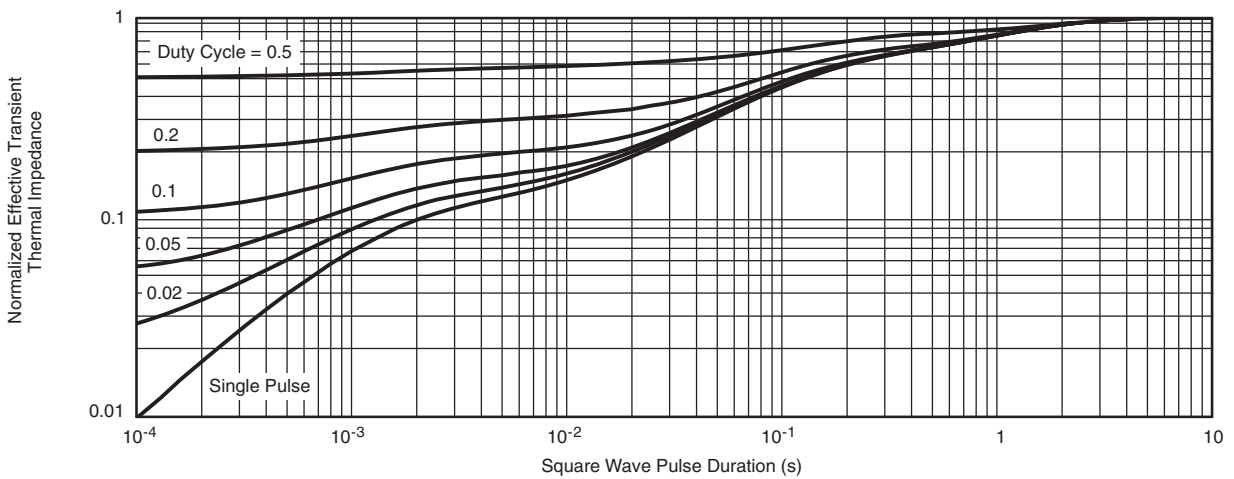


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P-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Foot

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppq?64805.

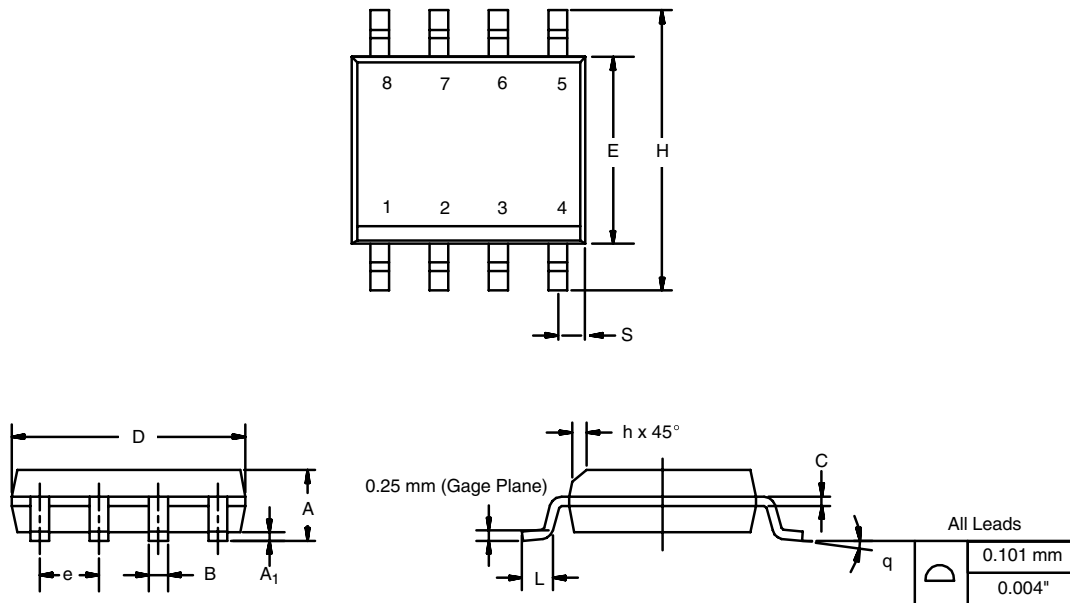


Package Information

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SOIC (NARROW): 8-LEAD

JEDEC Part Number: MS-012



DIM	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A ₁	0.10	0.20	0.004	0.008
B	0.35	0.51	0.014	0.020
C	0.19	0.25	0.0075	0.010
D	4.80	5.00	0.189	0.196
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.020
L	0.50	0.93	0.020	0.037
q	0°	8°	0°	8°
S	0.44	0.64	0.018	0.026

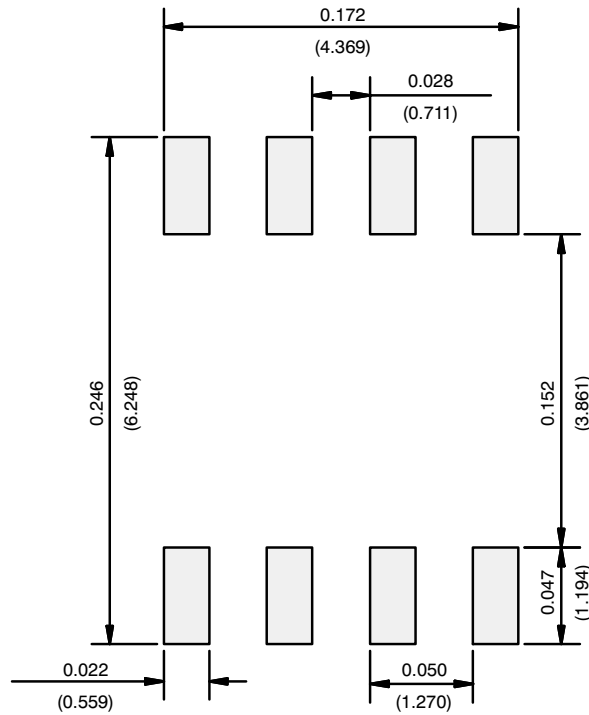
ECN: C-06527-Rev. I, 11-Sep-06
 DWG: 5498

Application Note 826

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RECOMMENDED MINIMUM PADS FOR SO-8



Recommended Minimum Pads
 Dimensions in Inches/(mm)

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APPLICATION NOTE



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