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[Vishay/Siliconix](#)
[SI4840BDY-T1-E3](#)

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sales@integrated-circuit.com



Si4840BDY
Vishay Siliconix

N-Channel 40-V (D-S) MOSFET

PRODUCT SUMMARY			
V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A) ^d	Q _g (Typ.)
40	0.009 at V _{GS} = 10 V	19	15 nC
	0.012 at V _{GS} = 4.5 V	16	

FEATURES

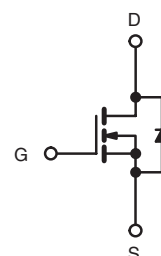
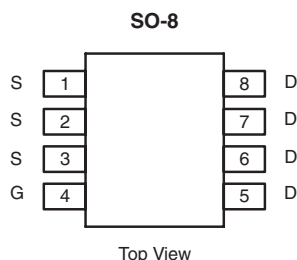
- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET[®] Power MOSFET
- 100 % R_g Tested
- 100 % UIS Tested
- Compliant to RoHS directive 2002/95/EC



RoHS
COMPLIANT
HALOGEN
FREE
Available

APPLICATIONS

- Synchronous Rectification
- POL, IBC
- Secondary Side



N-Channel MOSFET

Ordering Information: Si4840BDY-T1-E3 (Lead (Pb)-free)
 Si4840BDY-T1-GE3 (Lead (Pb)-free and Halogen-free)

ABSOLUTE MAXIMUM RATINGS T _A = 25 °C, unless otherwise noted				
Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V _{DS}	40	V
Gate-Source Voltage		V _{GS}	± 20	
Continuous Drain Current (T _J = 150 °C)	T _C = 25 °C	I _D	19	A
	T _C = 70 °C		15	
	T _A = 25 °C		12.4 ^{a, b}	
	T _A = 70 °C		9.9 ^{a, b}	
Pulsed Drain Current		I _{DM}	50	
Avalanche Current	L = 0.1 mH	I _{AS}	15	
Avalanche Energy		E _{AS}	11	mJ
Continuous Source-Drain Diode Current	T _C = 25 °C	I _S	5	A
	T _A = 25 °C		2.1 ^{a, b}	
Maximum Power Dissipation	T _C = 25 °C	P _D	6	W
	T _C = 70 °C		3.8	
	T _A = 25 °C		2.5 ^{a, b}	
	T _A = 70 °C		1.6 ^{a, b}	
Operating Junction and Storage Temperature Range		T _J , T _{stg}	- 55 to 150	°C

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{a, c}	t ≤ 10 s	R _{thJA}	37	50	°C/W
Maximum Junction-to-Foot (Drain)	Steady State	R _{thJF}	17	21	

Notes:

- Surface Mounted on 1" x 1" FR4 board.
- t = 10 s.
- Maximum under Steady State conditions is 85 °C/W.
- Based on T_C = 25 °C.

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SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	40			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 250\text{ }\mu\text{A}$		40		mV/ $^\circ\text{C}$
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			-6		
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	1		3	V
Gate-Source Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 40\text{ V}, V_{GS} = 0\text{ V}$			1	μA
		$V_{DS} = 40\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$			5	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}, V_{GS} = 10\text{ V}$	50			A
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 12.4\text{ A}$		0.0074	0.009	Ω
		$V_{GS} = 4.5\text{ V}, I_D = 10.8\text{ A}$		0.0095	0.012	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 15\text{ V}, I_D = 12.4\text{ A}$		56		S
Dynamic^b						
Input Capacitance	C_{iss}	$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		2000		pF
Output Capacitance	C_{oss}			260		
Reverse Transfer Capacitance	C_{rss}			150		
Total Gate Charge	Q_g	$V_{DS} = 10\text{ V}, V_{GS} = 10\text{ V}, I_D = 12.4\text{ A}$		33	50	nC
		$V_{DS} = 10\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 12.4\text{ A}$		15	23	
Q_{gs}			6.7			
Q_{gd}			5.1			
Gate Resistance	R_g	$f = 1\text{ MHz}$		1.4	2.1	Ω
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 20\text{ V}, R_L = 2\text{ }\Omega$ $I_D \cong 10\text{ A}, V_{GEN} = 4.5\text{ V}, R_g = 1\text{ }\Omega$		25	40	ns
Rise Time	t_r			12	20	
Turn-Off Delay Time	$t_{d(off)}$			25	40	
Fall Time	t_f			10	15	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 20\text{ V}, R_L = 2\text{ }\Omega$ $I_D \cong 10\text{ A}, V_{GEN} = 10\text{ V}, R_g = 1\text{ }\Omega$		10	15	
Rise Time	t_r			15	25	
Turn-Off Delay Time	$t_{d(off)}$			30	45	
Fall Time	t_f			10	15	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	$T_C = 25\text{ }^\circ\text{C}$			30	A
Pulse Diode Forward Current	I_{SM}				50	
Body Diode Voltage	V_{SD}	$I_S = 10\text{ A}, V_{GS} = 0\text{ V}$		0.8	1.2	V
Body Diode Reverse Recovery Time	t_{rr}	$I_F = 10\text{ A}, di/dt = 100\text{ A}/\mu\text{s}, T_J = 25\text{ }^\circ\text{C}$		30	60	ns
Body Diode Reverse Recovery Charge	Q_{rr}			26	52	nC
Reverse Recovery Fall Time	t_a			17.5		ns
Reverse Recovery Rise Time	t_b			12.5		

Notes:

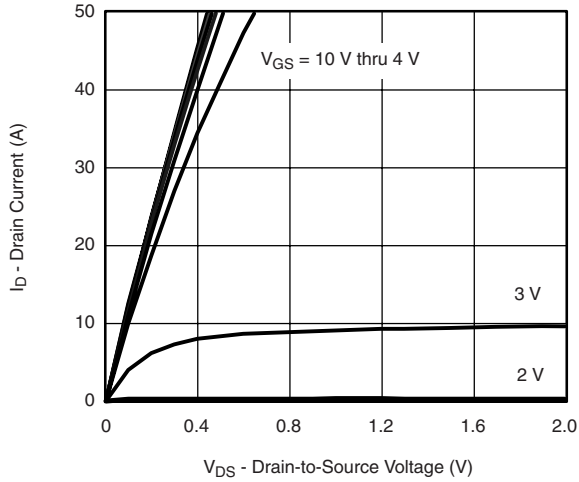
- Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$
- Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

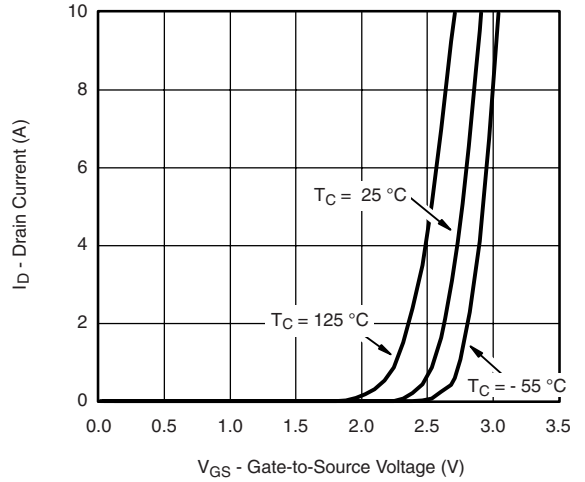


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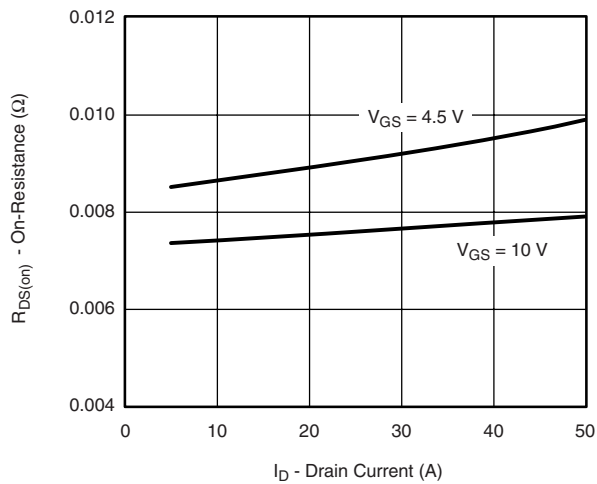
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



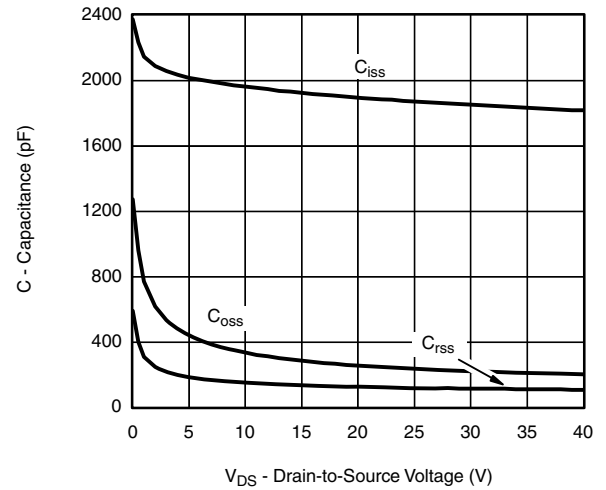
Output Characteristics



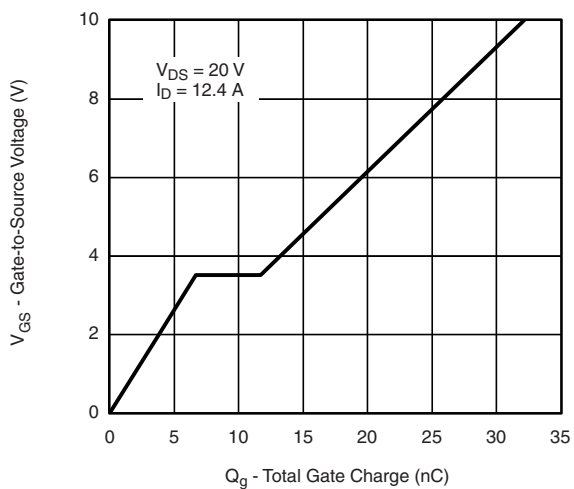
Transfer Characteristics



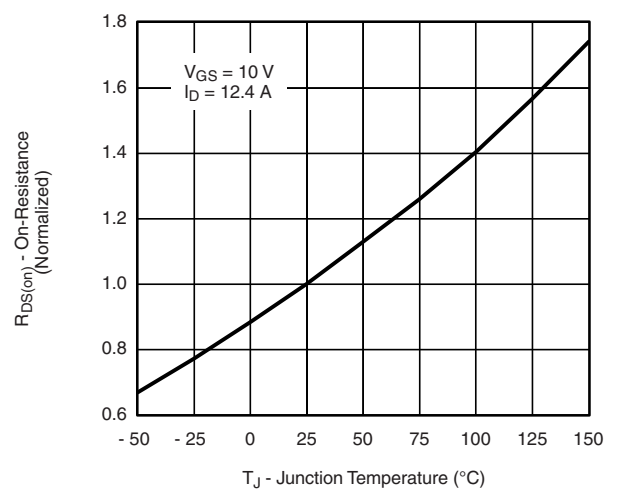
On-Resistance vs. Drain Current and Gate Voltage



Capacitance



Gate Charge



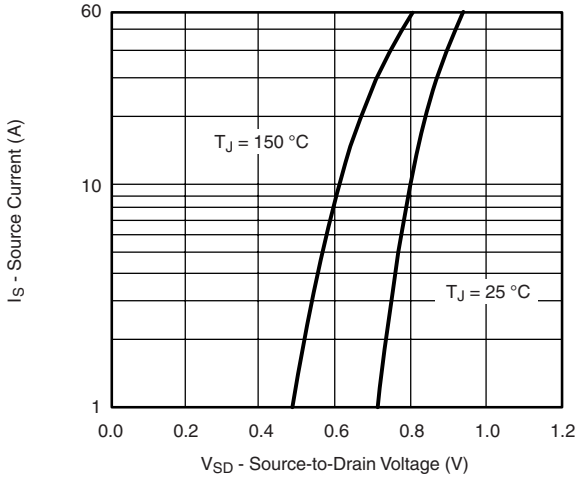
On-Resistance vs. Junction Temperature

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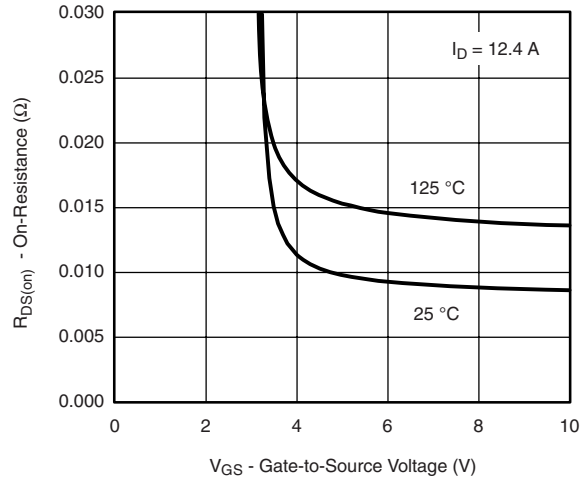
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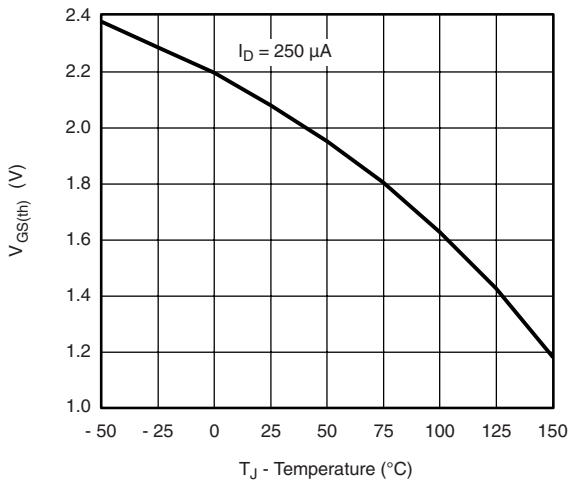
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



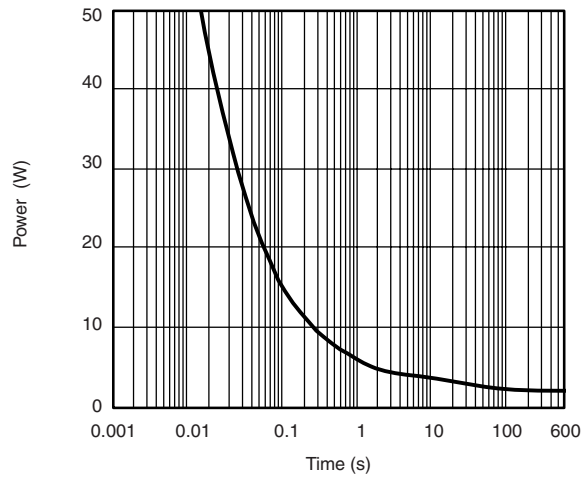
Source-Drain Diode Forward Voltage



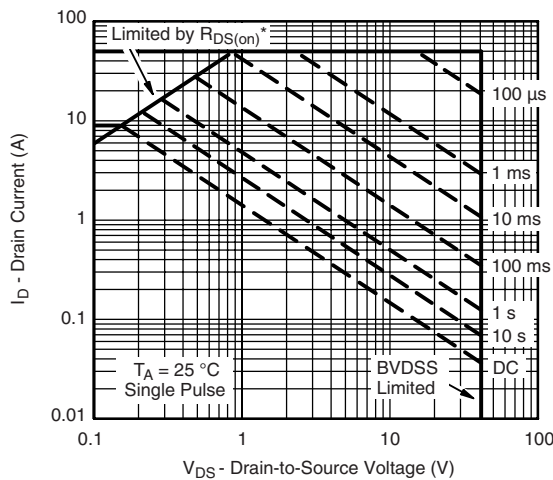
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



Single Pulse Power (Junction-to-Ambient)



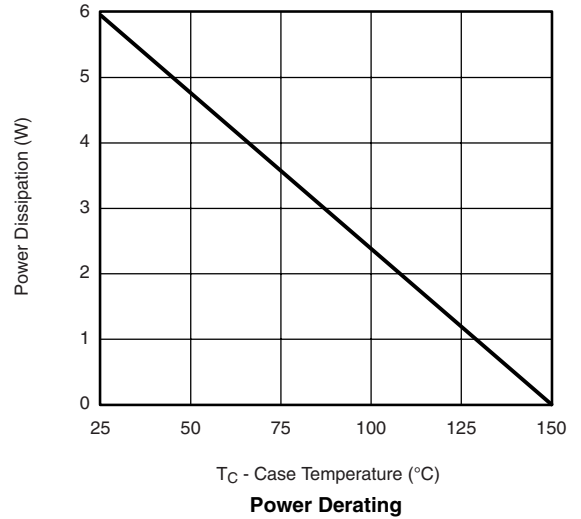
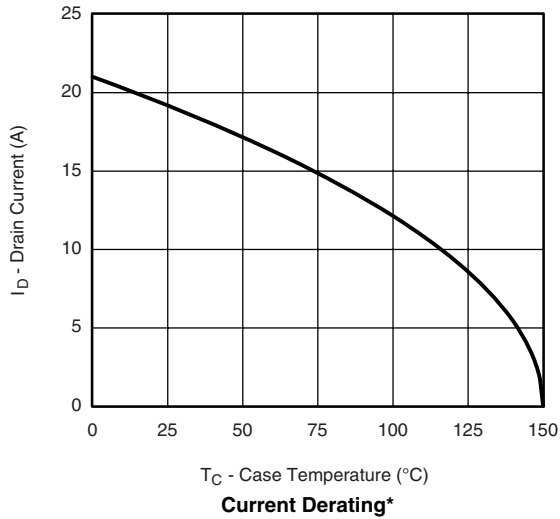
* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area, Junction-to-Ambient



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TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

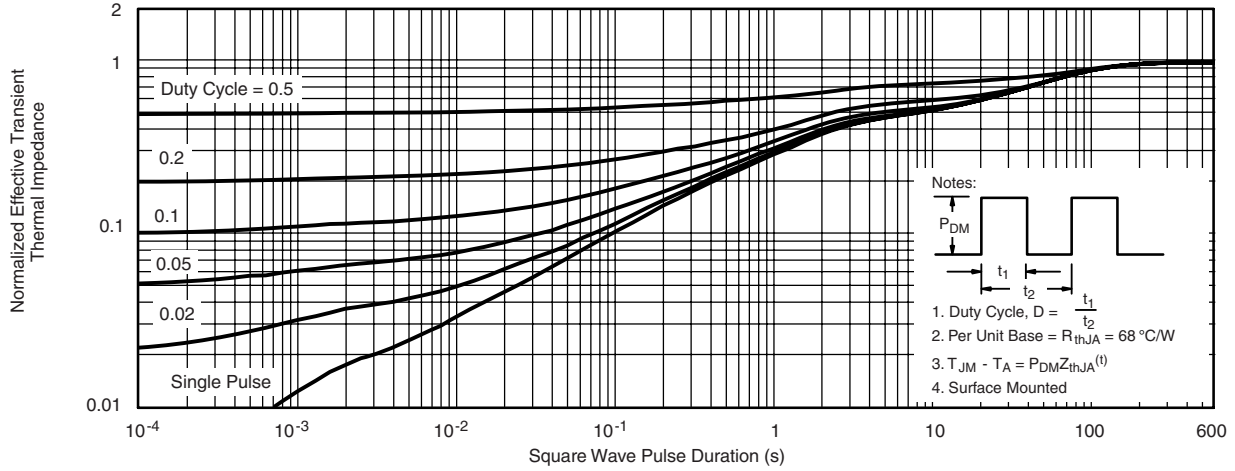


* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

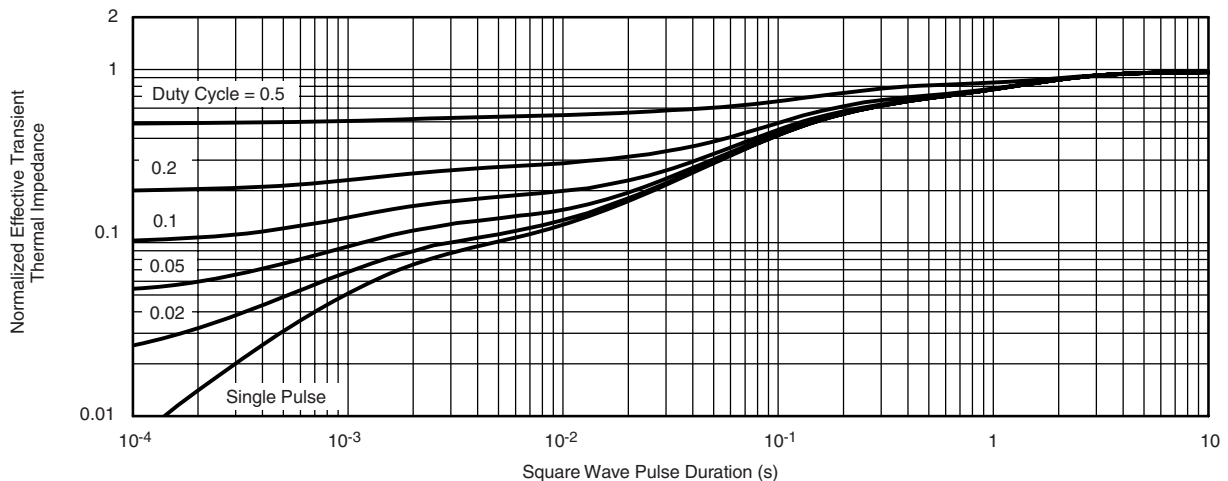
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TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Foot

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?69795.

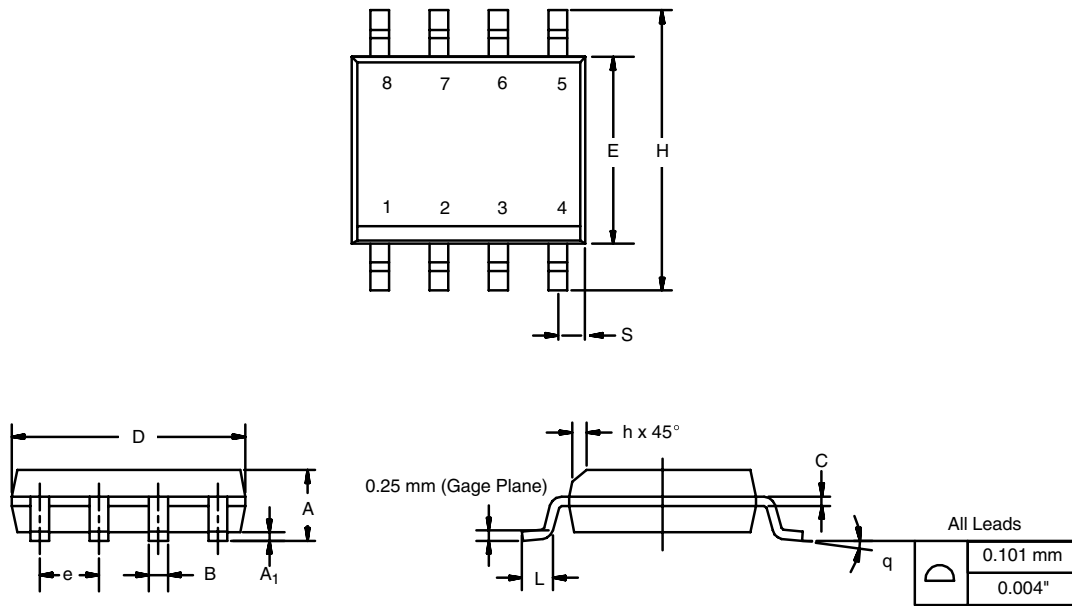


Package Information

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SOIC (NARROW): 8-LEAD

JEDEC Part Number: MS-012



DIM	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A ₁	0.10	0.20	0.004	0.008
B	0.35	0.51	0.014	0.020
C	0.19	0.25	0.0075	0.010
D	4.80	5.00	0.189	0.196
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.020
L	0.50	0.93	0.020	0.037
q	0°	8°	0°	8°
S	0.44	0.64	0.018	0.026

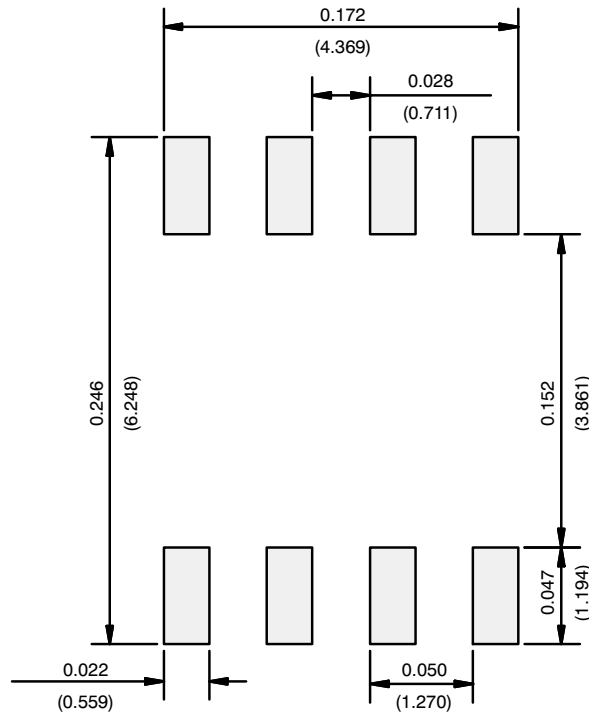
ECN: C-06527-Rev. I, 11-Sep-06
DWG: 5498

Application Note 826

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RECOMMENDED MINIMUM PADS FOR SO-8



Recommended Minimum Pads
 Dimensions in Inches/(mm)

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