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Stocking Distributor

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[Vishay/Siliconix](#)
[SI4866DY-T1-E3](#)

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Si4866DY

Vishay Siliconix

N-Channel Reduced Q_g, Fast Switching MOSFET

PRODUCT SUMMARY		
V_{DS} (V)	R_{DS(on)} (Ω)	I_D (A)
12	0.0055 at V _{GS} = 4.5 V	17
	0.008 at V _{GS} = 2.5 V	14

FEATURES

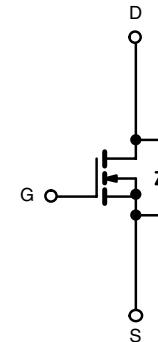
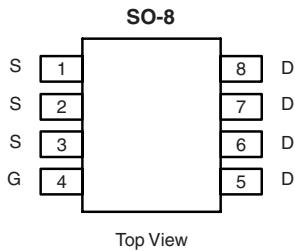
- Halogen-free According to IEC 61249-2-21 Available
- TrenchFET® Power MOSFETs
- PWM Optimized for High Efficiency
- Low Output Voltage
- 100 % R_g Tested



RoHS
COMPLIANT
HALOGEN
FREE
Available

APPLICATIONS

- Synchronous Rectifier
- Point-of-Load Synchronous Buck Converter



Ordering Information: Si4866DY-T1-E3 (Lead Pb)-free
Si4866DY-T1-GE3 (Lead Pb)-free and Halogen-free

N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS T _A = 25 °C, unless otherwise noted						
Parameter		Symbol	10 s	Steady State	Unit	
Drain-Source Voltage		V _{DS}	12		V	
Gate-Source Voltage		V _{GS}	± 8			
Continuous Drain Current (T _J = 150 °C) ^a	T _A = 25 °C	I _D	17	11	A	
	T _A = 70 °C		14	8		
Pulsed Drain Current		I _{DM}	± 50			
Continuous Source Current (Diode Conduction) ^a		I _S	2.7	1.40		
Maximum Power Dissipation ^a	T _A = 25 °C	P _D	3.0	1.6	W	
	T _A = 70 °C		2.0	1.0		
Operating Junction and Storage Temperature Range		T _J , T _{stg}	- 55 to 150		°C	

THERMAL RESISTANCE RATINGS					
Parameter	Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient (MOSFET) ^a	t ≤ 10 s	R _{thJA}	34	41	°C/W
	Steady State		67	80	
Maximum Junction-to-Foot (Drain)	Steady State	R _{thJF}	15	19	

Notes:

a. Surface Mounted on 1" x 1" FR4 board.

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MOSFET SPECIFICATIONS $T_J = 25^\circ\text{C}$, unless otherwise noted

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Gate Threshold Voltage	$V_{GS(\text{th})}$	$V_{DS} = V_{GS}$, $I_D = 250 \mu\text{A}$	0.6			V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0 \text{ V}$, $V_{GS} = \pm 8 \text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 9.6 \text{ V}$, $V_{GS} = 0 \text{ V}$		1		μA
		$V_{DS} = 9.6 \text{ V}$, $V_{GS} = 0 \text{ V}$, $T_J = 70^\circ\text{C}$		5		
On-State Drain Current ^a	$I_{D(\text{on})}$	$V_{DS} \geq 5 \text{ V}$, $V_{GS} = 4.5 \text{ V}$	40			A
Drain-Source On-State Resistance ^a	$R_{DS(\text{on})}$	$V_{GS} = 4.5 \text{ V}$, $I_D = 17$		0.0045	0.0055	Ω
		$V_{GS} = 2.5 \text{ V}$, $I_D = 14$		0.0065	0.008	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 6 \text{ V}$, $I_D = 17$		80		S
Diode Forward Voltage ^a	V_{SD}	$I_S = 2.7 \text{ A}$, $V_{GS} = 0 \text{ V}$		0.70	1.1	V
Dynamic^b						
Total Gate Charge	Q_g	$V_{DS} = 6 \text{ V}$, $V_{GS} = 4.5 \text{ V}$, $I_D = 17 \text{ A}$		21	30	nC
Gate-Source Charge	Q_{gs}			4.6		
Gate-Drain Charge	Q_{gd}			3.5		
Gate Resistance	R_G		1.5	2.3	3.9	Ω
Turn-On Delay Time	$t_{d(\text{on})}$	$V_{DD} = 6 \text{ V}$, $R_L = 6 \Omega$ $I_D \geq 1 \text{ A}$, $V_{GEN} = 4.5 \text{ V}$, $R_G = 6 \Omega$		28	42	ns
Rise Time	t_r			32	48	
Turn-Off Delay Time	$t_{d(\text{off})}$			82	123	
Fall Time	t_f			35	53	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = 2.7 \text{ A}$, $dI/dt = 100 \text{ A}/\mu\text{s}$		60	90	

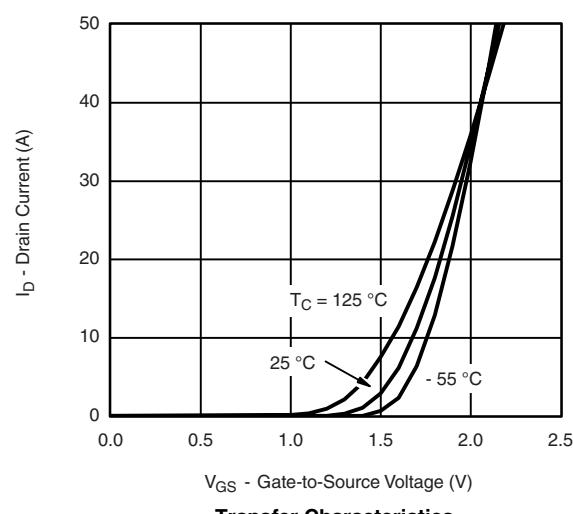
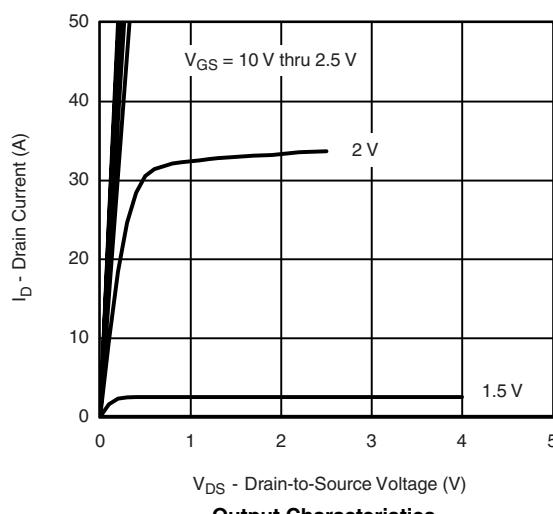
Notes:

a. Pulse test; pulse width $\leq 300 \mu\text{s}$, duty cycle $\leq 2\%$.

b. Guaranteed by design, not subject to production testing.

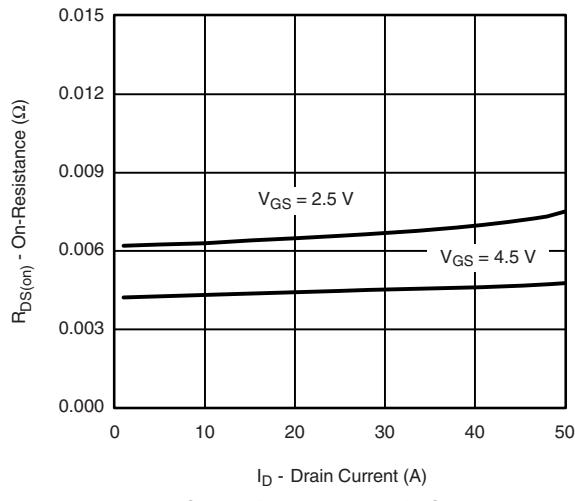
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS 25°C , unless otherwise noted

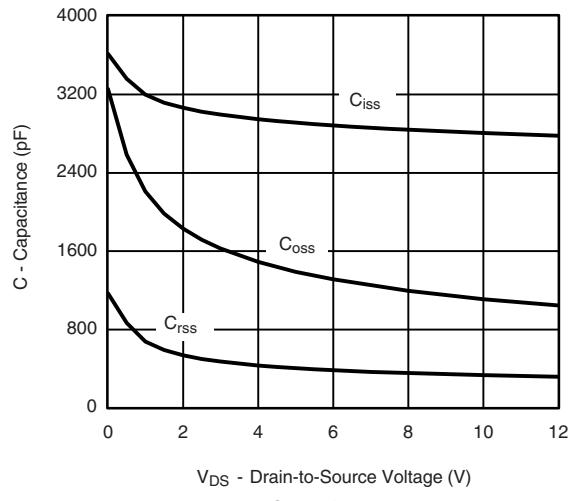




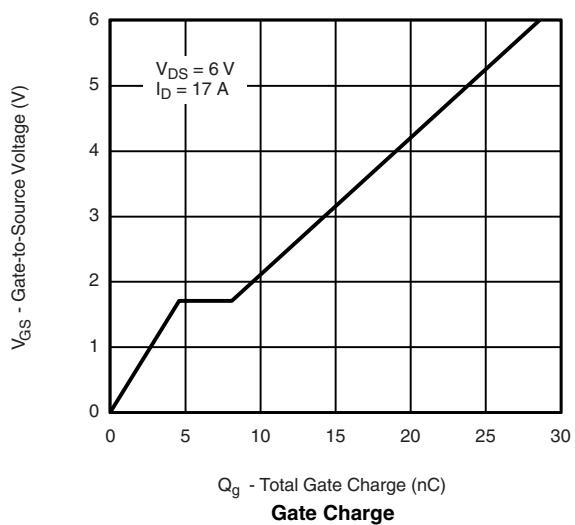
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



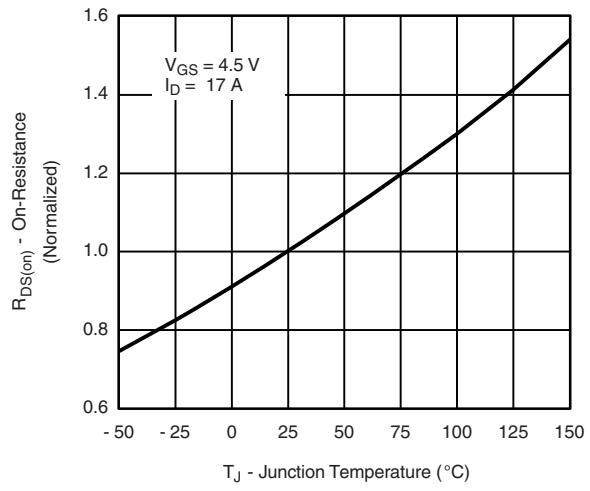
On-Resistance vs. Drain Current



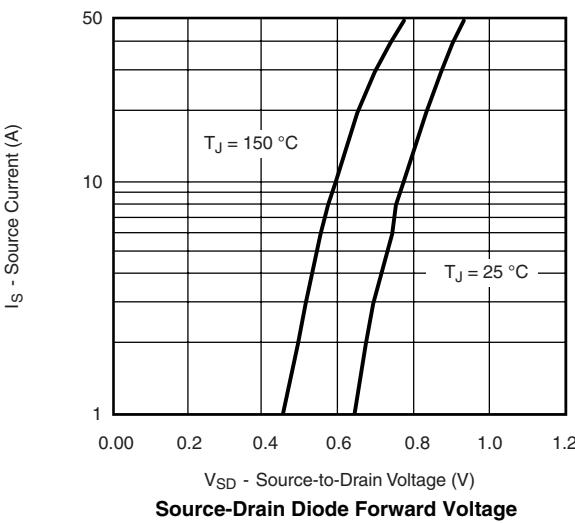
Capacitance



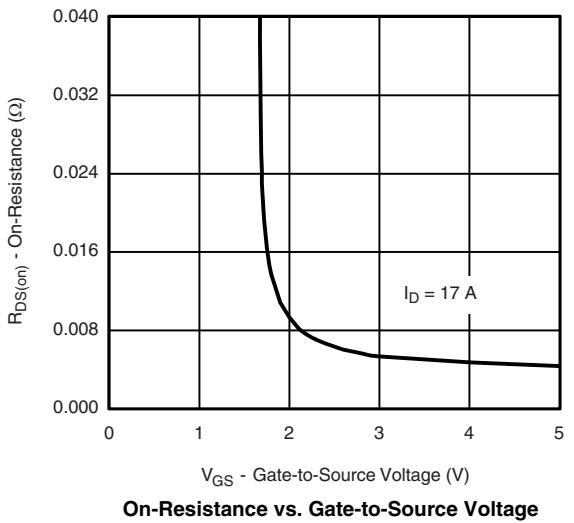
Gate Charge



On-Resistance vs. Junction Temperature



Source-Drain Diode Forward Voltage



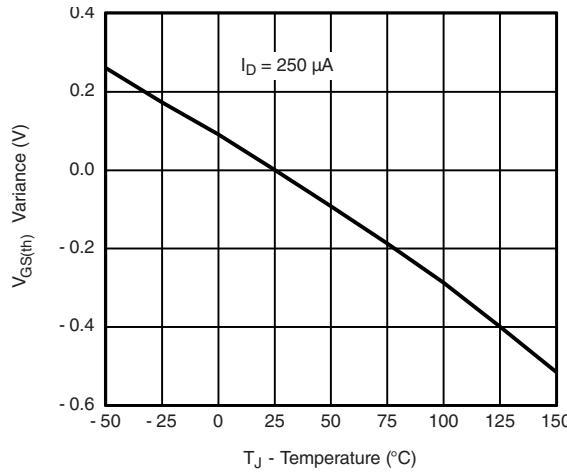
On-Resistance vs. Gate-to-Source Voltage

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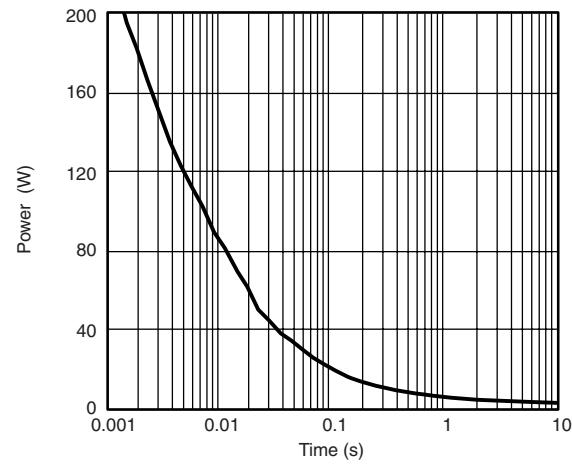
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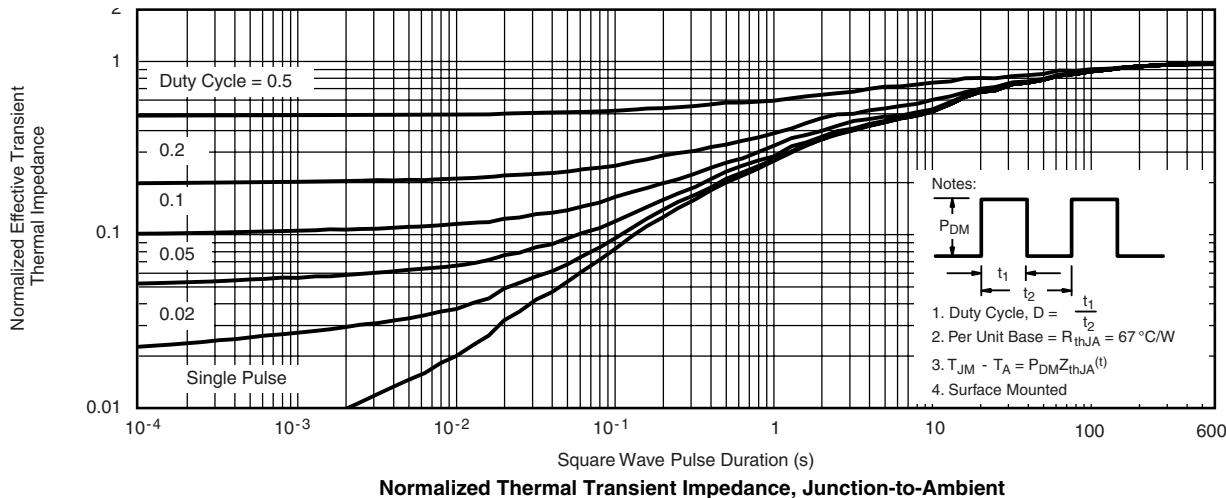
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



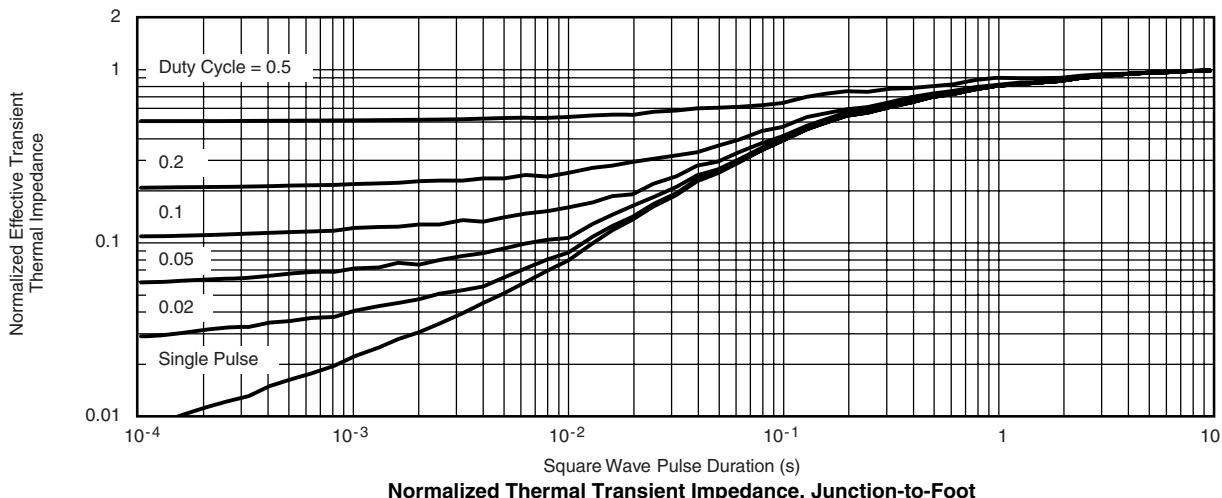
Threshold Voltage



Single Pulse Power



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Foot

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?71699.

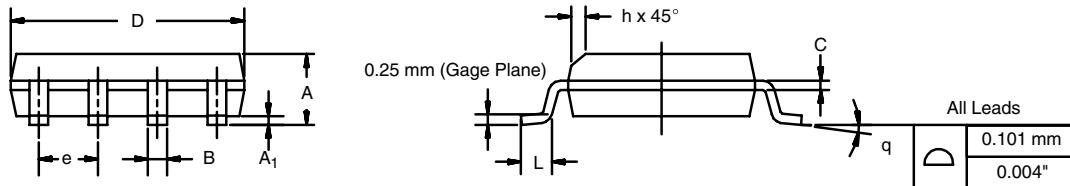
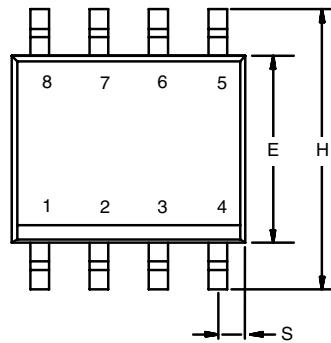


Package Information

Vishay Siliconix

SOIC (NARROW): 8-LEAD

JEDEC Part Number: MS-012



DIM	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A ₁	0.10	0.20	0.004	0.008
B	0.35	0.51	0.014	0.020
C	0.19	0.25	0.0075	0.010
D	4.80	5.00	0.189	0.196
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.020
L	0.50	0.93	0.020	0.037
q	0°	8°	0°	8°
S	0.44	0.64	0.018	0.026

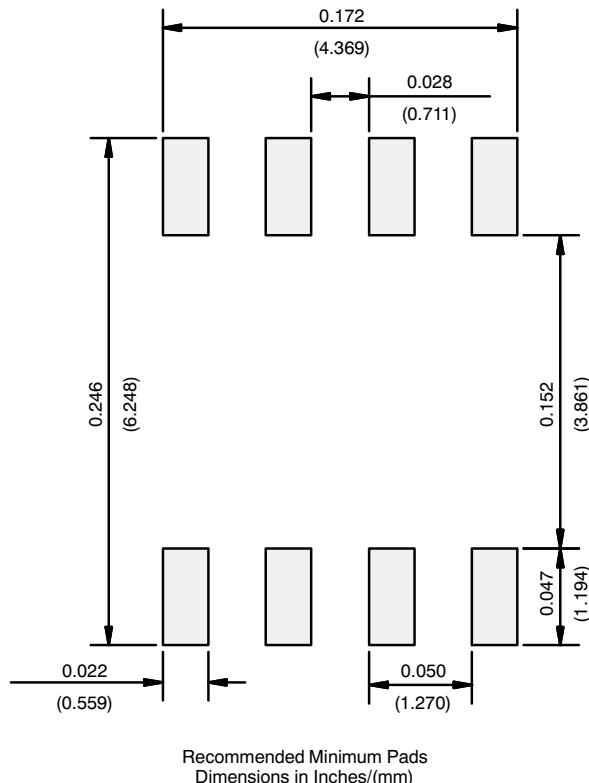
ECN: C-06527-Rev. I, 11-Sep-06
DWG: 5498

Application Note 826

Vishay Siliconix



RECOMMENDED MINIMUM PADS FOR SO-8



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