Excellent Integrated System Limited

Stocking Distributor

Click to view price, real time Inventory, Delivery & Lifecycle Information:

Vishay/Siliconix
SI6966EDQ-T1-E3

For any questions, you can email us directly:
sales@integrated-circuit.com

Distributor of Vishay/Siliconix: Excellent Integrated System Limited
Datasheet of SI6966EDQ-T1-E3 - MOSFET 2N-CH 20V 8TSSOP
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Dual N-Channel 2.5-V (G-S) MOSFET, ESD Protected

PRODUCT SUMMARY		
V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)
20	0.030 at V_{GS} = 4.5 V	± 5.2
	0.040 at V_{GS} = 2.5 V	± 4.5

FEATURES

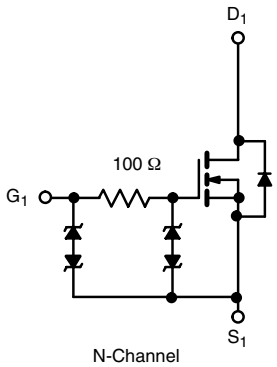
- **Halogen-free**
- ESD Protected: 4000 V

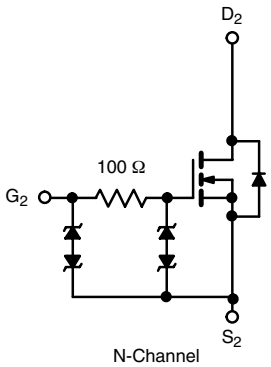
Pb-free
RoHS COMPLIANT

TSSOP-8

Top View

Ordering Information: Si6966EDG-T1-GE3 (Lead (Pb)-free and Halogen-free)





ABSOLUTE MAXIMUM RATINGS T_A = 25 °C, unless otherwise noted				
Parameter		**Symbol**	**Limit**	**Unit**
Drain-Source Voltage		V_{DS}	20	V
Gate-Source Voltage		V_{GS}	± 12	
Continuous Drain Current (T_J = 150 °C)[a, b]	T_A = 25 °C	I_D	± 5.2	A
	T_A = 70 °C		± 4.0	
Pulsed Drain Current		I_{DM}	± 30	
Continuous Source Current (Diode Conduction)[a, b]		I_S	1.25	
Maximum Power Dissipation[a, b]	T_A = 25 °C	P_D	1.25	W
	T_A = 70 °C		0.72	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 55 to 150	°C

THERMAL RESISTANCE RATINGS					
Parameter		**Symbol**	**Typical**	**Maximum**	**Unit**
Maximum Junction-to-Ambient[a]	t ≤ 10 s	R_{thJA}		110	°C/W
	Steady State		115		

Notes:
a. Surface Mounted on FR4 board.
b. t ≤ 10 s.

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SPECIFICATIONS T_J = 25 °C, unless otherwise noted						
Parameter	**Symbol**	**Test Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
Static						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	0.6			V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 4.5 V			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = + 20 V, V_{GS} = 0 V			1	µA
		V_{DS} = 20 V, V_{GS} = 0 V, T_J = 55 °C			25	
On-State Drain Current[a]	$I_{D(on)}$	V_{DS} ≥ 5 V, V_{GS} = 4.5 V	30			A
Drain-Source On-State Resistance[a]	$R_{DS(on)}$	V_{GS} = 4.5 V, I_D = 5.2 A		0.021	0.030	Ω
		V_{GS} = 2.5 V, I_D = 4.5 A		0.028	0.040	
Forward Transconductance[a]	g_{fs}	V_{DS} = 10 V, I_D = 5.2 A		20		S
Diode Forward Voltage[a]	V_{SD}	I_S = 1.25 A, V_{GS} = 0 V		0.65	1.2	V
Dynamic[b]						
Total Gate Charge	Q_g	V_{DS} = 15 V, V_{GS} = 4.5 V, I_D = 5.2 A		15	25	nC
Gate-Source Charge	Q_{gs}			2.5		
Gate-Drain Charge	Q_{gd}			4.5		
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 10 V, R_L = 10 Ω I_D ≅ 1 A, V_{GEN} = 4.5 V, R_G = 6 Ω		100	200	ns
Rise Time	t_r			130	250	
Turn-Off Delay Time	$t_{d(off)}$			420	800	
Fall Time	t_f			220	450	
Source-Drain Reverse Recovery Time	t_{rr}	I_F = 1.25 A, dI/dt = 100 A/µs		210	500	

Notes:
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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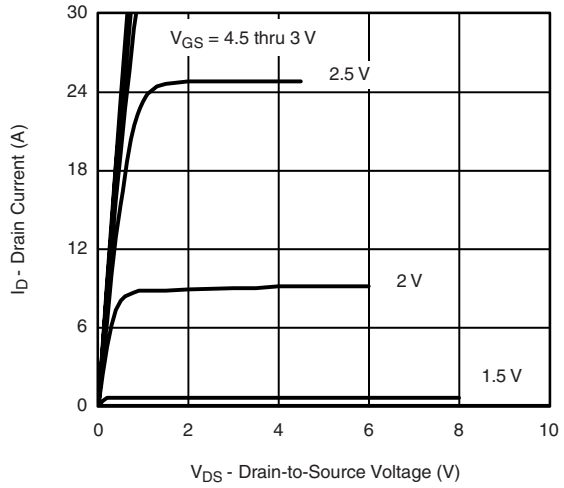
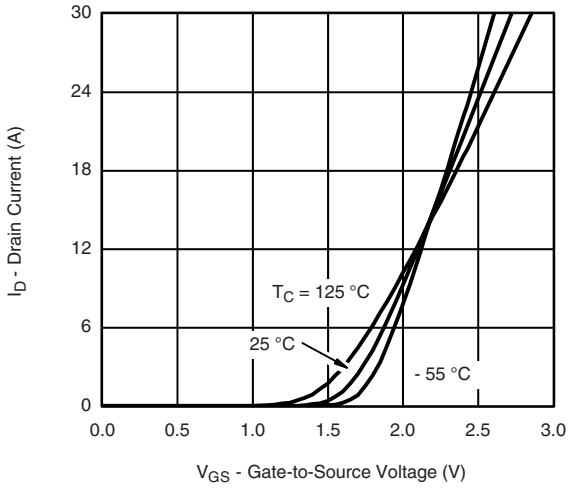
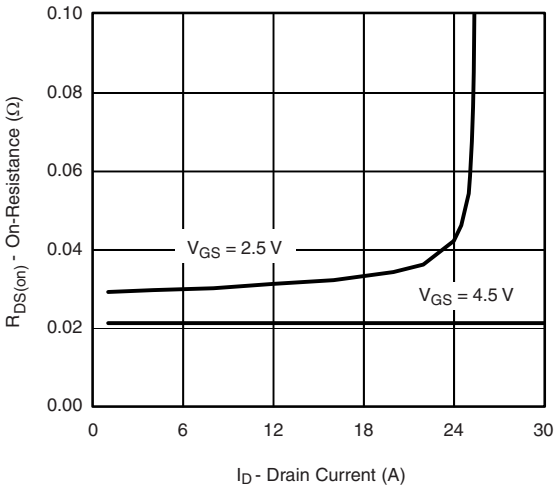
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



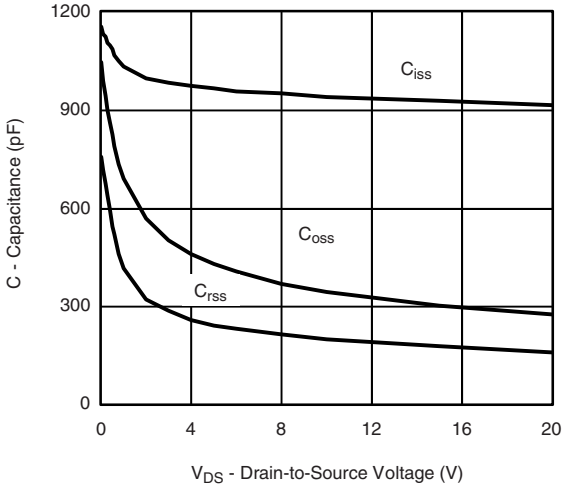
Output Characteristics



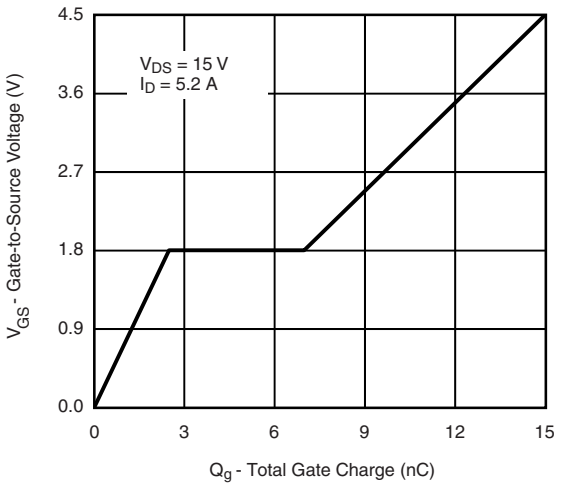
Transfer Characteristics



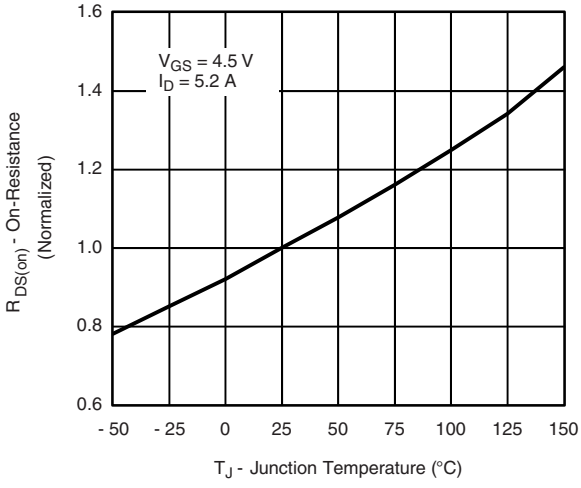
On-Resistance vs. Drain Current



Capacitance



Gate Charge



On-Resistance vs. Junction Temperature

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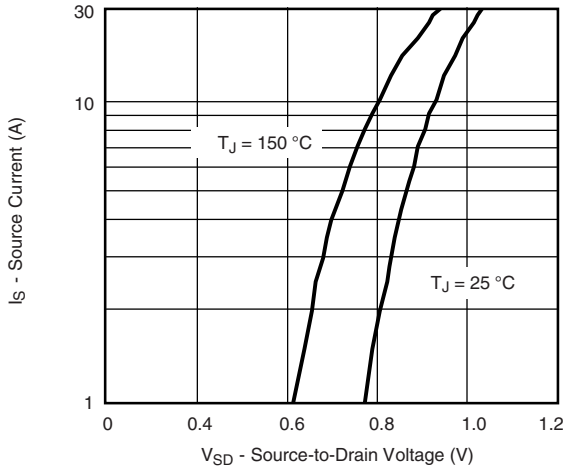
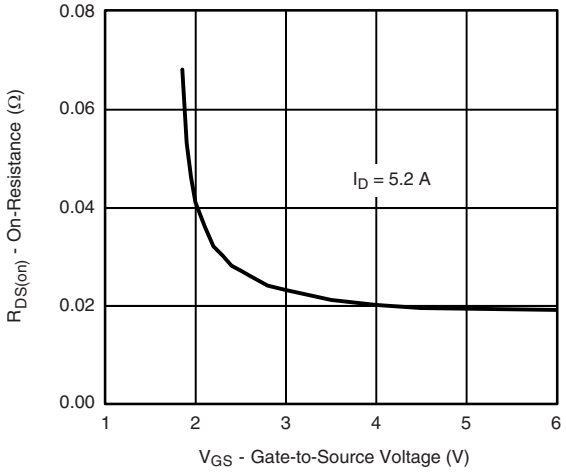
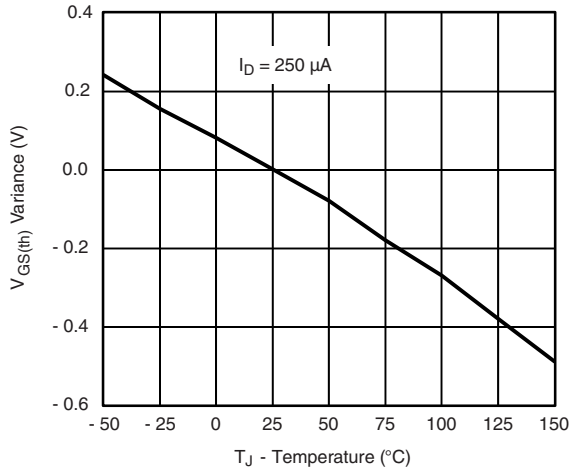


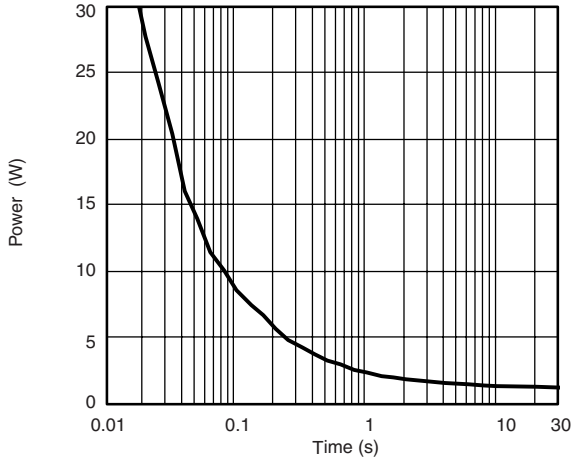
Source-Drain Diode Forward Voltage



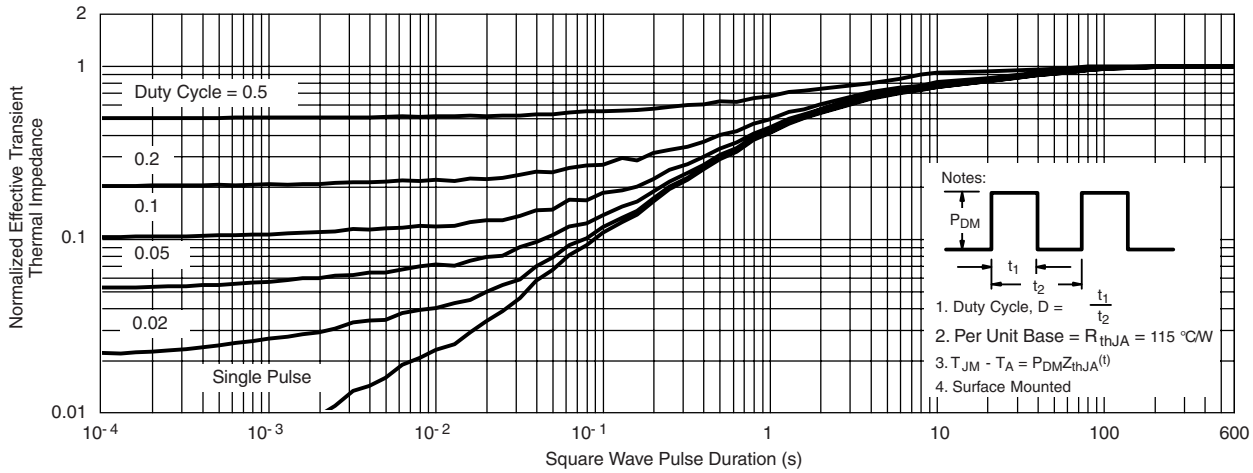
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



Single Pulse Power



Normalized Thermal Transient Impedance, Junction-to-Ambient

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