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[SI7342DP-T1-GE3](#)

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**Si7342DP**

Vishay Siliconix

## N-Channel 30 V (D-S) Fast Switching MOSFET

### PRODUCT SUMMARY

| V <sub>DS</sub> (V) | R <sub>DS(on)</sub> (Ω)            | I <sub>D</sub> (A) |
|---------------------|------------------------------------|--------------------|
| 30                  | 0.00825 at V <sub>GS</sub> = 10 V  | 15                 |
|                     | 0.00975 at V <sub>GS</sub> = 4.5 V | 13                 |

### FEATURES

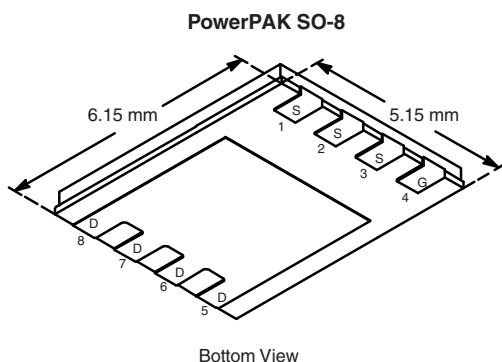
- Halogen-free According to IEC 61249-2-21 Definition
- Extremely Low Q<sub>gd</sub> for Low Switching Losses
- TrenchFET® Power MOSFET
- New Low Thermal Resistance PowerPAK® Package with Low 1.07 mm Profile
- 100 % R<sub>g</sub> Tested
- Compliant to RoHS Directive 2002/95/EC



**RoHS**  
COMPLIANT  
HALOGEN  
FREE  
Available

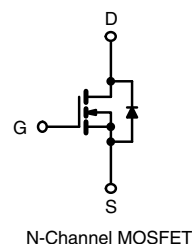
### APPLICATIONS

- High-Side DC/DC Conversion
  - Notebook
  - Server



Bottom View

**Ordering Information:** SI7342DP-T1-E3 (Lead (Pb)-free)  
SI7342DP-T1-GE3 (Lead (Pb)-free and Halogen-free)



N-Channel MOSFET

### ABSOLUTE MAXIMUM RATINGS (T<sub>A</sub> = 25 °C, unless otherwise noted)

| ABSOLUTE MAXIMUM RATINGS (T <sub>A</sub> = 25 °C, unless otherwise noted) |                        |                                   |             |              |      |
|---|------------------------|-----------------------------------|-------------|--------------|------|
| Parameter   |                        | Symbol                            | 10 s        | Steady State | Unit |
| Drain-Source Voltage  |                        | V <sub>DS</sub>                   | 30          |              | V    |
| Gate-Source Voltage   |                        | V <sub>GS</sub>                   | ± 12        |              |      |
| Continuous Drain Current (T <sub>J</sub> = 150 °C) <sup>a</sup>           | T <sub>A</sub> = 25 °C | I <sub>D</sub>                    | 15          | 9            | A    |
|   | T <sub>A</sub> = 70 °C |                                   | 12          | 7            |      |
| Pulsed Drain Current  |                        | I <sub>DM</sub>                   | ± 60        |              |      |
| Continuous Source Current (Diode Conduction) <sup>a</sup>                 |                        | I <sub>S</sub>                    | 4.1         | 1.5          |      |
| Maximum Power Dissipation <sup>a</sup>                                    | T <sub>A</sub> = 25 °C | P <sub>D</sub>                    | 5           | 1.8          | W    |
|   | T <sub>A</sub> = 70 °C |                                   | 3.2         | 1.1          |      |
| Operating Junction and Storage Temperature Range                          |                        | T <sub>J</sub> , T <sub>stg</sub> | - 55 to 150 |              | °C   |
| Soldering Recommendations (Peak Temperature) <sup>b, c</sup>              |                        |                                   | 260         |              |      |

### THERMAL RESISTANCE RATINGS

| Parameter   | Symbol            | Typical | Maximum | Unit |
|---|-------------------|---------|---------|------|
| Maximum Junction-to-Ambient (MOSFET) <sup>a</sup> | R <sub>thJA</sub> | 20      | 25      | °C/W |
|   |                   | 53      | 70      |      |
| Maximum Junction-to-Case (Drain)                  | R <sub>thJC</sub> | 2.1     | 3.2     |      |

Notes:

a. Surface mounted on 1" x 1" FR4 board.

b. See solder profile ([www.vishay.com/ppg?73257](http://www.vishay.com/ppg?73257)). The PowerPAK SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

c. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.

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| <b>MOSFETS SPECIFICATIONS</b> ( $T_J = 25\text{ }^{\circ}\text{C}$ , unless otherwise noted) |              |   |      |        |           |               |
|--|--------------|---|------|--------|-----------|---------------|
| Parameter  | Symbol       | Test Conditions   | Min. | Typ.   | Max.      | Unit          |
| <b>Static</b>  |              |   |      |        |           |               |
| Gate Threshold Voltage   | $V_{GS(th)}$ | $V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$  | 0.6  |        | 1.8       | V             |
| Gate-Body Leakage  | $I_{GSS}$    | $V_{DS} = 0\text{ V}$ , $V_{GS} = \pm 12\text{ V}$  |      |        | $\pm 100$ | nA            |
| Zero Gate Voltage Drain Current  | $I_{DSS}$    | $V_{DS} = 30\text{ V}$ , $V_{GS} = 0\text{ V}$  |      |        | 1         | $\mu\text{A}$ |
|  |              | $V_{DS} = 30\text{ V}$ , $V_{GS} = 0\text{ V}$ , $T_J = 70\text{ }^{\circ}\text{C}$   |      |        | 10        |               |
| On-State Drain Current <sup>a</sup>  | $I_{D(on)}$  | $V_{DS} \geq 5\text{ V}$ , $V_{GS} = 10\text{ V}$   | 40   |        |           | A             |
| Drain-Source On-State Resistance <sup>a</sup>  | $R_{DS(on)}$ | $V_{GS} = 10\text{ V}$ , $I_D = 15\text{ A}$  |      | 0.0066 | 0.00825   | $\Omega$      |
|  |              | $V_{GS} = 4.5\text{ V}$ , $I_D = 13\text{ A}$   |      | 0.0077 | 0.00975   |               |
| Forward Transconductance <sup>a</sup>  | $g_{fs}$     | $V_{DS} = 15\text{ V}$ , $I_D = 15\text{ A}$  |      | 65     |           | S             |
| Diode Forward Voltage <sup>a</sup>   | $V_{SD}$     | $I_S = 2.9\text{ A}$ , $V_{GS} = 0\text{ V}$  |      | 0.73   | 1.1       | V             |
| <b>Dynamic<sup>b</sup></b>   |              |   |      |        |           |               |
| Input Capacitance  | $C_{iss}$    | $V_{DS} = 15\text{ V}$ , $V_{GS} = 0\text{ V}$ , $f = 1\text{ MHz}$   |      | 1900   |           | pF            |
| Output Capacitance   | $C_{oss}$    |   |      | 530    |           |               |
| Reverse Transfer Capacitance   | $C_{rss}$    |   |      | 120    |           |               |
| Total Gate Charge  | $Q_g$        | $V_{DS} = 15\text{ V}$ , $V_{GS} = 4.5\text{ V}$ , $I_D = 15\text{ A}$  |      | 12.5   | 19        | nC            |
| Gate-Source Charge   | $Q_{gs}$     |   |      | 3.9    |           |               |
| Gate-Drain Charge  | $Q_{gd}$     |   |      | 2.1    |           |               |
| Gate Resistance  | $R_g$        |   | 0.8  | 1.2    | 1.8       | $\Omega$      |
| Turn-On Delay Time   | $t_{d(on)}$  | $V_{DD} = 15\text{ V}$ , $R_L = 15\text{ }\Omega$<br>$I_D \cong 1\text{ A}$ , $V_{GEN} = 10\text{ V}$ , $R_G = 6\text{ }\Omega$ |      | 13     | 20        | ns            |
| Rise Time  | $t_r$        |   |      | 8      | 13        |               |
| Turn-Off Delay Time  | $t_{d(off)}$ |   |      | 48     | 75        |               |
| Fall Time  | $t_f$        |   |      | 13     | 20        |               |
| Source-Drain Reverse Recovery Time   | $t_{rr}$     | $I_F = 2.9\text{ A}$ , $dI/dt = 100\text{ A}/\mu\text{s}$   |      | 36     | 55        |               |

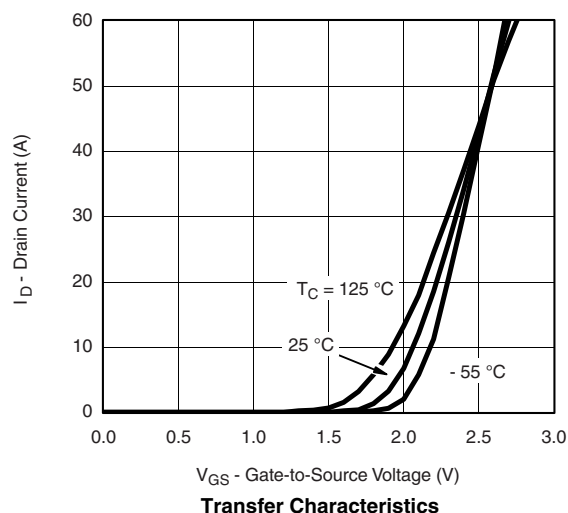
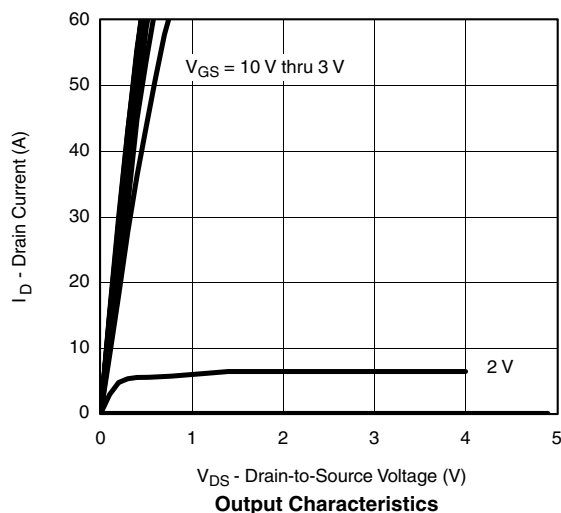
Notes:

a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .

b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

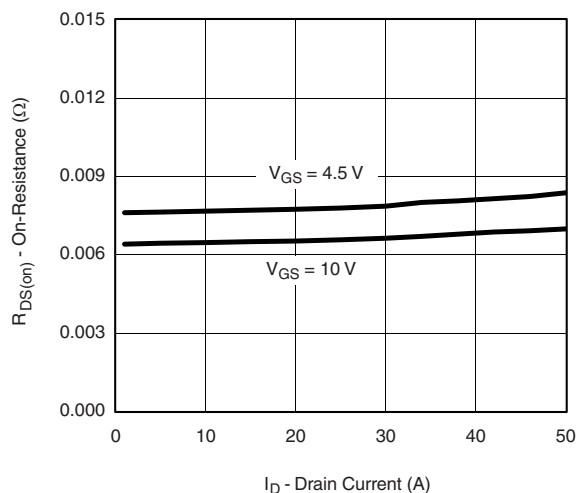




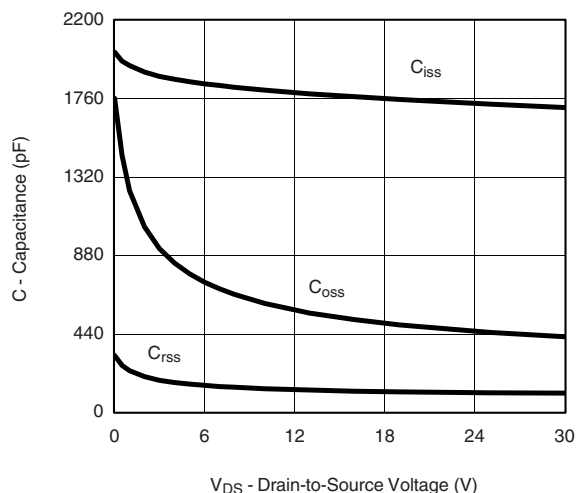
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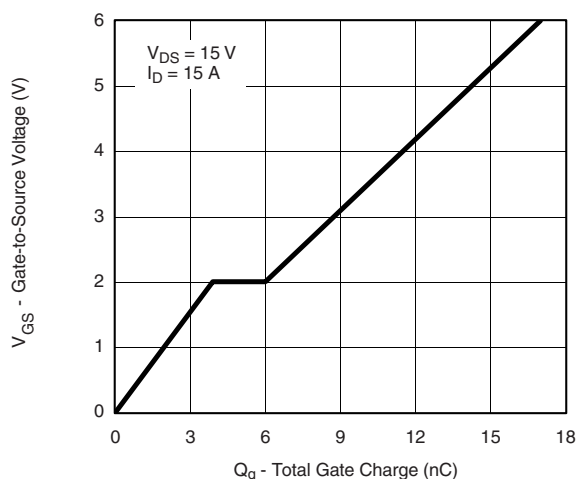
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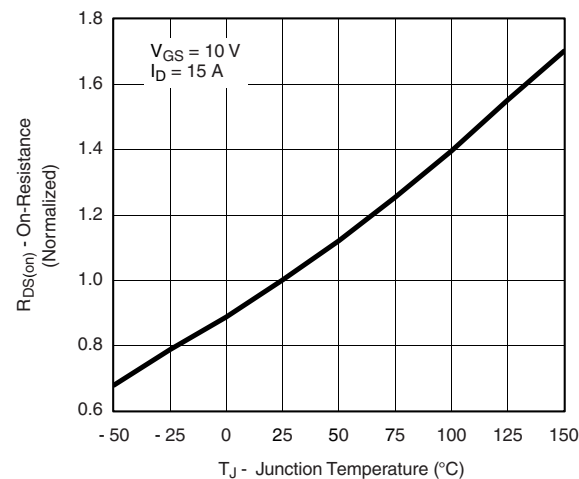
On-Resistance vs. Drain Current



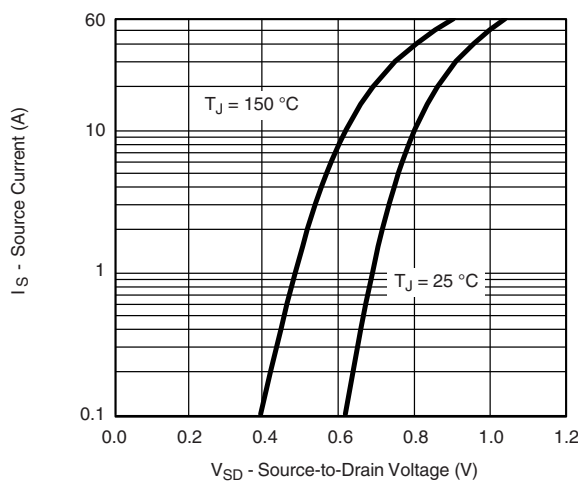
Capacitance



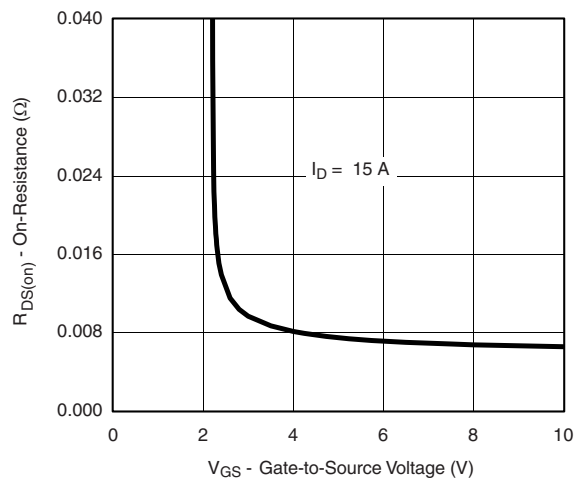
Gate Charge



On-Resistance vs. Junction Temperature



Source-Drain Diode Forward Voltage



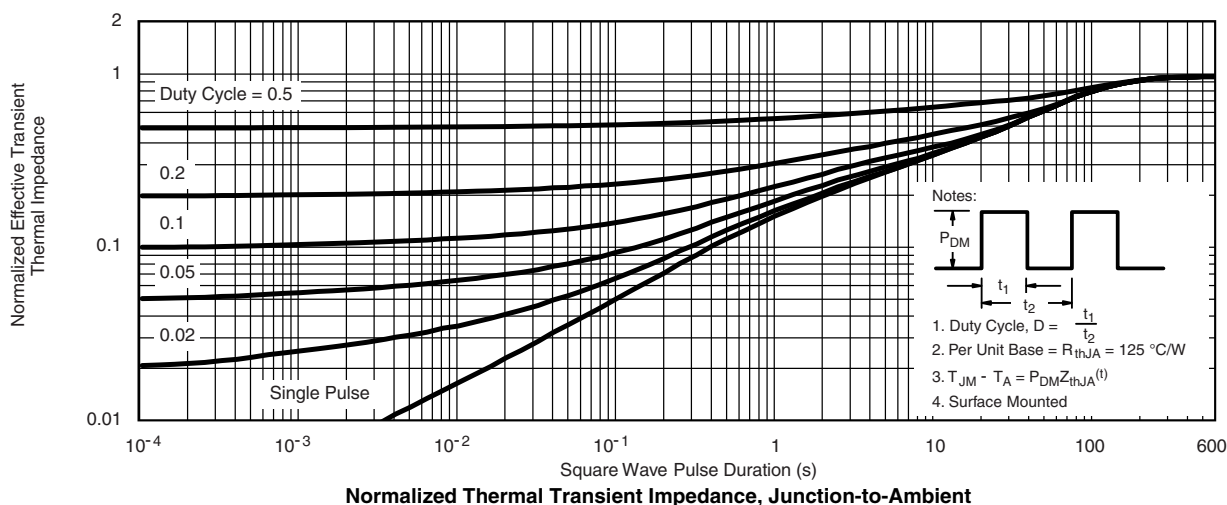
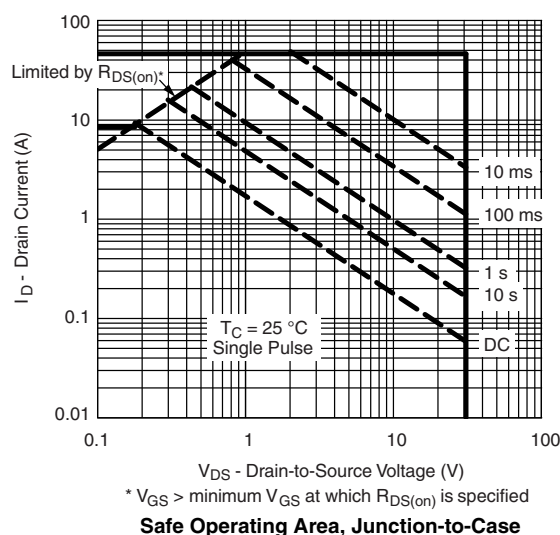
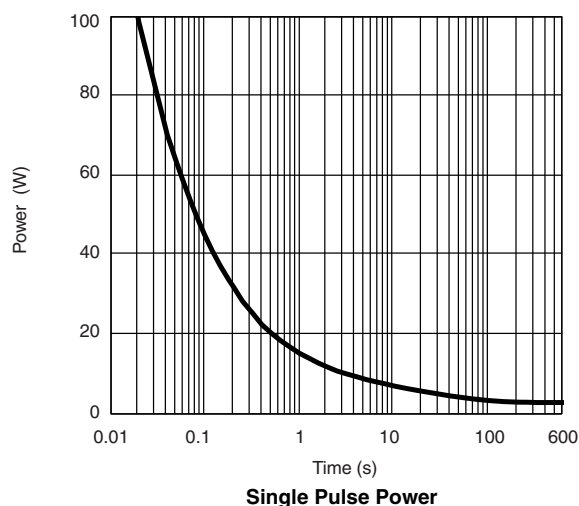
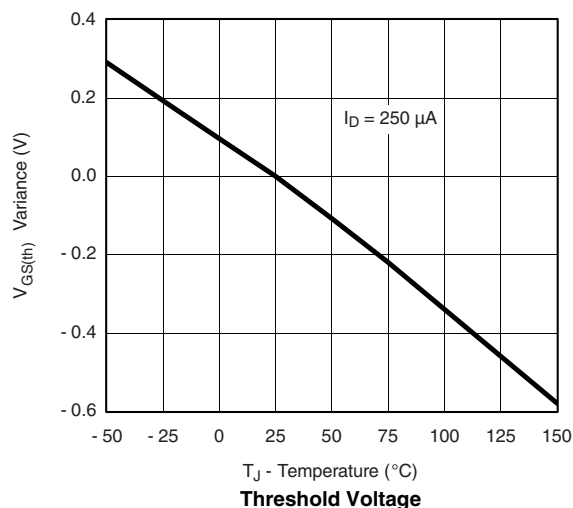
On-Resistance vs. Gate-to-Source Voltage

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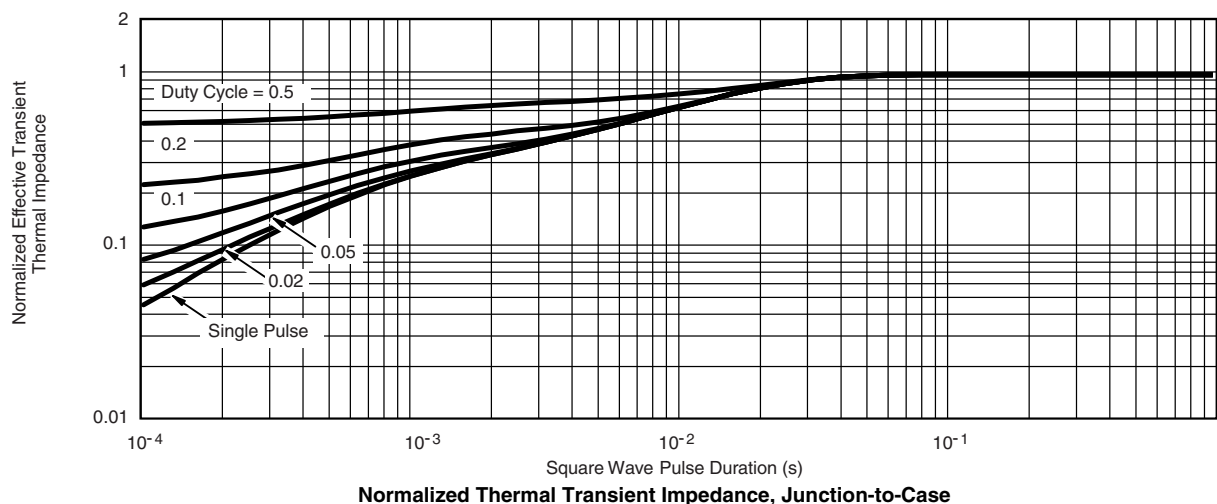




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Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see [www.vishay.com/ppg?72751](http://www.vishay.com/ppg?72751).



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