

Excellent Integrated System Limited

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Vishay/Siliconix SI7445DP-T1-E3

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Si7445DP

Vishay Siliconix

P-Channel 20-V (D-S) MOSFET

PRODUCT SUMMARY					
V _{DS} (V)	$R_{DS(on)}(\Omega)$	I _D (A)			
- 20	0.0077 at $V_{GS} = -4.5 \text{ V}$	- 19			
	0.0094 at V _{GS} = - 2.5 V	- 17			
	0.0125 at V _{GS} = - 1.8 V	- 15			

•	Halogen-free	According to	IEC	61249-2-21
	Available			

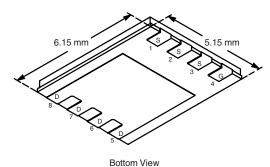
- TrenchFET[®] Power MOSFET
- New Low Thermal Resistance PowerPAK[®] Package with Low 1.07 mm Profile
- 100 % R_q Tested

FEATURES





PowerPAK SO-8

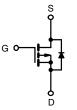


Ordering Information: Si7445DP-T1-E3 (Lead (Pb)-free)

Si7445DP-T1-GE3 (Lead (Pb)-free and Halogen-free)

APPLICATIONS

· Load Switch Battery Applications



P-Channel MOSFET

Parameter		Symbol	10 s	Steady State	Unit
Drain-Source Voltage		V_{DS}	- 20		V
Gate-Source Voltage		V_{GS}	± 8		V
Continuous Drain Current (T _{.I} = 150°C) ^a	T _A = 25°C	I _D	- 19	- 12	А
Continuous Diani Curient (1 j = 150 C)	T _A = 70°C		- 15	- 9	
Pulsed Drain Current		I _{DM}	- 50		A
Continuous Source Current (Diode Conduction) ^a		I _S	- 4.3 - 1.6		
Maniana Barra Biratian	T _A = 25°C	P _D	5.4	1.9	W
Maximum Power Dissipation ^a	T _A = 70°C		3.4	1.2	VV
Operating Junction and Storage Temperature Range		T _J , T _{stg}	- 55 to 150		°C
Soldering Recommendations (Peak Temperature)b, c			260		.0

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Marrian Installanta Amelianta	t ≤ 10 s	R _{thJA}	18	23	°C/W
Maximum Junction-to-Ambient ^a	Steady State		52	65	
Maximum Junction-to-Case (Drain)	Steady State	R_{thJC}	1.0	1.3	

Notes

- a. Surface Mounted on 1" x 1" FR4 board.
- b. See Solder Profile (<u>www.vishay.com/ppg?73257</u>). The PowerPAK SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- c. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

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Distributor of Vishay/Siliconix: Excellent Integrated System Limited

Datasheet of SI7445DP-T1-E3 - MOSFET P-CH 20V 12A PPAK 1212-8

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Si7445DP

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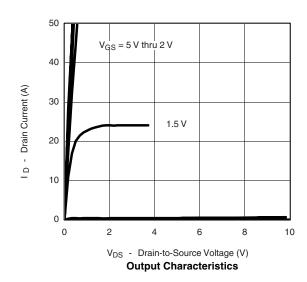


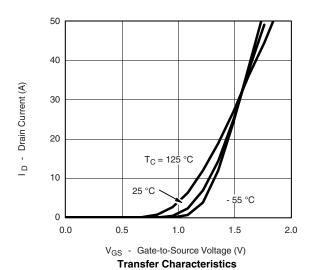
Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static							
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = -250 \mu A$	- 0.45		- 1.0	٧	
Gate-Body Leakage	I _{GSS}	$V_{DS} = 0 \text{ V, } V_{GS} = \pm 8 \text{ V} $ ± 100 $V_{DS} = -20 \text{ V, } V_{GS} = 0 \text{ V} $ -1 $V_{DS} = -20 \text{ V, } V_{GS} = 0 \text{ V, } T_{J} = 70 \text{ °C} $ -10 $V_{DS} \le -5 \text{ V, } V_{GS} = -4.5 \text{ V} $ -40 $V_{GS} = -4.5 \text{ V, } I_{D} = -19 \text{ A} $ $0.0064 $ 0.0073 $V_{GS} = -2.5 \text{ V, } I_{D} = -17 \text{ A} $ $0.0078 $ 0.0094					
Zava Cata Valtaga Duain Cumant	I _{DSS}	V _{DS} = - 20 V, V _{GS} = 0 V			- 1	μΑ	
Zero Gate Voltage Drain Current		$V_{DS} = -20 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 70 ^{\circ}\text{C}$			- 10		
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \le -5 \text{ V}, V_{GS} = -4.5 \text{ V}$	- 40			Α	
	R _{DS(on)}	V _{GS} = - 4.5 V, I _D = - 19 A		0.0064	0.0077		
Drain-Source On-State Resistance ^a		$V_{GS} = -2.5 \text{ V}, I_D = -17 \text{ A}$		0.0078	0.0094	Ω	
		$V_{GS} = -1.8 \text{ V}, I_D = -10 \text{ A}$		0.0105	0.0125		
Forward Transconductance ^a	9 _{fs}	V _{DS} = - 15 V, I _D = - 19 A		75		S	
Diode Forward Voltage ^a	V_{SD}	$I_S = -4.3 \text{ A}, V_{GS} = 0 \text{ V}$ - 0.65		- 1.1	V		
Dynamic ^b			•	•			
Total Gate Charge	Q_g			92	140		
Gate-Source Charge	Q_{gs}	$V_{DS} = -15 \text{ V}, V_{GS} = -5 \text{ V}, I_{D} = -19 \text{ A}$		19		nC	
Gate-Drain Charge	Q_{gd}			16.5			
Gate Resistance	R_g		1	2	3.4	Ω	
Turn-On Delay Time	t _{d(on)}			40	60		
Rise Time	t _r	t_r $V_{DD} = -15 \text{ V}, R_L = 15 \Omega$		45	65		
Turn-Off Delay Time	t _{d(off)}	$I_D\cong$ - 1.0 A, V_{GEN} = - 4.5 V, R_g = 6 Ω		400	600	ns	
Fall Time	t _f			190	290		
Source-Drain Reverse Recovery Time	t _{rr}	I _F = - 4.3 A, dI/dt = 100 A/μs		50	80		

Notes:

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted





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a. Pulse test; pulse width \leq 300 μ s, duty cycle \leq 2 %.

b. Guaranteed by design, not subject to production testing.

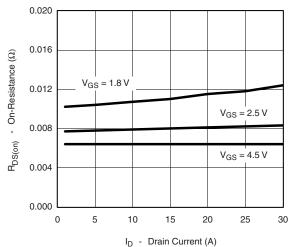




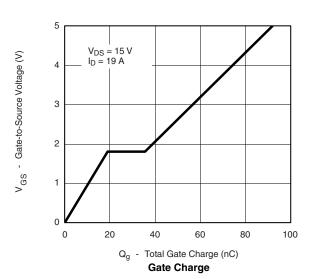
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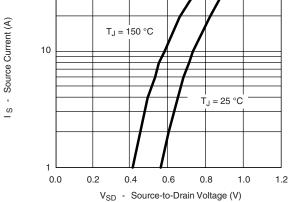
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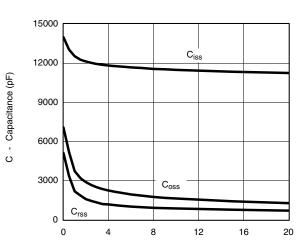


On-Resistance vs. Drain Current

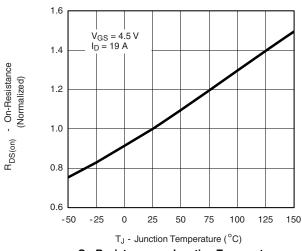




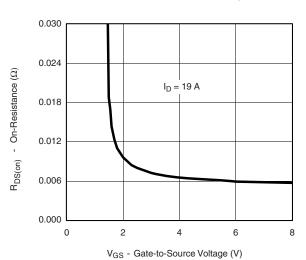
Source-Drain Diode Forward Voltage



V_{DS} - Drain-to-Source Voltage (V) **Capacitance**



On-Resistance vs. Junction Temperature



On-Resistance vs. Gate-to-Source Voltage

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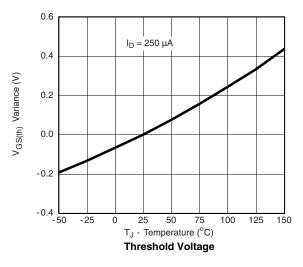


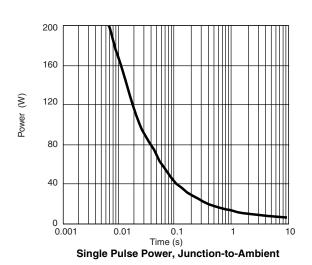
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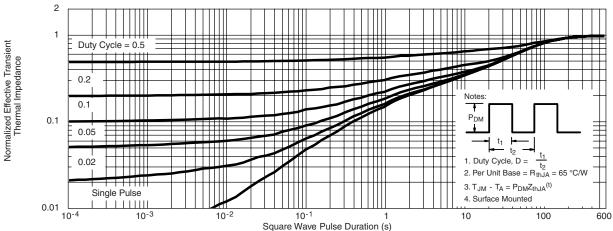
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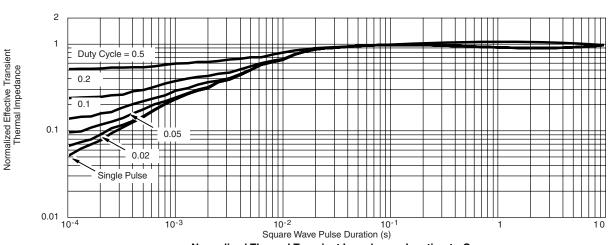
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TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted









Normalized Thermal Transient Impedance, Junction-to-Case

Normalized Thermal Transient Impedance, Junction-to-Ambient

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, seem www.vishay.com/ppg?71626.



Distributor of Vishay/Siliconix: Excellent Integrated System Limited Datasheet of SI7445DP-T1-E3 - MOSFET P-CH 20V 12A PPAK 1212-8

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