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[Vishay/Siliconix](#)
[SI7447ADP-T1-E3](#)

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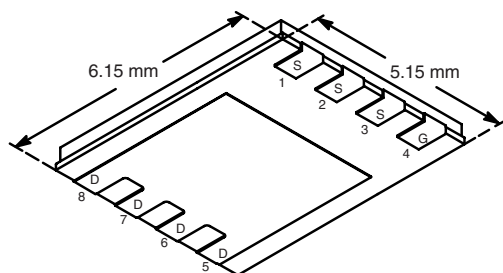


Si7447ADP
 Vishay Siliconix

P-Channel 30-V (D-S) MOSFET

PRODUCT SUMMARY			
V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A) ^a	Q _g (Typ.)
- 30	0.0065 at V _{GS} = - 10 V	- 35	100 nC

PowerPAK SO-8



Bottom View

Ordering Information: SI7447ADP-T1-E3 (Lead (Pb)-free)
 SI7447ADP-T1-GE3 (Lead (Pb)-free and Halogen-free)

FEATURES

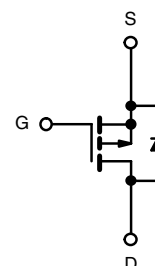
- Halogen-free According to IEC 61249-2-21 Available
- TrenchFET[®] Power MOSFET
- New Low Thermal Resistance PowerPAK[®] Package with Low 1.07 mm Profile
- 100 % R_g Tested



RoHS
 COMPLIANT
 HALOGEN
FREE
 Available

APPLICATIONS

- Battery and Load Switching
- Notebook Computers
- Notebook Battery Packs



P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS T _A = 25 °C, unless otherwise noted			
Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V _{DS}	- 30	V
Gate-Source Voltage	V _{GS}	± 25	
Continuous Drain Current (T _J = 150 °C)	I _D	T _C = 25 °C	- 35
		T _C = 70 °C	- 28
		T _A = 25 °C	- 21.5 ^{b, c}
		T _A = 70 °C	- 17 ^{b, c}
Pulsed Drain Current	I _{DM}	- 60	A
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C	
		T _A = 25 °C	- 4.3 ^{b, c}
Single Pulse Avalanche Current	I _{AS}	40	mJ
Avalanche Energy	E _{AS}	80	
Maximum Power Dissipation	P _D	T _C = 25 °C	83.3
		T _C = 70 °C	53.3
		T _A = 25 °C	5.4 ^{b, c}
		T _A = 70 °C	3.4 ^{b, c}
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to 150	°C
Soldering Recommendations (Peak Temperature) ^{d, e}		260	

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{b, f}	t ≤ 10 s	R _{thJA}	18	23	°C/W
Maximum Junction-to-Case (Drain)	Steady State	R _{thJC}	1.0	1.3	

Notes:

- Based on T_C = 25 °C.
- Surface Mounted on 1" x 1" FR4 board.
- t = 10 s.
- See Solder Profile (www.vishay.com/doc?73257). The PowerPAK SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.
- Maximum under Steady State conditions is 65 °C/W.

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SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = -250\text{ }\mu\text{A}$	-30			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = -250\text{ }\mu\text{A}$		-33		mV/ $^\circ\text{C}$
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$		5.3			
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$	-1	-2.0	-3	V
Gate-Source Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 25\text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -30\text{ V}, V_{GS} = 0\text{ V}$			-1	μA
		$V_{DS} = -30\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$			-10	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq -5\text{ V}, V_{GS} = -10\text{ V}$	-30			A
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = -10\text{ V}, I_D = -24\text{ A}$		0.0054	0.0065	Ω
Forward Transconductance ^a	g_{fs}	$V_{DS} = -15\text{ V}, I_D = -24\text{ A}$		50		S
Dynamic^b						
Input Capacitance	C_{iss}	$V_{DS} = -15\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		4650		μF
Output Capacitance	C_{oss}		1200			
Reverse Transfer Capacitance	C_{rss}		930			
Total Gate Charge	Q_g	$V_{DS} = -15\text{ V}, V_{GS} = -10\text{ V}, I_D = -24\text{ A}$		100	150	nC
Gate-Source Charge	Q_{gs}		15.5			
Gate-Drain Charge	Q_{gd}		25			
Gate Resistance	R_g	$f = 1\text{ MHz}$	1.7	3.5	5.3	Ω
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -15\text{ V}, R_L = 1.5\text{ }\Omega$ $I_D \cong -10\text{ A}, V_{GEN} = -10\text{ V}, R_g = 1\text{ }\Omega$		20	30	ns
Rise Time	t_r		25	40		
Turn-Off Delay Time	$t_{d(off)}$		82	125		
Fall Time	t_f		98	150		
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	$T_C = 25\text{ }^\circ\text{C}$			-28	A
Pulse Diode Forward Current ^a	I_{SM}				-60	
Body Diode Voltage	V_{SD}	$I_S = -4.3\text{ A}$		-0.72	-1.1	V
Body Diode Reverse Recovery Time	t_{rr}	$I_F = -19\text{ A}, di/dt = -100\text{ A}/\mu\text{s}, T_J = 25\text{ }^\circ\text{C}$		47	70	ns
Body Diode Reverse Recovery Charge	Q_{rr}		50	75	nC	
Reverse Recovery Fall Time	t_a		22		ns	
Reverse Recovery Rise Time	t_b		25			

Notes:

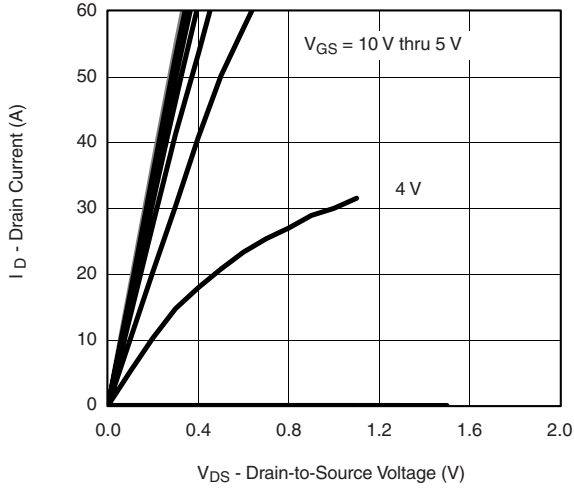
- Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
- Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

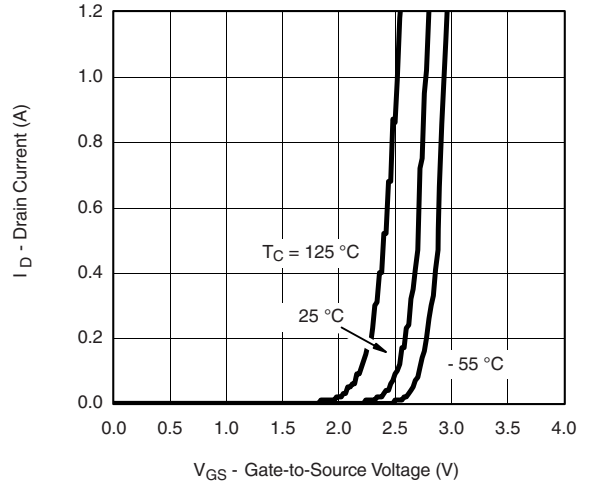


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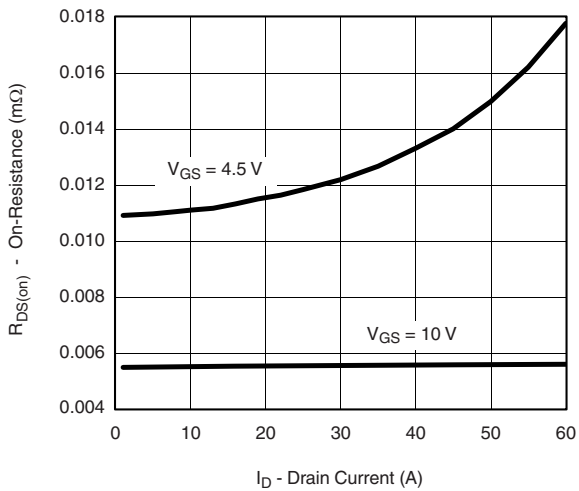
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



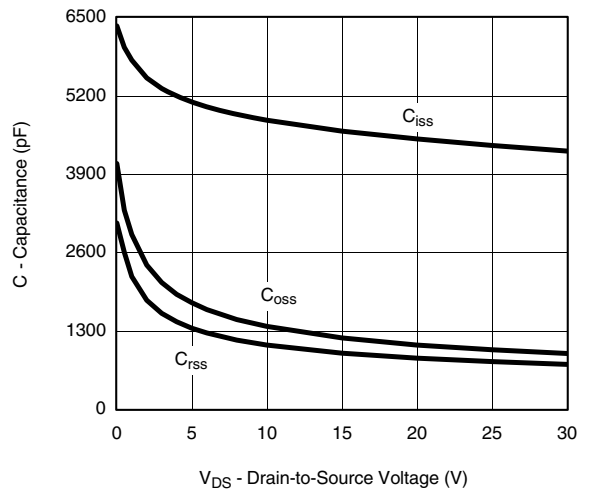
Output Characteristics



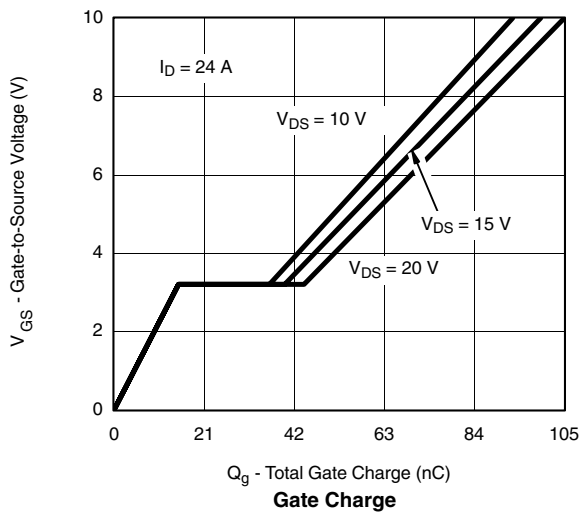
Transfer Characteristics



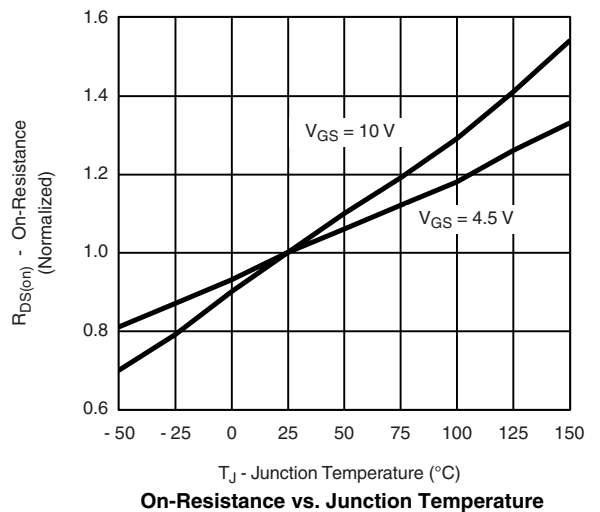
On-Resistance vs. Drain Current and Gate Voltage



Capacitance



Gate Charge

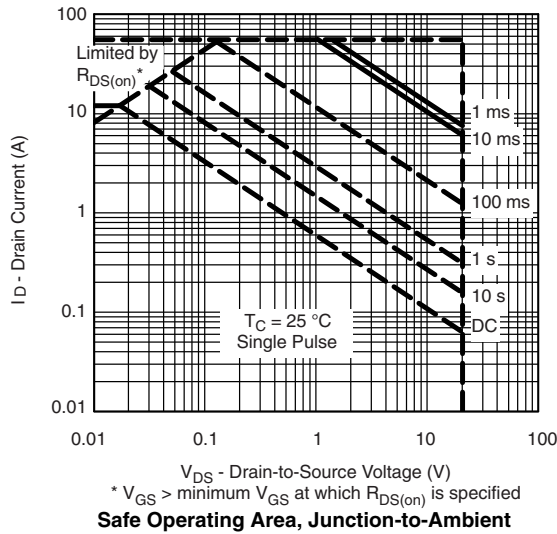
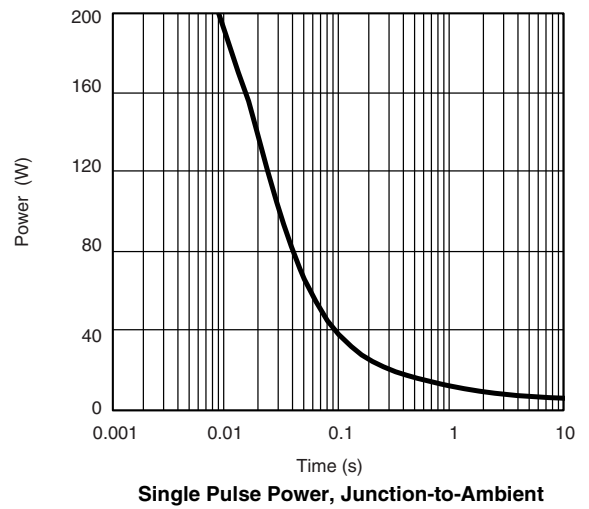
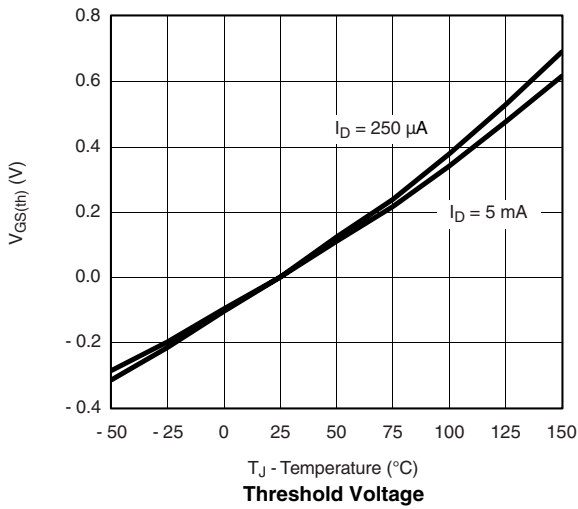
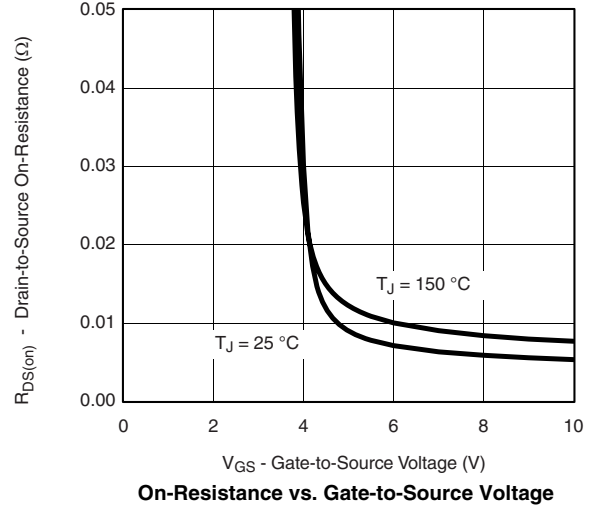
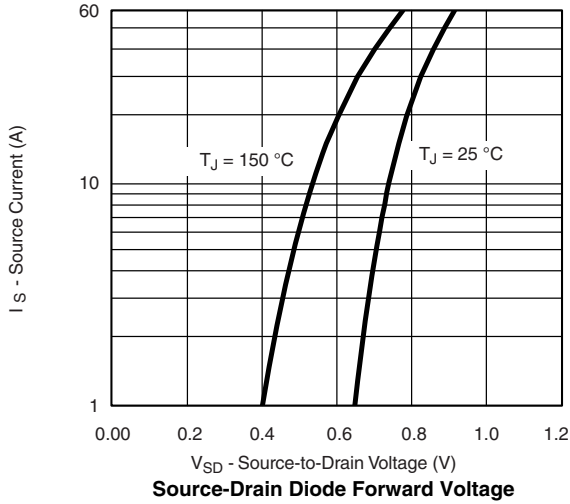


On-Resistance vs. Junction Temperature

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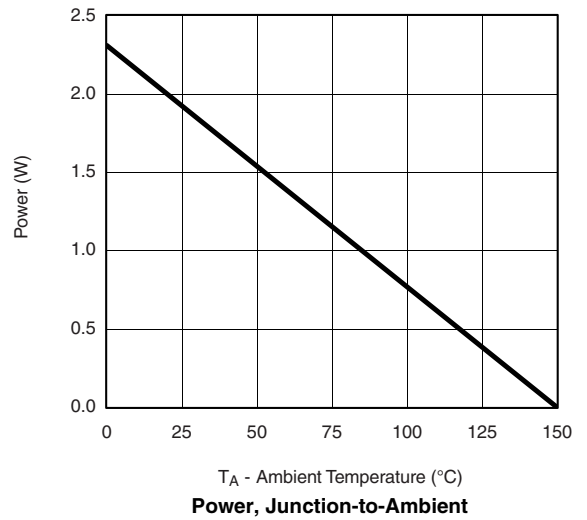
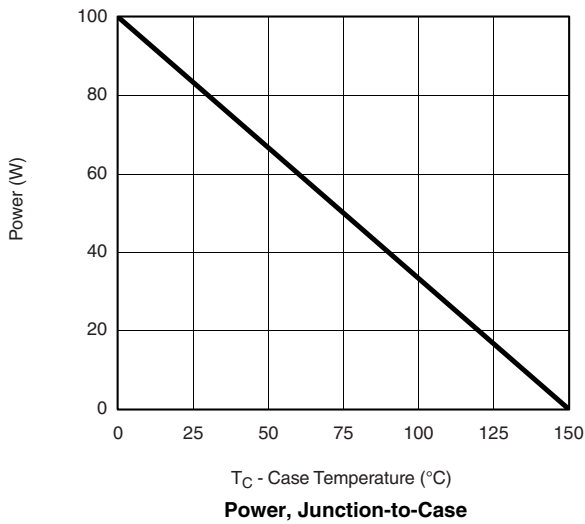
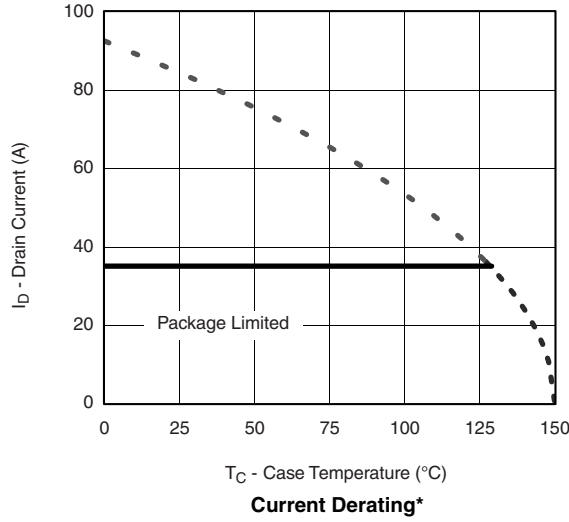
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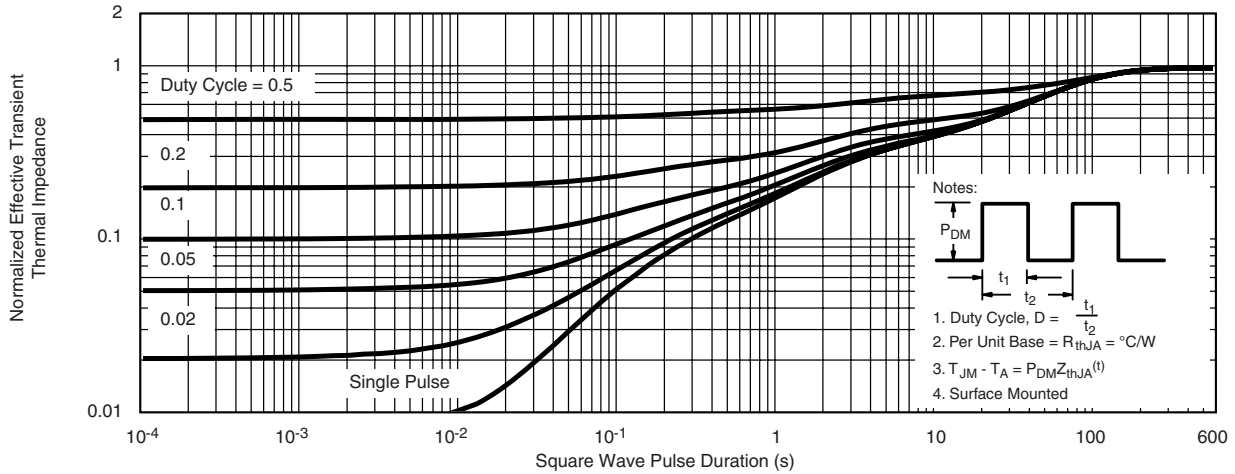


* The power dissipation P_D is based on T_{J(max)} = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

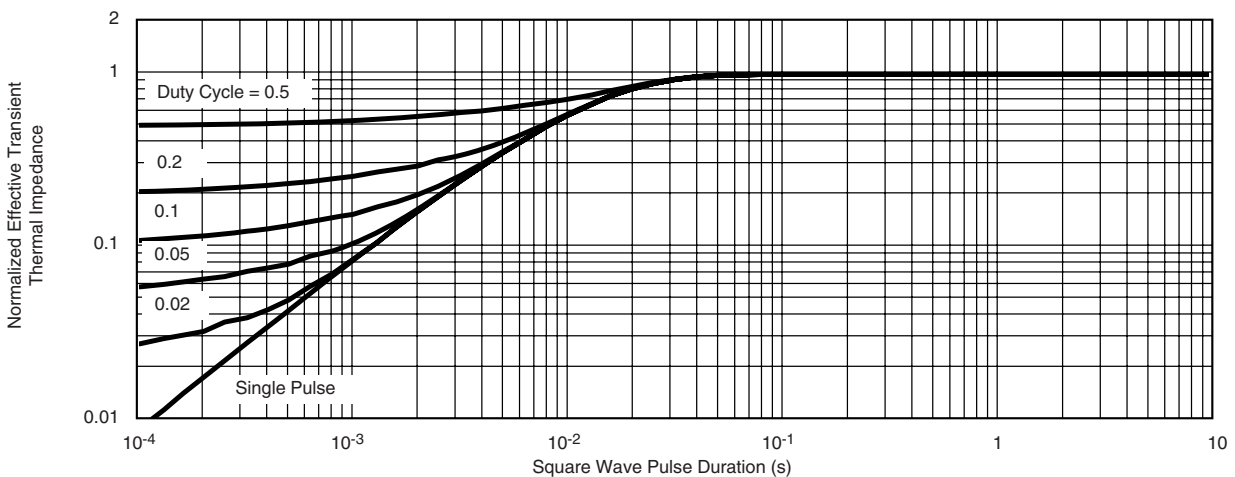
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TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

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