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[SI7901EDN-T1-E3](#)

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Si7901EDN
Vishay Siliconix

Dual P-Channel 20-V (D-S) MOSFET

PRODUCT SUMMARY

V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)
- 20	0.048 at $V_{GS} = - 4.5$ V	- 6.3
	0.068 at $V_{GS} = - 2.5$ V	- 5.3
	0.090 at $V_{GS} = - 1.8$ V	- 4.6

FEATURES

- Halogen-free According to IEC 61249-2-21 Available
- TrenchFET® Power MOSFETS: 1.8 V Rated
- ESD Protected: 4500 V
- Ultra Low Thermal Resistance PowerPAK® Package with Low 1.07 mm Profile

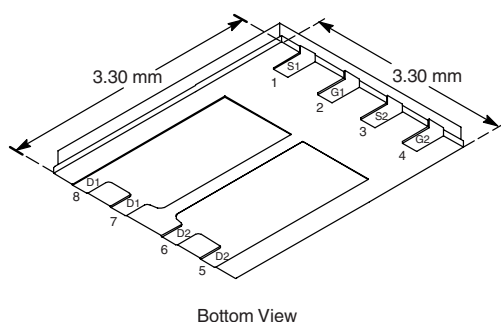


RoHS
COMPLIANT
HALOGEN
FREE
Available

APPLICATIONS

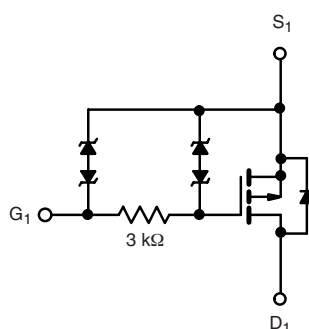
- Bidirectional Switch

PowerPAK 1212-8

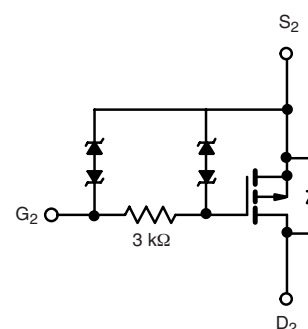


Bottom View

Ordering Information: Si7901EDN-T1-E3 (Lead (Pb)-free)
Si7901EDN-T1-GE3 (Lead (Pb)-free and Halogen-free)



P-Channel MOSFET



P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS $T_A = 25^\circ\text{C}$, unless otherwise noted

Parameter	Symbol	10 s	Steady State	Unit
Drain-Source Voltage	V_{DS}	- 20		V
Gate-Source Voltage	V_{GS}	± 12		
Continuous Drain Current ($T_J = 150^\circ\text{C}$) ^a	I_D	- 6.3	- 4.3	A
		- 4.5	- 3.1	
Pulsed Drain Current	I_{DM}	- 20		
Continuous Source Current (Diode Conduction) ^a	I_S	- 2.3	- 1.1	
Maximum Power Dissipation ^a	P_D	2.8	1.3	W
		1.5	0.7	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to 150		$^\circ\text{C}$
Soldering Recommendations ^{b,c}		260		

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^a	R_{thJA}	35	44	$^\circ\text{C}/\text{W}$
		75	94	
Maximum Junction-to-Case (Drain)	R_{thJC}	4	5	

Notes:

a. Surface Mounted on 1" x 1" FR4 board.

b. See Solder Profile (www.vishay.com/ppg?73257). The PowerPAK 1212-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

c. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

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SPECIFICATIONS $T_J = 25\text{ }^{\circ}\text{C}$, unless otherwise noted							
Parameter		Test Conditions		Min.	Typ.	Max.	Unit
Static							
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -800\text{ }\mu\text{A}$	-0.45		-1.0	V	
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 4.5\text{ V}$			± 1.5	nA	
		$V_{DS} = 0\text{ V}, V_{GS} = \pm 12\text{ V}$			± 10	mA	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -20\text{ V}, V_{GS} = 0\text{ V}$			-1	μA	
		$V_{DS} = -20\text{ V}, V_{GS} = 0\text{ V}, T_J = 85\text{ }^{\circ}\text{C}$			-5		
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \leq -5\text{ V}, V_{GS} = -4.5\text{ V}$	-20			A	
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = -4.5\text{ V}, I_D = -6.3\text{ A}$		0.041	0.048	Ω	
		$V_{GS} = -2.5\text{ V}, I_D = -5.3\text{ A}$		0.057	0.068		
		$V_{GS} = -1.8\text{ V}, I_D = -1\text{ A}$		0.072	0.090		
Forward Transconductance ^a	g_{fs}	$V_{DS} = -15\text{ V}, I_D = -6.3\text{ A}$		14		S	
Diode Forward Voltage ^a	V_{SD}	$I_S = -2.3\text{ A}, V_{GS} = 0\text{ V}$		-0.8	-1.2	V	
Dynamic ^b							
Total Gate Charge	Q_g	$V_{DS} = -10\text{ V}, V_{GS} = -4.5\text{ V}, I_D = -6.3\text{ A}$		12	18	nC	
Gate-Source Charge	Q_{gs}			2.5			
Gate-Drain Charge	Q_{gd}			2.9			
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -10\text{ V}, R_L = 10\text{ }\Omega$ $I_D \cong -1\text{ A}, V_{GEN} = -4.5\text{ V}, R_G = 6\text{ }\Omega$		2.5	4	μs	
Rise Time	t_r			4	6		
Turn-Off DelayTime	$t_{d(off)}$			15	23		
Fall Time	t_f			12	18		

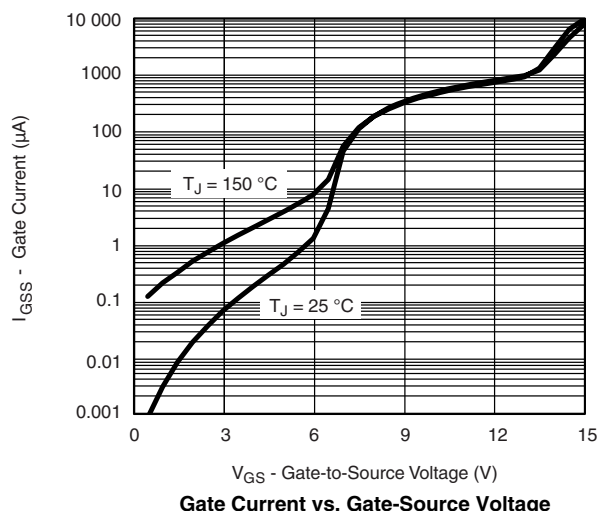
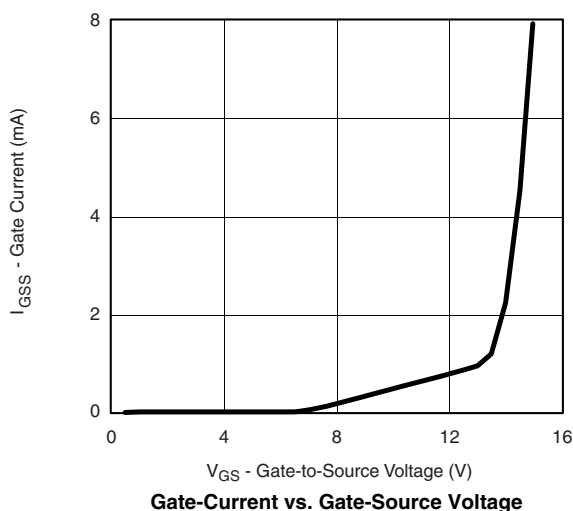
Notes

a. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.

b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, unless otherwise noted

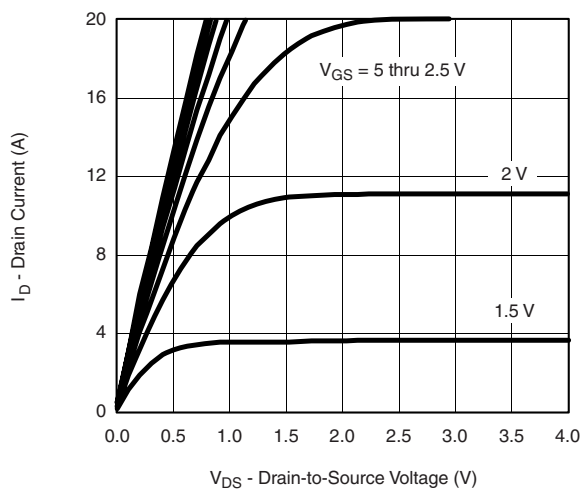




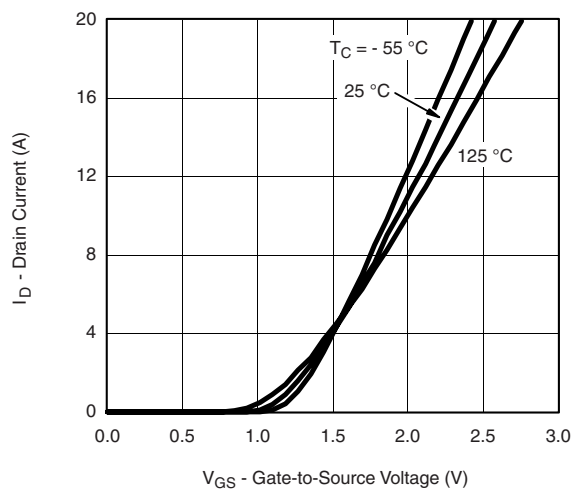
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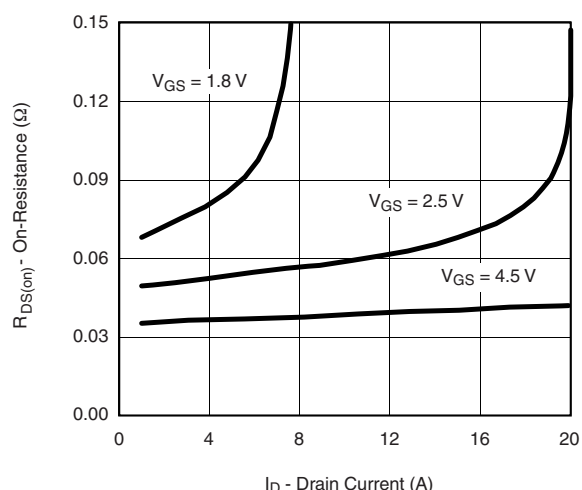
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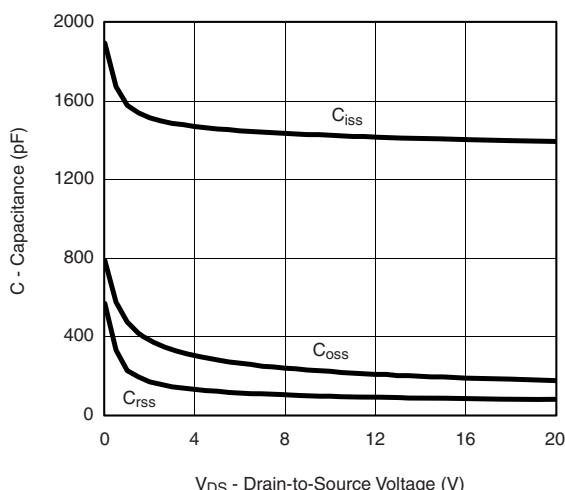
Output Characteristics



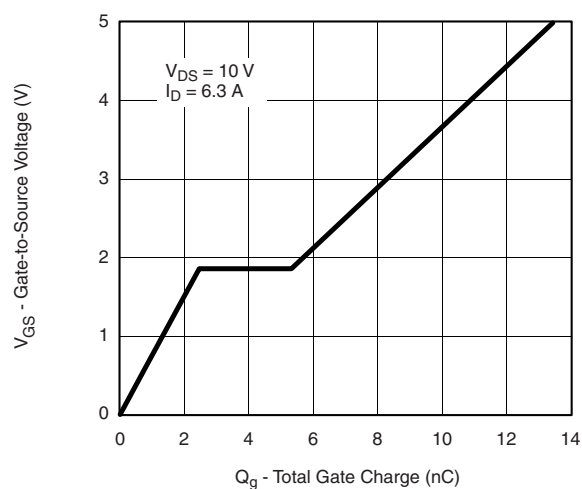
Transfer Characteristics



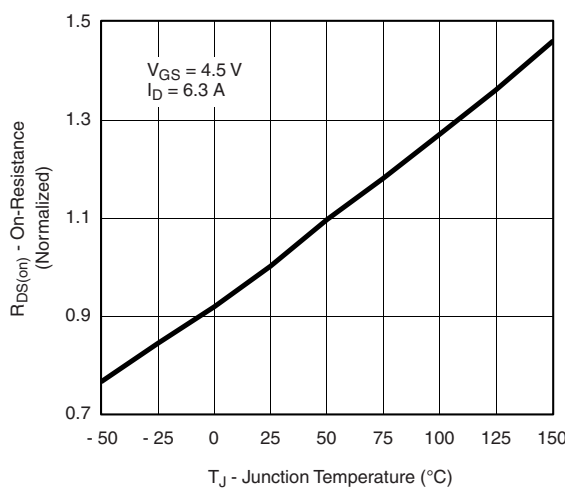
On-Resistance vs. Drain Current



Capacitance



Gate Charge



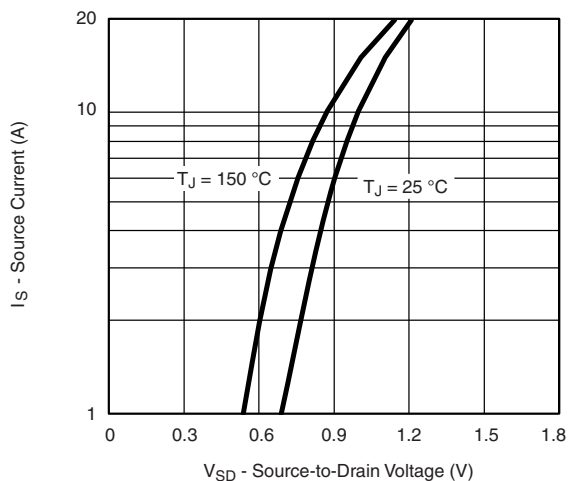
On-Resistance vs. Junction Temperature

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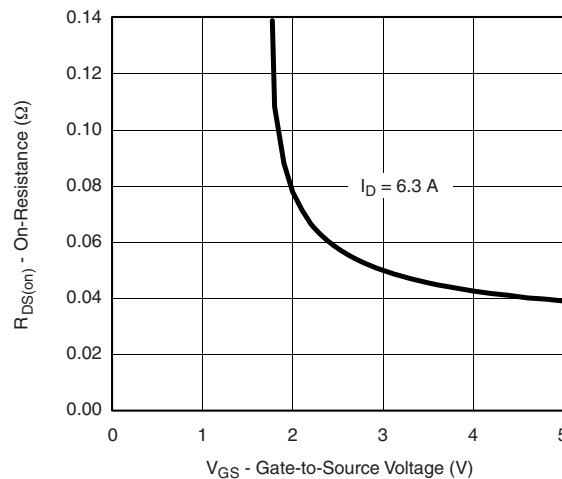
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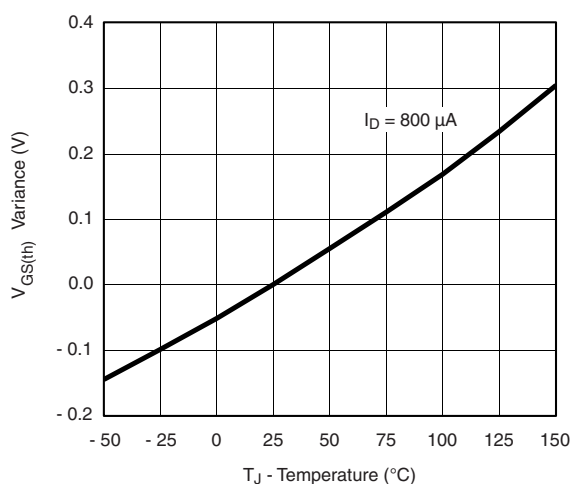
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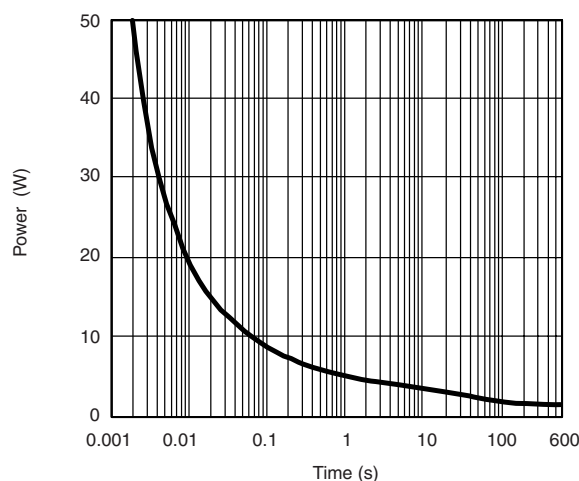
Source-Drain Diode Forward Voltage



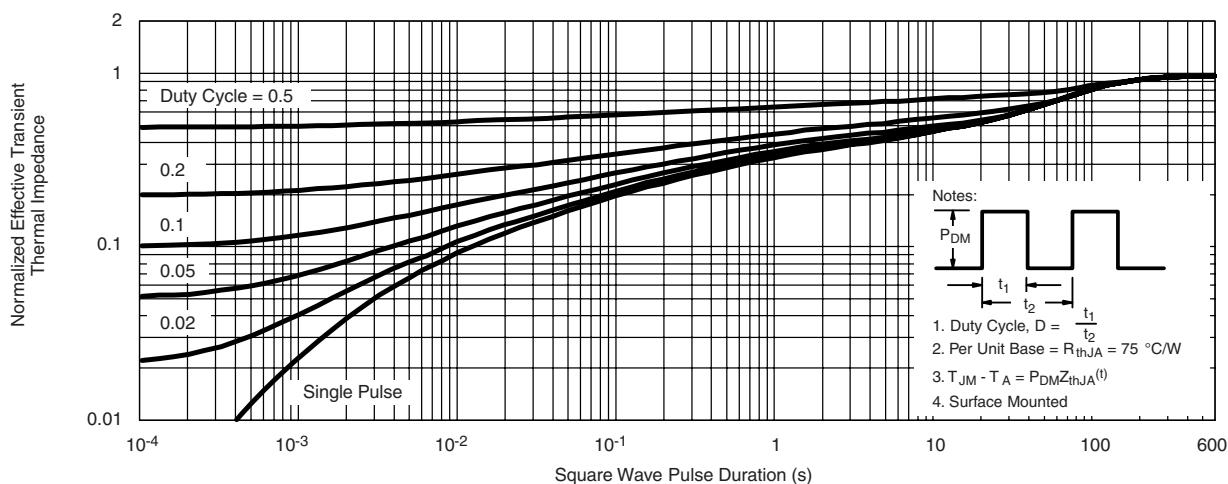
On-Resistance vs. Gate-to-Source



Threshold Voltage



Single Pulse Power, Junction-to-Ambient



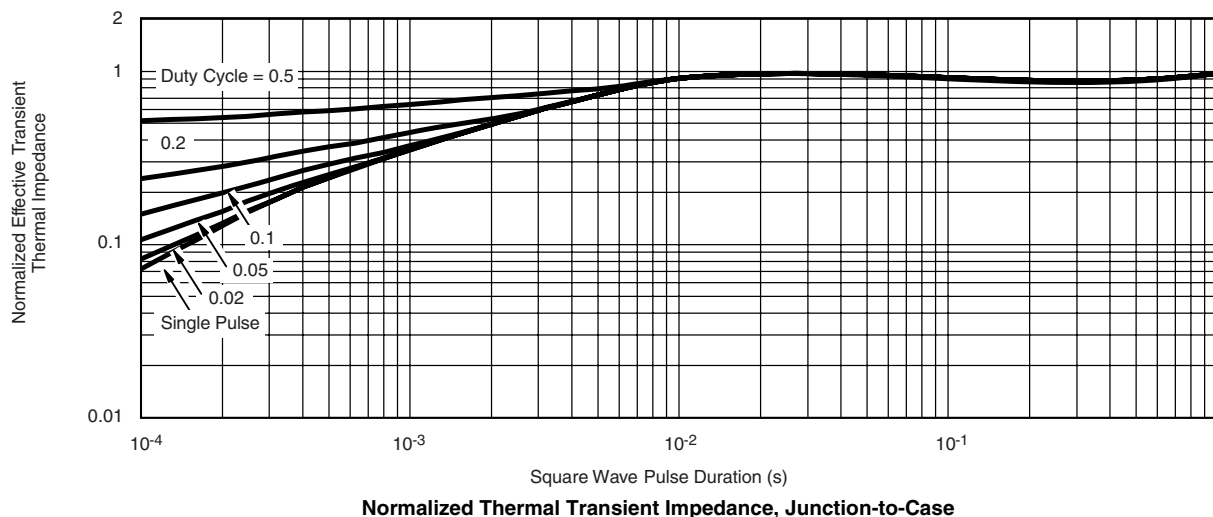
Normalized Thermal Transient Impedance, Junction-to-Ambient



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