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Vishay/Siliconix
SI9913DY-T1-E3

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Product is End of Life 3/2014

Si9913

Vishay Siliconix

Half-Bridge MOSFET Driver for Switching Power Supplies

DESCRIPTION

The Si9913 is a dual MOSFET high-speed driver with break-before-make. It is designed to operate in high frequency dc-dc switchmode power supplies. The high-side driver is boot-strapped to handle the high voltage slew rate associated with "floating" high-side gate drivers. Each driver is capable of switching a 3000 pF load with 60 ns propagation delay and 25 ns transition time. The Si9913 comes with internal break-before-make feature to prevent shoot-through current in the external MOSFETs. A synchronous enable pin is used to enable the low-side driver. When disabled, the OUT_L is logic low.

The Si9913 is available in both standard and lead (Pb)-free 8-pin SOIC packages for operation over the industrial operation range (- 40 °C to 85 °C).

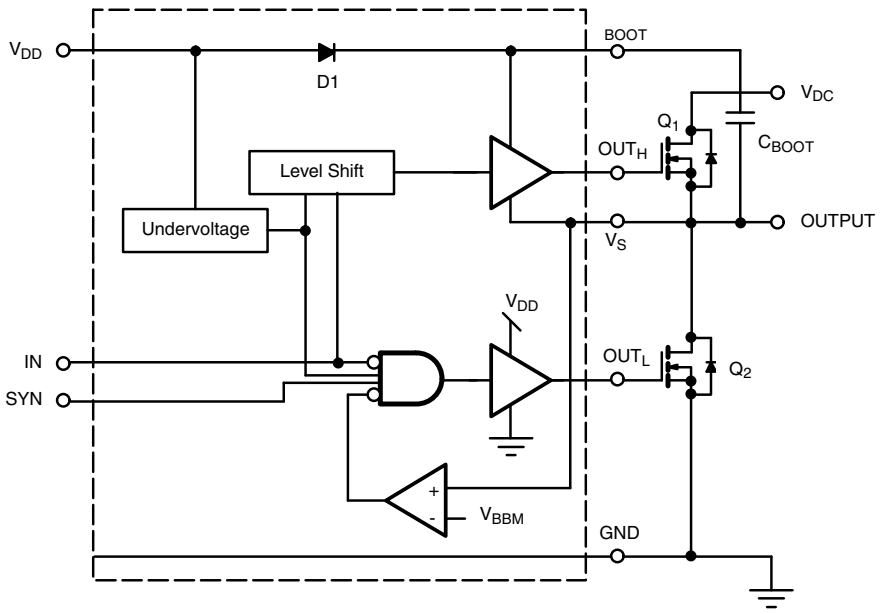
FEATURES

- 4.5 to 5.5 V Operation
- Undervoltage Lockout
- 250 kHz to 1 MHz Switching Frequency
- Synchronous Switch Enable
- One Input PWM Signal Generates Both Drive
- Bootstrapped High-Side Drive
- Operates from 4.5 to 30 V Supply
- TTL/CMOS Compatible Input Levels
- 1 A Peak Drive Current
- Break-Before-Make Circuit

APPLICATIONS

- Multiphase Desktop CPU Supplies
- Single-Supply Synchronous Buck Converters
- Mobile Computing CPU Core Power Converters
- Standard-Synchronous Converters
- High Frequency Switching Converters

FUNCTIONAL BLOCK DIAGRAM AND TRUTH TABLE



TRUTH TABLE				
V_S	SYN	IN	V_{OUTL}	V_{OUTH}
L	L	L	L	L
L	L	H	L	H
L	H	L	H	L
L	H	H	L	H
H	L	L	L	L
H	L	H	L	H
H	H	L	L	L
H	H	H	L	H

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C unless otherwise noted)

Parameter	Symbol	Limit	Unit
Low Side Driver Supply Voltage	V_{DD}	7.0	V
Input Voltage on IN	V_{IN}	- 0.3 to V_{DD} + 0.3	
Synchronous Pin Voltage	V_{SYN}	- 0.3 to V_{DD} + 0.3	
Bootstrap Voltage	V_{BOOT}	35.0	
High Side Driver (Bootstrap) Supply Voltage	V_{BOOT} - V_S	7.0	
Operating Junction Temperature Range	T_J	- 40 to 125	°C
Storage Temperature Range	T_{stg}	- 40 to 150	
Power Dissipation (Note a and b)	P_D	830	mW
Thermal Impedance	θ_{JA}	125	°C/W
Lead Temperature (soldering 10 Sec)		300	°C

Notes:
a. Device Mounted with all leads soldered to P.C. Board.
b. Derate 8.3 W/°C above 25 °C.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Limit	Unit
Bootstrap Voltage (High-Side Drain Voltage)	V_{BOOT}	4.5 to 30	V
Logic Supply	V_{DD}	4.5 to 5.5	
Bootstrap Capacitor	C_{BOOT}	100 n to 1 µ	F
Ambient Temperature	T_A	- 40 to 85	°C

SPECIFICATIONS

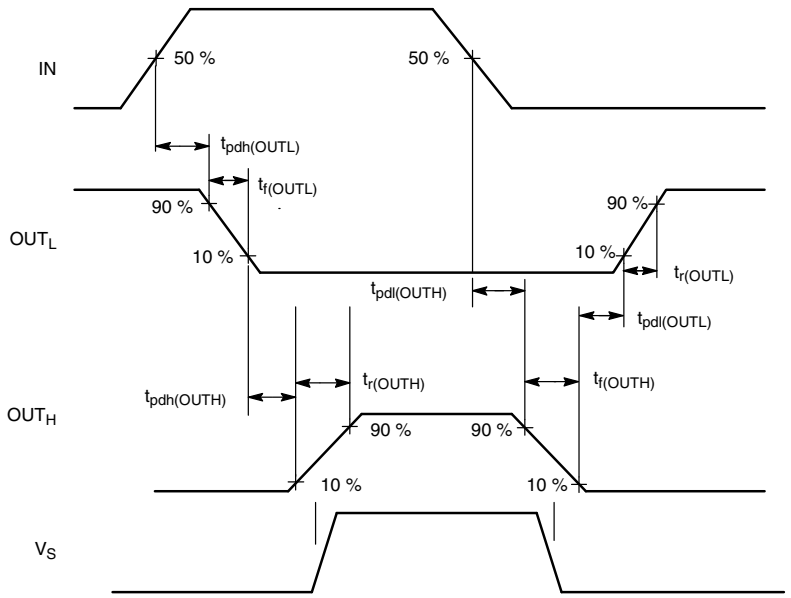
Parameter	Symbol	Test Conditions Unless Specified V_{BOOT} = 4.5 to 30 V, V_{DD} = 4.5 to 5.5 V T_A = - 40 to 85 °C	Limits Min[a]	Typ[b]	Max[a]	Unit
Power Supplies						
V_{DD} Supply	V_{DD}		4.5		5.5	µA
I_{DD} Supply	$I_{DD1(en)}$	SYN = H, IN = H, V_S = 0 V			1000	
I_{DD} Supply	$I_{DD2(en)}$	SYN = H, IN = L, V_S = 0 V			500	
I_{DD} Supply	$I_{DD3(dis)}$	SYN = L, IN = X, V_S = 0 V			500	
I_{DD} Supply	$I_{DD4(en)}$	SYN = H, IN = X, V_S = 25 V, V_{BOOT} = 30 V			200	
I_{DD} Supply	$I_{DD5(dis)}$	SYN = L, IN = X, V_S = 25 V, V_{BOOT} = 30 V			200	
I_{DD} Supply	$I_{DD(en)}$	F_{IN} = 300 kHz, SYN = High, Driving Si4412DY		9		mA
	$I_{DD(dis)}$	F_{IN} = 300 kHz, SYN = Low, Driving Si4412DY		5		
Boot Strap Current	I_{BOOT}	V_{BOOT} = 30 V, V_S = 25 V, V_{OUTH} = H	0.9		3	
Reference Voltage						
Break-Before-Make Reference Voltage	V_{BBM}		1.1		3	V
Logic Inputs (SYN, IN)						
Input High	V_{IH}		0.7 x V_{DD}		V_{DD} + 0.3	V
Input Low	V_{IL}		- 0.3		0.3 x V_{DD}	
Undervoltage Lockout						
V_{DD} Undervoltage	V_{UVL}	V_{DD} Rising	3.7		4.3	V
V_{DD} Undervoltage Hysteresis	V_{HYST}			0.4		

SPECIFICATIONS

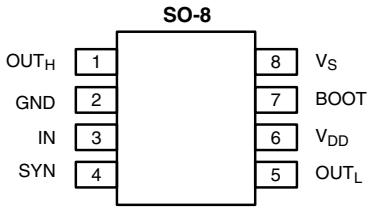
Parameter	Symbol	Test Conditions Unless Specified V_{BOOT} = 4.5 to 30 V, V_{DD} = 4.5 to 5.5 V T_A = - 40 to 85 °C	Limits Min[a]	Typ[b]	Max[a]	Unit
Bootstrap Diode						
Diode Forward Voltage	VF_{D1}	Forward Current = 100 mA		0.8	1	V
Output Drive Current						
OUT_H Source Current	$I_{OUT(H+)}$	V_{BOOT} - V_S = 3.7 V, V_{OUTH} - V_S = 2 V			- 0.4	A
OUT_H Sink Current	$I_{OUT(H-)}$	V_{BOOT} - V_S = 3.7 V, V_{OUTH} - V_S = 1 V	0.4			
OUT_L Source Current	$I_{OUT(L+)}$	V_{DD} = 4.5 V, V_{OUTL} = 2 V			- 0.4	
OUT_L Sink Current	$I_{OUT(L-)}$	V_{DD} = 4.5 V, V_{OUTL} = 1 V	0.6			
Timing (C_{LOAD} = 3 nF)						
OUT_L Off Propagation Delay	$t_{pdl(OUTL)}$	V_{DD} = 4.5 V		30		ns
OUT_L On Propagation Delay	$t_{pdh(OUTL)}$			20		
OUT_H Off Propagation Delay	$t_{pdl(OUTH)}$	V_{BOOT} - V_S = 4.5 V		30		
OUT_H On Propagation Delay	$t_{pdh(OUTH)}$			20		
OUT_L Turn On Time	$t_{r(OUTL)}$	OUT_L = 10 to 90 %		25		
OUT_L Turn Off Time	$t_{f(OUTL)}$	OUT_L = 90 to 10 %		25		
OUT_H Turn On Time	$t_{r(OUTH)}$	OUT_H - V_S = 10 to 90 %		30		
OUT_H Turn Off Time	$t_{f(OUTH)}$	OUT_H - V_S = 90 to 10 %		30		

Notes:
a. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
b. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

TIMING WAVEFORMS



PIN CONFIGURATION



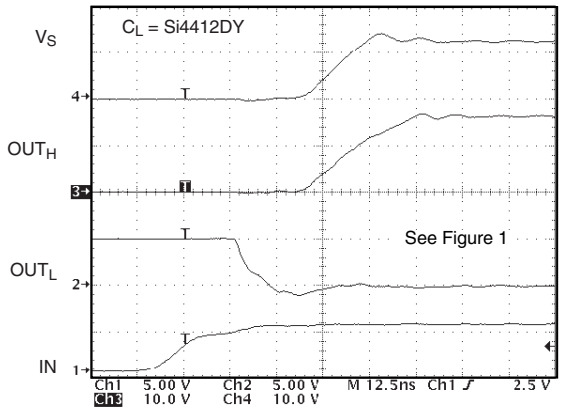
Top View

PIN DESCRIPTION		
Pin Number	**Name**	**Function**
1	OUT_H	Output drive for upper MOSFET.
2	GND	Ground supply
3	IN	CMOS level input signal. Controls both output drives.
4	SYN	Synchronous enable. When logic is high, the low-side driver is enabled.
5	OUT_L	Output drive for lower MOSFET.
6	V_{DD}	Input power supply
7	BOOT	Floating bootstrap supply for the upper MOSFET
8	V_S	Floating GND for the upper MOSFET. V_S is connected to the buck switching node and the source side of the upper MOSFET.

ORDERING INFORMATION		
Part Number	**Temperature Range**	**Package**
Si9913DY	- 40 to 85 °C	Bulk
Si9913DY-T1		Tape and Reel
Si9913DY-T1-E3		Lead (Pb)-free Tape and Reel

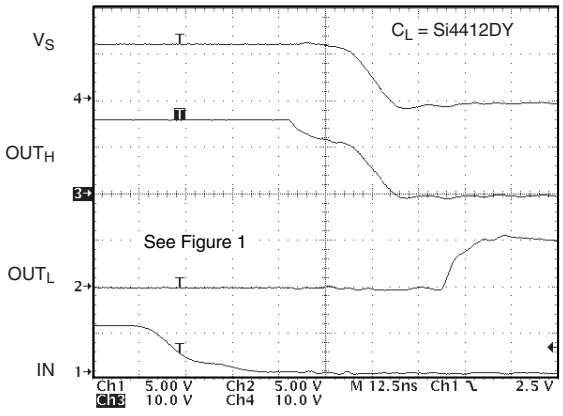
Eval Kit	Temperature Range	Board Type
Si9913DB	- 40 to 85 °C	Surface Mount

TYPICAL WAVEFORMS



Si9912 tr, tf, tpd

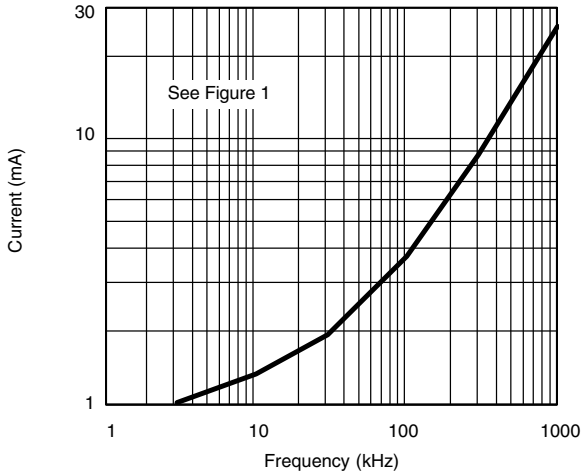
Driver On Switch Delay



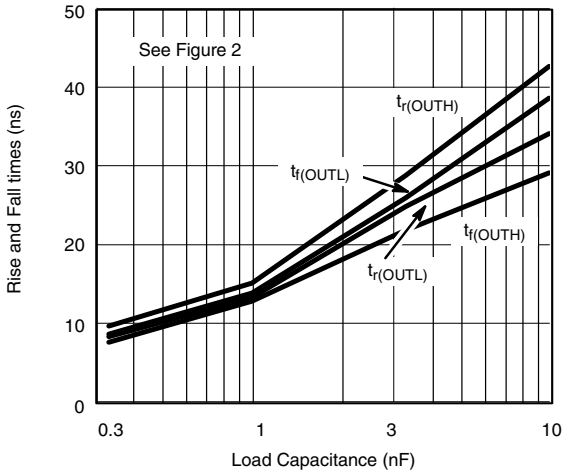
Si9912 tr, tf, tpd

Driver Off Switch Delay

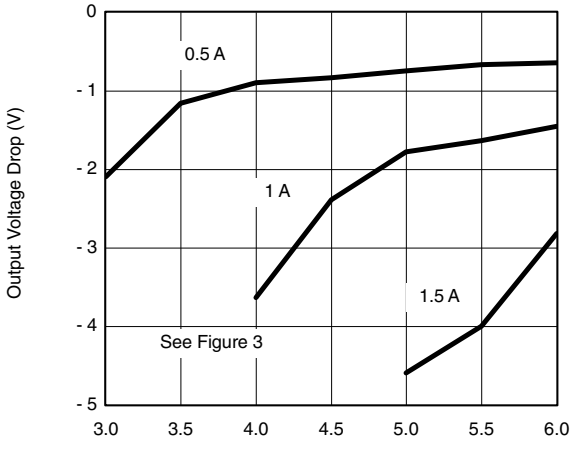
TYPICAL CHARACTERISTICS 25 °C unless noted



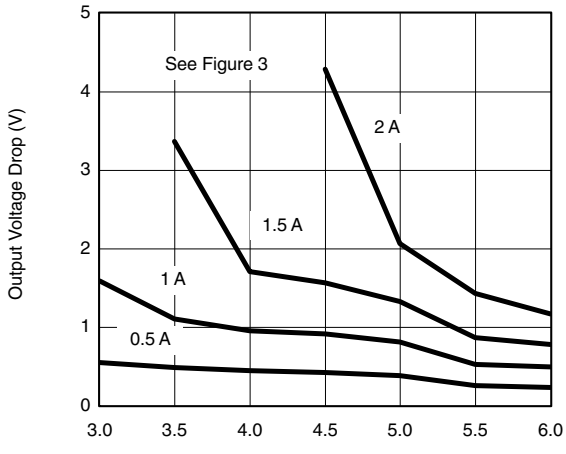
I_{DD} Supply Current vs. Frequency



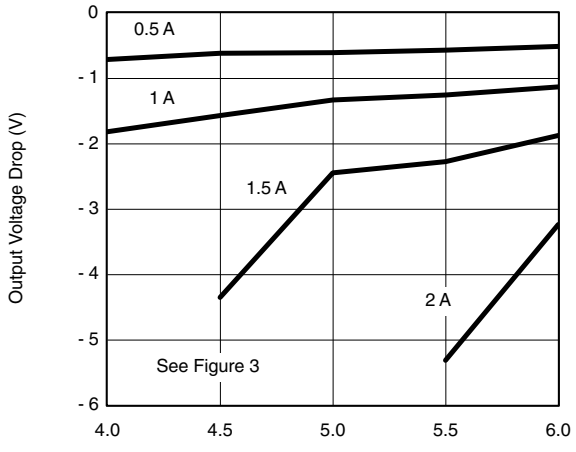
Rise and Fall Time vs. C_{LOAD}



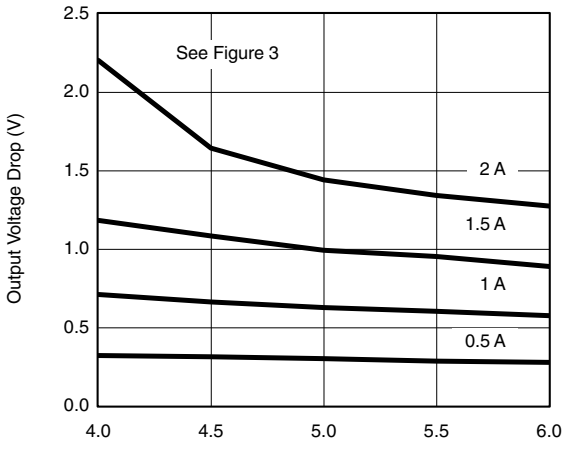
$V_{OUT(H+)}$ vs. Supply



$V_{OUT(H-)}$ vs. Supply

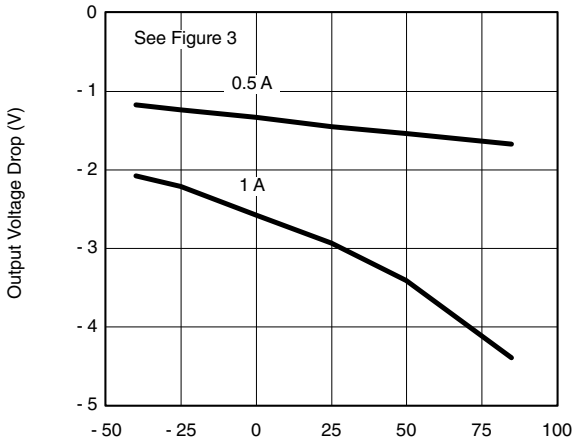


$V_{OUT(L+)}$ vs. Supply

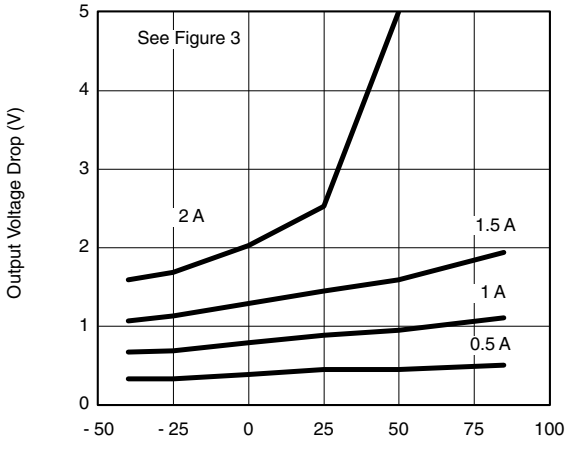


$V_{OUT(L-)}$ vs. Supply

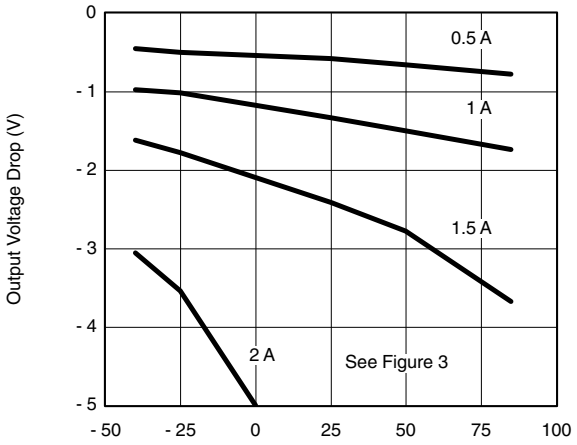
TYPICAL CHARACTERISTICS 25 °C unless noted



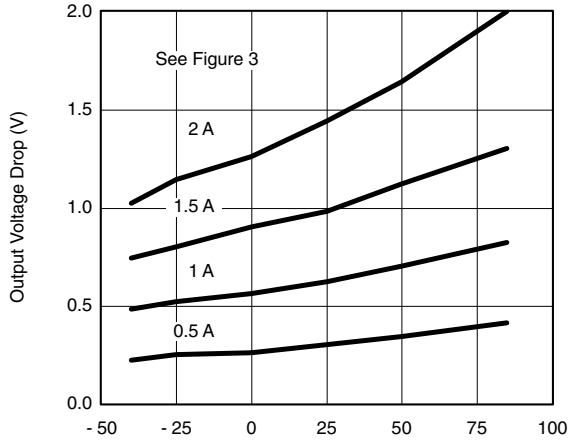
$V_{OUT(H+)}$ vs. Temperature



$V_{OUT(H-)}$ vs. Temperature



$V_{OUT(L+)}$ vs. Temperature



$V_{OUT(L-)}$ vs. Temperature

THEORY OF OPERATION

Break-Before-Make Function

The Si9913 has an internal break-before-make function to ensure that both high-side and low-side MOSFETs are not turned on at the same time. The high-side drive (OUT_H) will not turn on until the low-side gate drive voltage (measured at the OUT_L pin) is less than V_{BBM}, thus ensuring that the low-side MOSFET is turned off. The low-side drive (OUT_L) will not turn on until the voltage at the MOSFET half-bridge output (measured at the V_S pin) is less than V_{BBM}, thus ensuring that the high-side MOSFET is turned off.

Under Voltage Lockout Function

The Si9913 has an internal under-voltage lockout feature to prevent driving the MOSFET gates when the supply voltage (at V_{DD}) is less than the under-voltage lockout specification (V_{UVL}). This prevents the output MOSFETs from being turned on without sufficient gate voltage to ensure they are fully on. There is hysteresis included in this feature to prevent lockout from cycling on and off.

Bootstrap Supply Operation (see Functional Block Diagram)

The power to drive the high-side MOSFET (Q2) gate comes from the bootstrap capacitor (C_{BOOT}). This capacitor charges through D1 during the time when the low-side MOSFET is on (V_S is at GND potential), and then provides the necessary charge to turn on the high-side MOSFET. C_{BOOT} should be sized to be greater than ten times the high-side MOSFET gate capacitance, and large enough to supply the bootstrap current (I_{BOOT}) during the high-side on time, without significant voltage droop.

Synchronous Enable

The synchronous enable pin serves to enable and disable the drive to the low-side MOSFET gate. With SYN high, the low-side MOSFET is driven on and off in antiphase with the high-side MOSFET to form a synchronous rectifier. This improves efficiency at high load currents because the flyback current is carried by the MOSFET, thus eliminating the diode drop. With SYN low, the low-side MOSFET is held off all the time. This is particularly useful for discontinuous operation under light load or pulse skipping mode, where there is a long off time, because it prevents current flowing back from the output to ground during the off time.

Layout Considerations

There are a few critical layout considerations for these parts. Firstly, the IC must be decoupled as closely as possible to the power pins. Secondly the IC should be placed physically close to the high- and low-side MOSFETs it is driving. The major consideration is that the MOSFET gates must be charged or discharged in a few nanoseconds, and the peak current to do this is of the order of 1 A. This current must flow from the decoupling and bootstrap capacitors to the IC, and from the output driver pin to the MOSFET gate, returning from the MOSFET source to the IC. The aim of the layout is to reduce the parasitic inductance of these current paths as much as possible. This is accomplished by making these traces as short as possible, and also running trace and its

APPLICATIONS

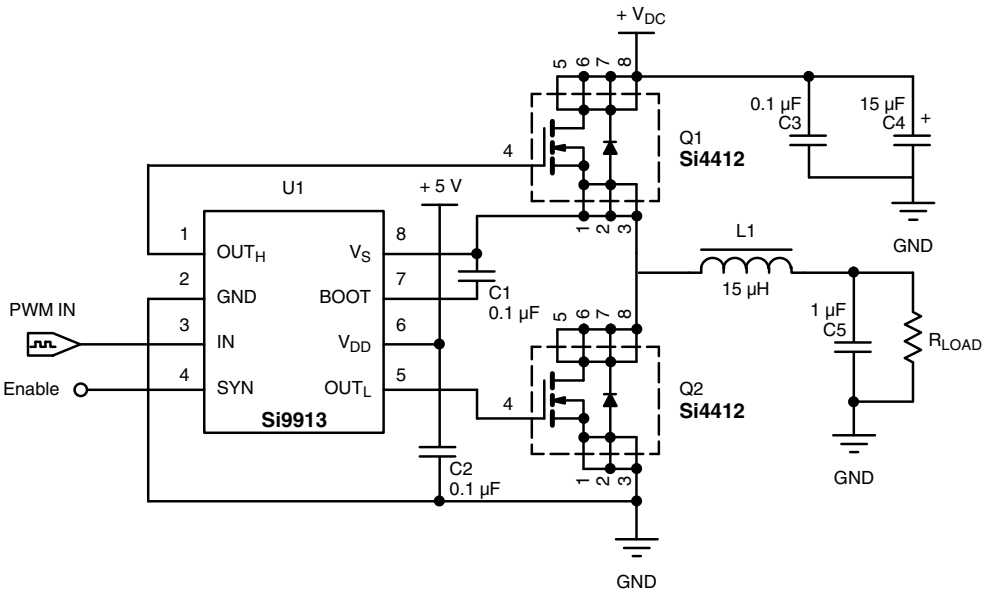


Figure 1. Typical Applications Schematic Circuit Used to Obtain Typical Rising and Falling Switching Waveforms

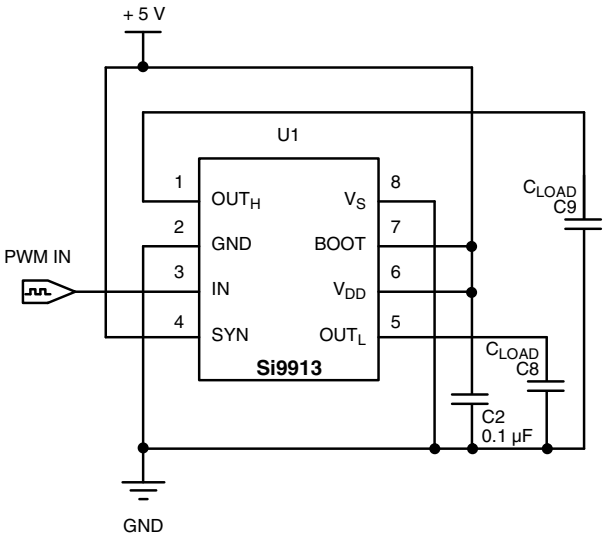


Figure 2. Capacitive Load Test Circuit Used to Measure Rise and Fall Times vs. Capacitance

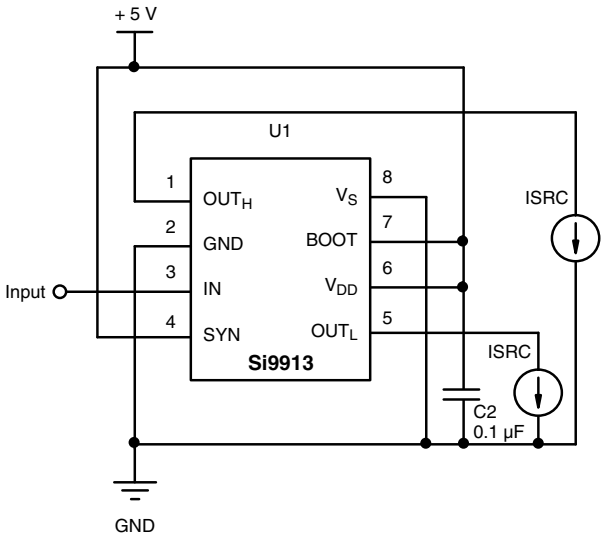


Figure 3. Load Test Schematic Circuit Used to Measure Driver Output Impedance

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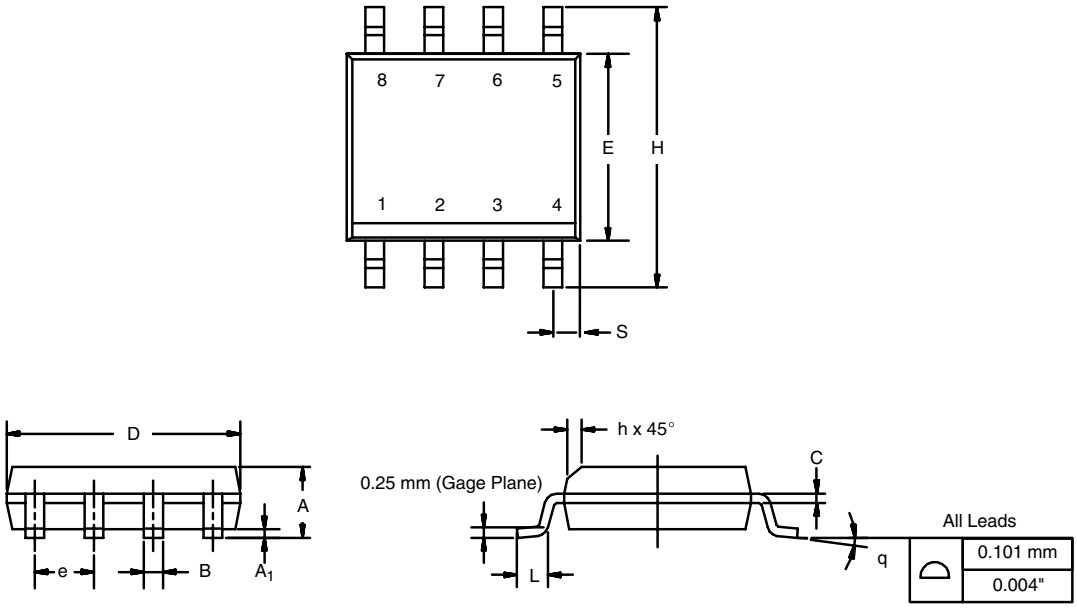
Package Information

Vishay Siliconix

SOIC (NARROW): 8-LEAD

JEDEC Part Number: MS-012



DIM	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A_1	0.10	0.20	0.004	0.008
B	0.35	0.51	0.014	0.020
C	0.19	0.25	0.0075	0.010
D	4.80	5.00	0.189	0.196
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.020
L	0.50	0.93	0.020	0.037
q	0°	8°	0°	8°
S	0.44	0.64	0.018	0.026
ECN: C-06527-Rev. I, 11-Sep-06 DWG: 5498				

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