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Vishay/Siliconix
SIC413CB-T1-E3

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*End of Life. Last Available Purchase Date is 31-Dec-2014*



# microBUCK® SiC413
## 4 A, 26 V Integrated Synchronous Buck Regulator

### DESCRIPTION

The SiC413 is an integrated, DC/DC power conversion solution with built-in PWM-optimized high- and low-side n-channel MOSFETs and advanced PWM controller. The SiC413 provides a quick and easy to use POL voltage regulation solution for a wide range of applications. Vishay Siliconix's Proprietary packaging technology is used to optimize the power stage and minimize power losses associated with parasitic impedances and switching delays. The co-packaged Gen III TrenchFET power MOSFET devices deliver higher efficiency than lateral DMOS monolithic solutions.

| PRODUCT SUMMARY | |
|---|---|
| Input Voltage Range | 4.75 V to 26 V |
| Output Voltage Range | 0.6 V to 13.2 V |
| Operating Frequency | 500 kHz |
| Continuous Output Current | 4 A |
| Peak Efficiency | 93 % |
| Highside/Lowside $R_{DS\_ON}$ | 35 mΩ/19 mΩ |
| Package | SO-8 |

### FEATURES

- Integrated PWM controller and Gen III trench MOSFETs
- Quick and easy single chip converter
- Integrated current sense
- Cycle by cycle over-current protection
- Built-In bootstrap diode
- Output over-voltage protection
- Under voltage lockout
- Thermal shutdown
- Soft start
- Break-before-make operation
- PowerCAD Simulation software available at www.vishay.com/power-ics/powercad-list/
- Material categorization: For definitions of compliance please see www.vishay.com/doc?99912

Pb-free RoHS COMPLIANT HALOGEN FREE

### APPLICATIONS

- LCD TV, set top box and DVD player
- Desktop PC and server
- Add-in graphics board
- Memory, FPGA or µP device power supplies
- Point of load DC/DC conversion
- Telecom and networking equipment

### TYPICAL APPLICATION

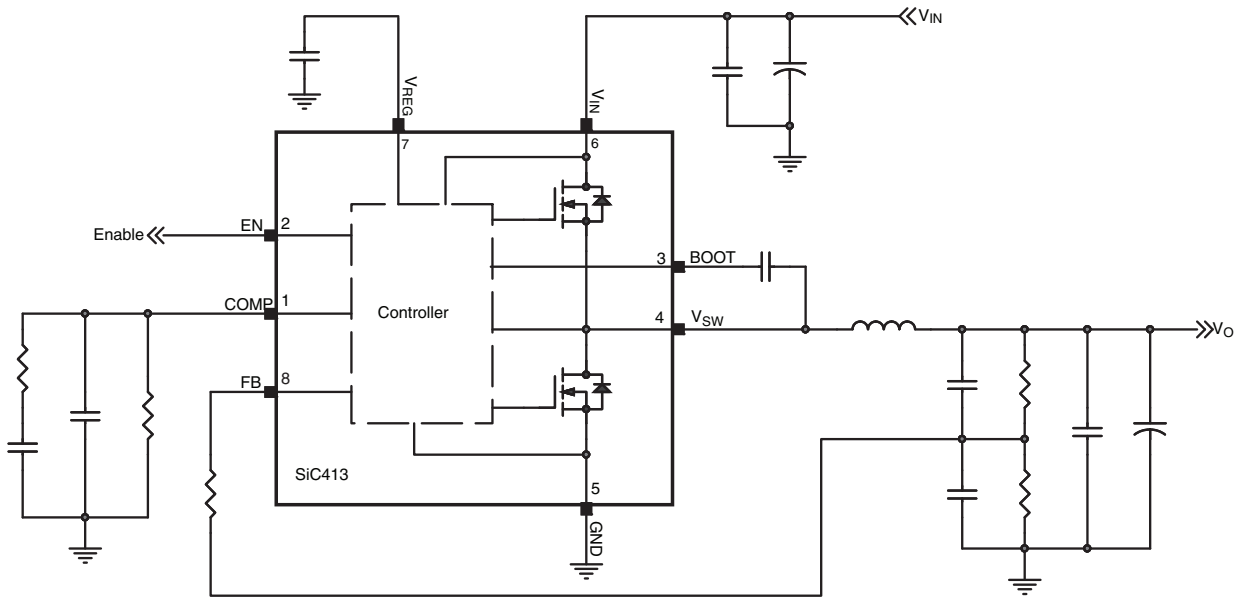



**Figure 1 - Typical Application Circuit**

## PIN CONFIGURATION

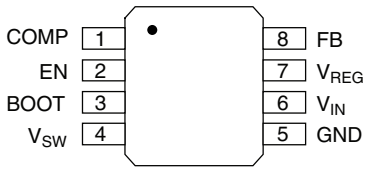



**Figure 2. SO-8 Pin Out - Top View**

| PIN DESCRIPTION | | |
|---|---|---|
| **Pin Number** | **Symbol** | **Description** |
| 1 | COMP | Error amplifier output. Connects to the compensation network. |
| 2 | EN | Chip enable pin. Active HIGH. Connects to a power source through a 10K to100K resistor to enable. |
| 3 | BOOT | Connect to 0.1 µF capacitor from $V_{SW}$ to BOOT to power the high side gate driver. |
| 4 | $V_{SW}$ | Inductor Connection. Connect an output filter inductor to this pin. $V_{SW}$ is high impedance when the IC is in shutdown mode. |
| 5 | GND | GROUND pin. |
| 6 | $V_{IN}$ | Supply voltage. |
| 7 | $V_{REG}$ | Internal regulator output. An external 4.7 µF decoupling capacitor is required at this pin. |
| 8 | FB | Output voltage feedback input. |

| ORDERING INFORMATION | |
|---|---|
| **Part Number** | **Package** |
| SiC413CB-T1-E3 | SO-8 (6.2 x 5 x 1.75 mm) |
| SiC413DB | Reference board |

## FUNCTIONAL BLOCK DIAGRAM

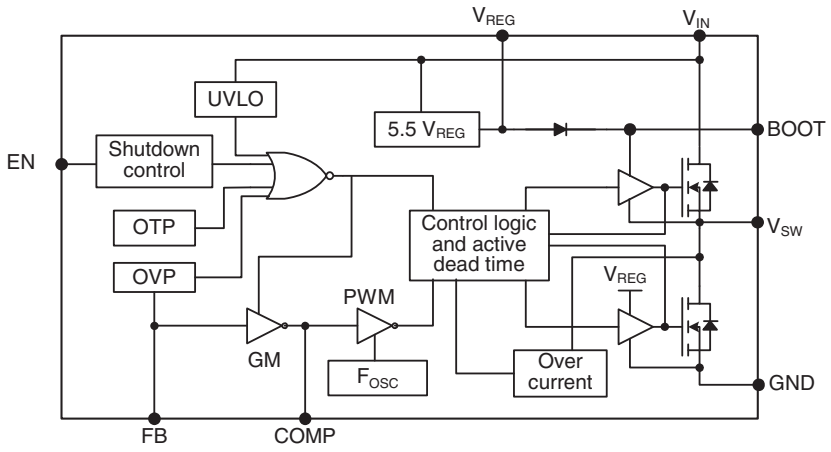



**Figure 3. Functional Block Diagram**

## ABSOLUTE MAXIMUM RATINGS ($T_A$ = 25 °C, unless otherwise noted)[a]

| Parameter | Symbol | Min. | Max. | Unit |
|---|---|---|---|---|
| Input Breakdown Voltage | $V_{IN}$ | - 0.3 | 28 | V |
| Common Switch Node Breakdown Voltage | $V_{SW}$ DC | - 1 | 28 | |
| | $V_{SW}$ Peak[c] | -1 | 30 | |
| Logic Inputs | $V_{COMP}$, $V_{FB}$, $V_{EN}$ | - 0.3 | 6 | |
| Bootstrap Voltage | $V_{BOOT}$ | - 0.3 | 33 | |
| Maximum Power Dissipation | $P_D$ | | 1.5 | W |
| Operating Temperature | $T_j$ | - 25 | 125 | °C |
| Storage Junction Temperature | $T_{stg}$ | - 40 | 150 | |
| Soldering Peak Temperature | | | 260 | |

Notes:
a. $T_A$ = 25 °C and all voltages referenced to GND unless otherwise noted.

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating/conditions for extended periods may affect device reliability.*

## RECOMMENDED OPERATING CONDITIONS[b]

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Input Voltage | $V_{IN}$ | 4.75 | 12 | 26 | V |
| Logic Inputs | $V_{COMP}$, $V_{FB}$, $V_{EN}$ | 4.5 | 5 | 5.5 | |
| Common Switch Node | $V_{SW\ DC}$ | - 0.3 | 12 | 26 | |
| | $V_{SW\ peak}$[c] | - 0.3 | 24 | 28 | |

Notes:
b. Recommended operating conditions are specified over the entire temperature range, and all voltages referenced to GND unless otherwise noted.
c. Peak value is specified for pulses ≤ 100 ns.

## THERMAL RESISTANCE RATINGS

| Parameter | Symbol | Typ. | Unit |
|---|---|---|---|
| Junction-to-Case Resistance<br>In Operation, Max. Junction | $R_{thJC}$ | Contact Vishay for thermal design assistance | °C/W |
| Junction-to-Ambient Resistance<br>PCB = Copper 25 mm x 25 mm | $R_{thJA}$ | | |
| Case Top to Board Edge<br>PCB = EVBSiC413 Rev. 3.0; No Forced Airflow | $R_{thCA}$ | | |

# SiC413

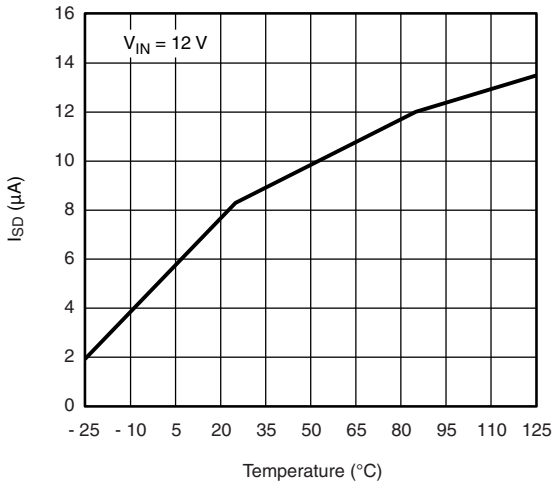
Vishay Siliconix

## SPECIFICATIONS

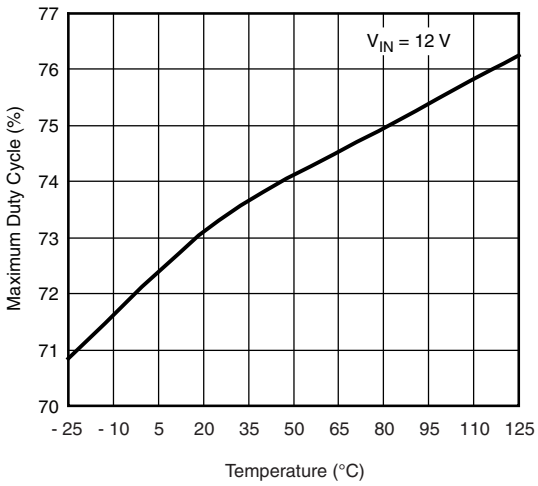
| Parameter | Symbol | Conditions Unless Specified Otherwise $V_{IN}$ = 12 V, $V_{EN}$ = 5 V, $V_{OUT}$ = 3.3 V, $T_A$ = 25 °C | Min. | Typ.[a] | Max. | Unit |
|---|---|---|---|---|---|---|
| **Converter Operation** | | | | | | |
| Output Current[a] | $I_{OUT}$ | Air flow = 0 | | 4 | | A |
| Internal Regulated Voltage | $V_{REG}$ | | 5 | 5.7 | 6.1 | V |
| Load Regulation[a] | | 0 ≤ $I_O$ ≤ 4 A | | | 0.6 | % |
| Line Regulation[a] | | $I_{OUT}$ = 0 | | | 0.1 | %/V |
| Feedback Voltage | $V_{FB}$ | $T_A$ = 25 °C | 0.591 | 0.6 | 0.609 | V |
| | | $T_A$ = - 25 °C to 85 °C | 0.582 | 0.6 | 0.618 | |
| MOSFET On Resistance | $R_{DS(ON)HS}$ | $V_{BOOT}$ - $V_{SW}$ = 5.5 V | | 35 | | mΩ |
| | $R_{DS(ON)LS}$ | $V_{REG}$ = 5.5 V | | 19 | | |
| Internal Oscillator Frequency | $F_{OSC}$ | | 435 | 500 | 565 | kHz |
| Max. PWM Duty Cycle | DC | | 62 | 70 | | % |
| **Error Amplifier** | | | | | | |
| Open Loop Voltage Gain | | | | 110 | | dB |
| Unity Gain Bandwidth | | | | 2.5 | | MHz |
| Transconductance | | | | 1.5 | | mS |
| Input Bias Current | $I_{FB}$ | | | 2 | | nA |
| Max. Sink/Source Current | | | | 30 | | µA |
| **Enable** | | | | | | |
| Enable Logic Level High | $V_{EN\ H}$ | $V_{EN}$ rising | 1.8 | | | V |
| Enable Logic Level Low | $V_{EN\ L}$ | $V_{EN}$ falling | | | 0.6 | |
| **Protection** | | | | | | |
| Overvoltage Trip Point | OVP | $V_{FB}$ rising and when $V_{FB}/V_{REF}$ is greater than | 115 | 120 | 125 | % |
| Overvoltage Trip Hysteresis | $OVP_{HYS}$ | $V_{FB}$ falling and when $V_{FB}/V_{REF}$ is less than | | 110 | | |
| $V_{IN}$ Undervoltage Lockout | $V_{IN\ UVLO-h}$ | $V_{IN}$ rising | 3.55 | 3.8 | 4.05 | V |
| $V_{IN}$ Undervoltage Lockout Hysteresis | $V_{IN\ UVLO\ HS}$ | $V_{IN}$ falling | | 200 | | mV |
| Thermal Shutdown | $T_{J\ SD}$ | | | 165 | | °C |
| Thermal Shutdown Hysteresis | $T_{J\ SD\ HS}$ | | | 20 | | |
| Peak Current Limit | $I_{LIM}$ | | | 7 | | A |
| **Soft Start** | | | | | | |
| Soft Start Period | $T_{SS}$ | | | 5 | | ms |
| **Supply Current** | | | | | | |
| Input Current | $I_Q$ | $V_{EN}$ = high and no load | | 10 | | mA |
| Shutdown Current | $I_{SD}$ | $V_{EN}$ = 0 V | | 8 | | µA |
| **Dynamic[b]** | | | | | | |
| Rise Time | $T_{r\_SW}$ | 10 % to 90 % of SW | | 16 | | ns |
| Fall Time | $T_{f\_SW}$ | 90 % to 10 % of SW | | 15 | | |

Notes:
a. Guaranteed by design and not 100 % production tested.
b. Pulse test; pulse width ≤ 300 ms, duty cycle ≤ 2 %.

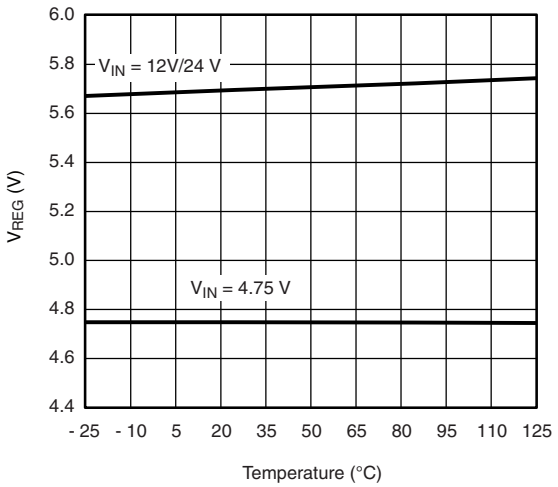
## ELECTRICAL CHARACTERISTICS



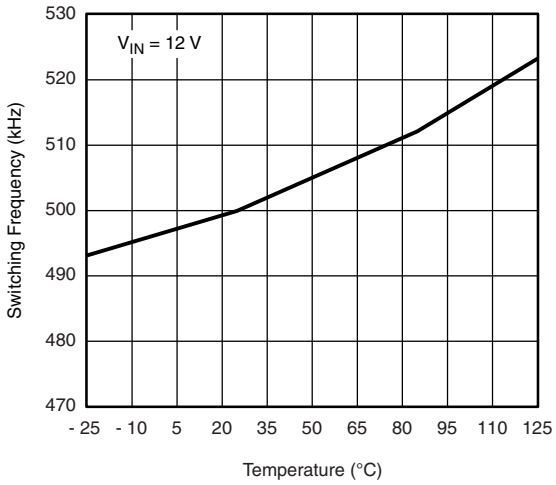

**Shut Down Current vs. Temperature**



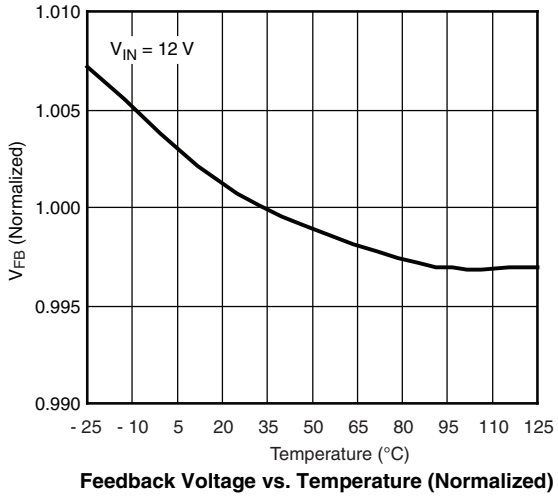

**Maximum Duty Cycle vs. Temperature**



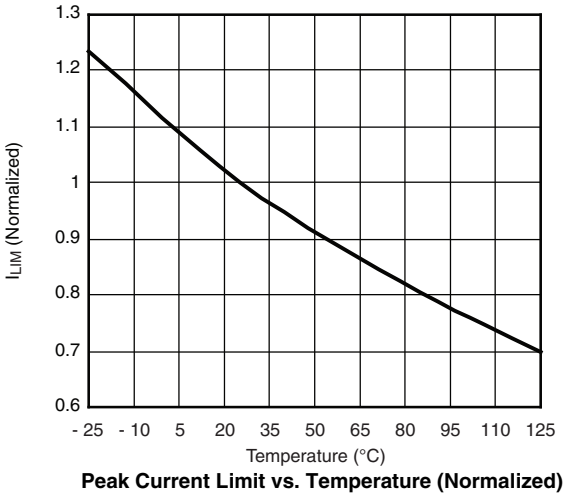

**Internal Regulator Voltage vs. Temperature**




**Frequency vs. Temperature**

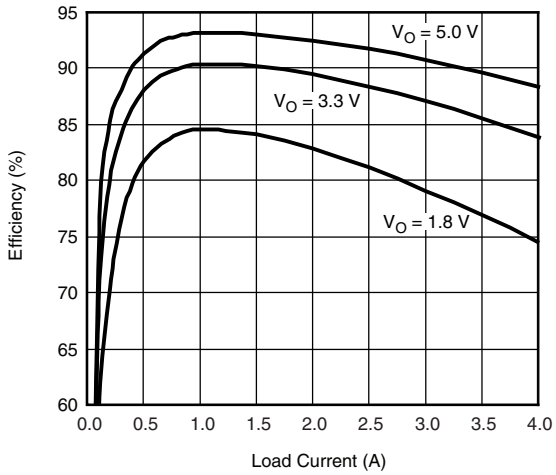



**Feedback Voltage vs. Temperature (Normalized)**

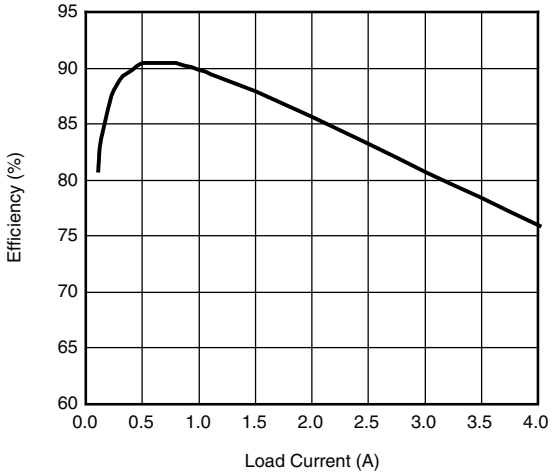



**Peak Current Limit vs. Temperature (Normalized)**

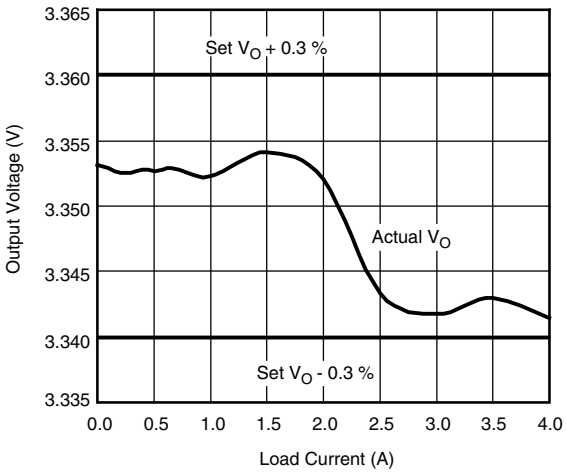
## ELECTRICAL CHARACTERISTICS



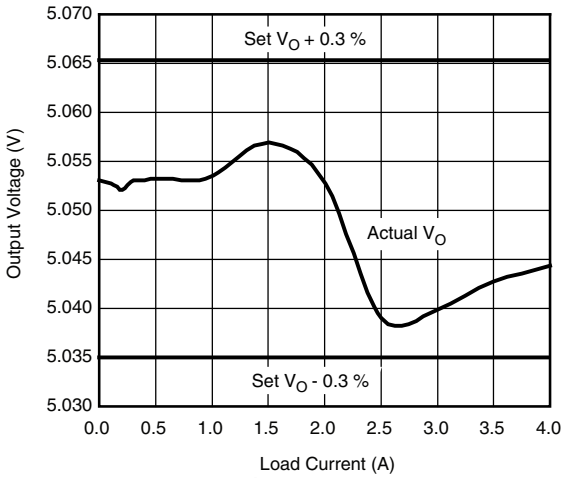

**Efficiency at $V_{IN}$ = 12 V**




**Efficiency at $V_{IN}$ = 5 V and $V_O$ = 1.8 V**

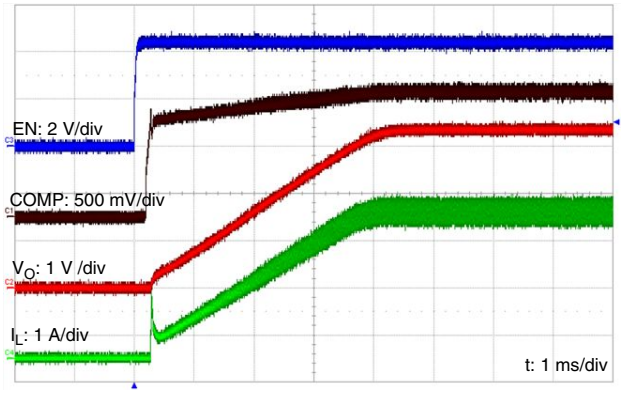



**Load Regulation at $V_{IN}$ = 12 V, $V_O$ = 3.3 V**

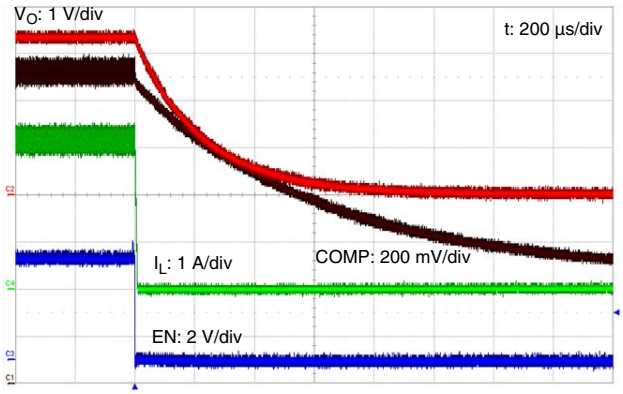



**Load Regulation at $V_{IN}$ = 12 V, $V_O$ = 5.0 V**

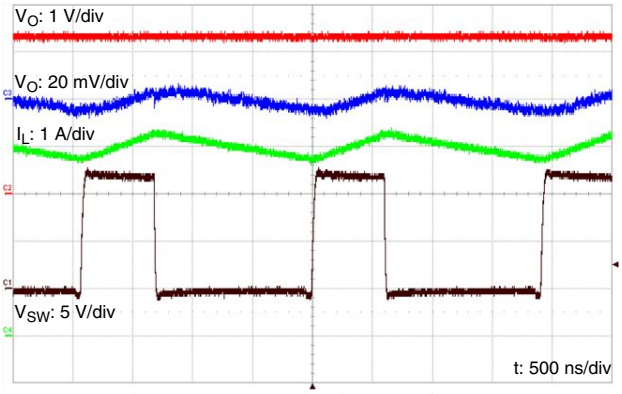
## ELECTRICAL CHARACTERISTICS



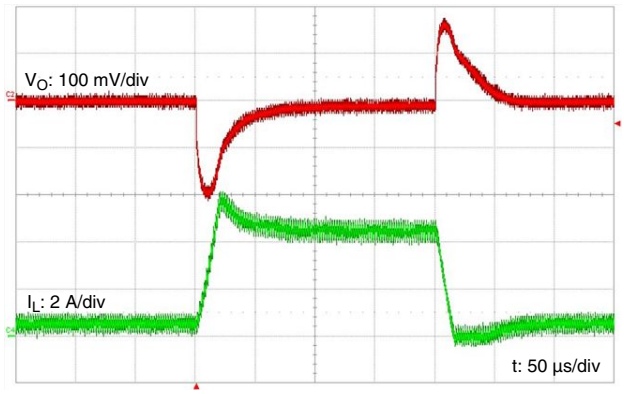

**System starts up with EN pin becoming HIGH while $V_{IN}$ is ready. $V_{IN}$ = 12 V, $V_O$ = 3.3 V and $I_O$ is preset to about 3 A. Resistive load.**



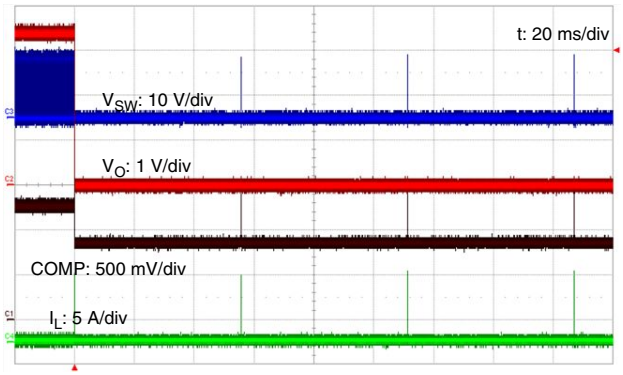

**System shuts down with EN pin becoming LOW. $V_{IN}$ = 12 V, $V_O$ = 3.3 V and $I_O$ comes down from about 3 A.**




**$V_O$ ripple and $V_{SW}$ switching waveform. $V_{IN}$ = 12 V, $V_O$ = 3.3 V and L = 10 µH (IHLP2525EZ type). $C_O$ consists of MLCC of 4.7 µF and tantalum of 100 µF/20 V x 2**




**Transient response. $V_{IN}$ = 12 V, $V_O$ = 3.3 V and L = 10 µH (IHLP2525EZ type). $C_O$ consists of MLCC of 4.7 µF and tantalum of 100 µF/20 V x 2. Output current steps up and down between 0.4 A and 4 A with less than 1 µs rising and falling time.**




**Overcurrent protection at $I_O$ = 8 ~ 10 A. $V_{IN}$ = 12 V, $V_O$ = 3.3 V and L = 10 µH (IHLP2525EZ type). $C_O$ consists of MLCC of 4.7 µF and tantalum of 100 µF/20 V x 2**

## DETAILED OPERATIONAL DESCRIPTION

### Input Voltage ($V_{IN}$)

The input voltage pin on the SiC413CB provides the bias supply for the PWM controller IC and the MOSFET driver circuitry. This pin also is internally connected to the drain of the high side MOSFET.

### Feedback (FB) and Output Voltage ($V_O$)

The FB pin is the negative input of the internal error amplifier. This pin connects to the center of the output voltage divider, through a 10K ~ 100K resistor (for noise isolation). When in regulation the FB voltage is 0.6 V. The output voltage $V_O$ is set based on the following formula.

$$V_O = V_{REF} (1 + R1/R2)$$

where R1 and R2 are shown in Figure 4.

### Enable (EN)

CMOS logic signal. In the low state, the EN pin shuts down the driver IC and disables both high-side and low-side MOSFETs. An internal pull up resistor will enable the device if this pin is left open. An external pull up of 10 kΩ to 100 kΩ is recommended for better noise immunity.

### Soft-Start (SS)

This device allows typical 5 ms soft start time to prevent inrush current during system startup. The soft start cycle starts when EN is asserted (low to high).

### Under Voltage Lockout (UVLO)

The SiC413CB incorporates an under voltage lockout circuit to keep the device disabled when the input voltage ($V_{IN}$) is below x.xx V typical. During power up, internal circuits are held inactive until $V_{IN}$ exceeds the nominal UVLO threshold voltage. Once the UVLO rising threshold is reached, the device start-up begins. The device keeps operating unless $V_{IN}$ drops below UVLO falling threshold. The nominal 200 mV UVLO hysteresis and 2.5 µs rising and falling edge de-glitch circuit reduce the likelihood of the device shutdown due to noise on $V_{IN}$.

### Switch Node ($V_{SW}$)

The switch node is the interconnection between the and high- and low-side MOSFETs. Connect the output inductor to this pin. Also, this node is the return path for the bootstrap capacitor.

### Bootstrap Circuit (BOOT)

A diode and a capacitor form a bootstrap circuit that powers high-side MOSFET driver. SiC413 has this diode built in and therefore only an external capacitor is required to form this circuit. This capacitor is connected between BOOT pin and $V_{SW}$ pin.

### Over Temperature Protection (OTP)

OTP provides thermal protection to the controller and power MOSFETs when an overload condition occurs. When the junction temperature of the SiC413CB exceeds nominal 165 °C (OTP trip point), the power MOSFETs will be turned off and the controller will be disabled. The device will automatically restart when the junction temperature drops to nominal 20 °C below its trip point. After the thermal protection is deasserted, a regular soft start cycle will be initiated.

### Over Voltage Protection (OVP)

When the feedback voltage on FB pin exceeds 120 % of $V_{REF}$, the over voltage condition is asserted. When over voltage occurs, the controller will turn on low-side MOSFET and turn off high-side MOSFET to discharge the excessive output voltage. The over voltage condition is removed when the voltage on FB pin drops to below 110 % of $V_{REF}$.

### Over Current Protection (OCP)

The SiC413CB integrates all components required for over current protection. This achieved by sensing the current flowing through the Low-side MOSFET. When low-side MOSFET is turned on, the current flowing through it will generate a voltage drop determined by its $R_{DS(ON)}$. After a blanking time delay (to ignore switching noise), this voltage is compared to a reference that corresponds to a preset overcurrent threshold (typical 7 A peak). If the voltage drop on low-side MOSFET is higher than the preset reference, an overcurrent protection event occurs. This triggers the PWM controller to keep the low side MOSFET on until the inductor current discharges to a level below the over current protection threshold. This lowers the duty cycle and causes the output voltage to droop.

The SiC413CB overcurrent fault mode is designed to protect against false triggering.An overcurrent event is defined as starting when the overcurrent threshold is tripped and ending when the inductor current in the low side MOSFET is below the overcurrent trheshold. Seven sequential overcurrent events are required to place the SiC413CB into the over current fault mode.

Overcurrent events are counted by an up down counter. If the overcurrent state is detected, the counter counts 1 up otherwise it counts 1 down. If the count reaches 7, the device will enter fault mode and both high- and low-side MOSFETs will turn off for 15 PWM clock cycles. After this period, the device will initiate a regular soft start. This sequence repeats until the overcurrent is completely removed. This is often referred to as hiccup mode. If the counter does not reach the count of 7. The SiC413CB does not enter into the overcurrent fault mode and operation is not disrupted.

### Shoot-Through Protection (Break-Before-Make: BBM)

The SiC413CB has an internal break-before-make function to ensure that both high- and low-side MOSFETs are not turned on at the same time.

An internal circuit detects the falling edge of both high- and low-side gate drive. The low-side MOSFET is turned on only after the high-side gate voltage is less than $V_{BBM}$, similarly the high-side MOSFET gate is turned on after a fixed dead-time after the low side gate is less than $V_{BBM}$. This Break-Before-Make time parameter is not user adjustable.

## APPLICATION NOTES

### Inductor Selection

The inductor is one of the energy storage components in a converter. Choosing an inductor means specifying its size, structure, material, inductance, saturation level, DC-resistance (DCR), and core loss. Fortunately, there are many inductor vendors that offer wide selections with ample specifications and test data, such as Vishay Dale.

The following are some key parameters that users should focus on. In PWM mode, inductance has a direct impact on the ripple current. Assuming 100 % efficiency, the steady state peak-to-peak inductor (L) ripple current ($I_{PP}$) can be calculated as

$$I_{PP} = \frac{V_O \cdot (V_{IN} - V_O)}{V_{IN} \cdot L \cdot f}$$

where f = switching frequency.

Higher inductance means lower ripple current, lower rms current, lower voltage ripple on both input and output, and higher efficiency, unless the resistive loss of the inductor dominates the overall conduction loss. However, higher inductance also means a bigger inductor size and a slower response to transients. For fixed line and load conditions, higher inductance results in a lower peak current for each pulse, a lower load capability, and a higher switching frequency. The saturation level is another important parameter in choosing inductors. Note that the saturation levels specified in data sheets are maximum currents. For a dc-to-dc converter operating in PWM mode, it is the maximum peak inductor ($I_{PK}$) current that is relevant, and can be calculated using these equations:

$$I_{PK} = I_O + \frac{I_{PP}}{2}$$

where $I_O$ = output current.

This peak current varies with inductance tolerance and other errors, and the rated saturation level varies over temperature. So a sufficient design margin is required when choosing current ratings. A high-frequency core material, such as ferrite, should be chosen, the core loss could lead to serious efficiency penalties. The DCR should be kept as low as possible to reduce conduction losses.

### Input Capacitor Selection

To minimize input voltage ripple caused by the step-down conversion, and interference of large voltage spikes from other circuits, a low-ESR input capacitor is required to filter the input voltage. The input capacitor should be rated for the maximum RMS input current of:

$$I_{RMS} = I_{O.MAX} \sqrt{\frac{V_O}{V_{IN}} \left(1 - \frac{V_O}{V_{IN}}\right)}$$

It is common practice to rate for the worst-case RMS ripple that occurs when the duty cycle is at 50 %:

$$I_{RMS} = \frac{I_{O.MAX.}}{2}$$

### Output Capacitor Selection

The output capacitor affects output voltage ripple due to 2 reasons: the capacitance and the effective series resistance (ESR). The selection of the output capacitor is primarily determined by the capacitor ESR required minimizing voltage ripple and current ripple. The relationship between output ripple $\Delta V_O$, capacitance $C_O$ and its ESR is:

$$\Delta V_O = I_{PP} \cdot \left(ESR + \frac{1}{8 \cdot f \cdot C_O}\right)$$

Multiple capacitors placed in parallel may be needed to meet the ESR requirements. However if the ESR is too low it may cause stability problems.

### Control Loop Design

The SiC413CB is an integrated voltage mode buck converter. The loop stability depends on input and output voltage, output LC filter, the equivalent lumped capacitance, resistance and inductance attached to the output voltage rail beyond the LC filter. The output LC filter creates a two pole roll-off of the loop gain that makes the closed loop system inherently unstable. Therefore, a compensation network of poles and zeros must be implemented to achieve unconditional stability.

Figure 4 shows a simplified diagram of the SiC413CB buck converter control loop and the external elements that affect loop gain, phase shift and stability. In this diagram L1, C4 and C5 and R6 form a first order model of low pass filter. Resistor R6 represents the effective series resistance (ESR) of C5, which is often the case of a polymer (tantalum) capacitor. Ceramic (MLCC) capacitors are also used as denoted by C4, which has near zero ESR. To balance the performance and cost, the recommended output capacitor configuration is a combination of low cost, high capacitance polymer capacitors (C5) with ESR (R6) to add a zero to help boost phase margin and MLCC capacitors (C4) that have low ESR for achieving low voltage ripple. In practice, the lumped equivalent capacitance at the output of the filter may be a combination of many different kinds of capacitors. The characteristics of these capacitors must be considered when deriving the open loop transfer function and designing the loop compensation. It is important to have a good approximation of the lumped impedance (capacitors, resistors, ferrite beads, $\pi$ filters, etc.) tied to the rail before calculating compensation network component values.

Resistor R1 and R2 form the feedback voltage divider that samples the DC output and applies a feedback signal to the FB pin. Components C1, C2, C3, R4, R5 and the transconductance error amplifier form the loop compensation network. With voltage mode control loop the

output voltage is fed back at the FB pin. This feedback signal is summed with a precision voltage reference through a high bandwidth transconductance amplifier, often referred to as the error amplifier. This summation creates an error signal that is proportional to the difference between the actual output voltage and the desired output voltage, which is achieved when the voltage at the center tap of the feedback resistor divider is equal to the voltage reference. The error signal is present at the COMP pin, which is the output of the error amplifier.

The error amplifier in the SiC413CB has a high loop gain and a 2.5 MHz Gain Bandwidth Product. It is designed this way to provide fast transient response in applications such as DRAM memory arrays in Graphics Cards. This lets the control loop quickly respond to any deviation of the output voltage. It also makes the SiC413CB more sensitive to noise on the FB pin. It is recommended to add resistor R3 at 20 kΩ to help isolate the error amplifier from noise on the FB pin and give the designer the full benefit of the fast response time the SiC413CB can deliver.

Under normal operation the output of the error signal varies between 1.0 V and 2.0 V. This corresponds to the peak to peak amplitude of the saw-tooth wave form generated by the oscillator at the input to the PWM comparator. The PWM comparator drives the logic that controls the MOSFET gate drivers. These drivers control the turn on and turn off of the high- and low-side MOSFETs. As the error signal varies the PWM duty cycle is adjusted up and down to counteract the error. This interaction is normal load modulation and can be seen in a slight jitter on the trailing edge of the PWM signal. The resulting PWM signal at the VSW switching node is integrated by the LC filter to deliver the desired DC output voltage.

Very low steady state duty cycles occur when the desired output is much smaller than the input (i.e. 24 V input to 1.2 V output). In this case, the error signal will be closer to 1 V. Very high duty cycles occur when the desired output is closer to the input (i.e. 5 V input to 3.3 V output). In this case, the error signal is closer to 2 V. As can be seen, in these cases the error signal may have limited headroom for control under severe load transient conditions. This can result an asymmetrical transient response characteristic and slightly longer regulation recovery times for either the load acquisition or load shedding.

Open Loop Transfer Function

The following discussion derives the equations for the open loop transfer function. The technique for selecting the poles and zeros for optimized loop stability is then presented.

For this analysis we are considering the LC filter approximation given in Figure 4 and are not considering the impedance of the load. However, most output impedances can be modeled using the lumped circuit approximation shown in Figure 4. One exception is the use of a π filter with a roll off frequency that is inside the loop bandwidth. In this case, derivation of the transfer function that includes the phase and gain effects of this filter is important. In some cases, π filters can reduce gain margin and cause marginal stability if not considered thoroughly.

The loop gain transfer function is broken into four blocks, each representing a different part of the buck converter. The four blocks and their frequency domain equations are as follows:

**Block 1** - $G_{LC}$: Output LC filter consisting of L1, C4, C5 and R6

$$G_{LC} = \frac{SR6 \bullet C5 + 1}{S^3 R6 \bullet C4 \bullet C5 \bullet L1 + S^2 L1 \bullet (C4 + C5) + SR6 \bullet C5 + 1}$$

**Block 2** - $G_{SP}$: Output voltage sampling network composed of C1, R1 and R2

$$G_{SP} = \frac{S + \frac{1}{R1 \bullet C1}}{S + \frac{1}{\frac{R1 \bullet R2}{R1 + R2} \bullet C1}}$$

**Block 3** - $G_{PWM}$: PWM modulation gain that equals to $V_{IN}/\Delta V_{OSC}$, where $\Delta V_{OSC}$ = saw tooth peak to peak voltage

$$G_{PWM} = \frac{V_{IN}}{\Delta V_{OSC}}$$

**Block 4** - $G_{COMP}$: Amplifier compensator with components of C2, C3, R4, R5 and the amplifier gain $g_M$, which is a function of frequency.

$$G_{COMP} = g_M \bullet \frac{1}{C3} \bullet \frac{S + \frac{1}{R5 \bullet C2}}{S^2 + S\left(\frac{1}{R5 \bullet C2} + \frac{1}{R4 \bullet C3} + \frac{1}{R5 \bullet C3}\right) + \frac{1}{R4 \bullet R5 \bullet C2 \bullet C3}}$$

Resistor R4 value should be very large compared to R5. The purpose of R4 is to eliminate non-monotonic output behavior during rapidly pulsed off-then-on line transients. R4 provides a fast discharge path for C3 and resets the error signal at COMP to zero before the line input pulses back on. Ideally, R4 can be ignored for the purposes of the loop transfer function.

Ignoring R4 gives the following simplified transfer function for Block 4.

$$G_{COMP} = \frac{g_M}{SC3} \bullet \frac{S + \frac{1}{R5 \bullet C2}}{S + \frac{1}{R5 \bullet \frac{C2 \bullet C3}{C2 + C3}}}$$

The overall open loop transfer function for this system, $G_{OL}$, is then the product of the four transfer functions derived for each block.

$$G_{OL} = G_{LC} \bullet G_{SP} \bullet G_{PWM} \bullet G_{COMP}$$

Converting to the logarithm form we have

$$G_{OL}(dB) = G_{LC}(dB) + G_{SP}(dB) + G_{PWM}(dB) + G_{COMP}(dB)$$

Compensation Considerations

The criterion for unconditional stability of a closed loop system is that the open loop transfer function has the following attributes.

1. The magnitude of the open loop transfer function must cross through 0 dB with a slope of - 20 dB per decade
2. The phase shift of the open loop transfer function must be at least 45 at the frequency, at which the magnitude of the loop gain crosses through 0 dB
3. The phase shift should not be rapidly decreasing at loop gain slightly less than 0 dB

To determine if these criterion are met the Bode plot of the transfer function is drawn. Before drawing the bode plot, the poles and zeros need to be located. The following discussion serves as a guide to selection of the component values for the compensation network.

The compensation process begins by selecting loop bandwidth. We recommend that the 0 dB crossover frequency is set somewhere between 10 % and 20 % of switching frequency. The SiC413CB has a fixed switching frequency of 500 kHz. This means that the bandwidth of the loop can be set somewhere between 50 kHz and 100 kHz. This wide loop bandwidth, made possible by the ultra fast error amplifier in the SiC413CB, can provide excellent transient response and load regulation.

It can be seen that within the LC filter block, there are generally three poles (denoted P1, P2 and P3) and one zero (denoted Z1). The double pole (P1 and P2) created by the LC filter is the dominant response characteristic of the system. The locations of these poles and zero depend strongly on the types of capacitors used in the output filter. Three cases will be analyzed as follows.

Case 1: Output capacitors are a combination of those with ESR (C5. e.g. polymer or tantalum type) and those with no ESR or little ESR (C4. e.g. ceramic type)

The poles and zero for this case are as follows

$$f_{P1,P2} \approx \frac{1}{2\pi\sqrt{L1 \bullet (C4 + C5)}}$$

$$f_{P3} \approx \frac{1}{2\pi \bullet C4 \bullet R6}$$

$$f_{Z1} \approx \frac{1}{2\pi \bullet C5 \bullet R6}$$

To meet the above stability criterion, the frequency of the zero $f_{Z1}$ should be placed at a frequency lower than or equal to that at the double pole of $f_{P1,P2}$. Pole $f_{P3}$ should be located at a much higher frequency than $f_{P1,P2}$. This requirement sets the boundaries on the values of C4, C5 and R6. Capacitor C4 has to be much smaller than C5.

Case 2: Output capacitor is all ceramic MLCC

Ignoring C5 and R6, the poles are as follows

$$f_{P1,P2,\,MLCC} = \frac{1}{2\pi\sqrt{L1 \bullet C4}}$$

$f_{P3,\,MLCC}$ and $f_{Z1,\,MLCC}$ will not exist

This output filter configuration can be challenging because there is no zero to help boost the phase shift that is introduced by the LC double pole.

Case 3: All capacitors have ESR, no ceramics.

Ignoring C4 we have the following for the poles and zero

$$f_{P1,P2,ESR} = \frac{1}{2\pi\sqrt{L1 \bullet C5}}$$

$f_{P3,ESR}$ does not exist

$$f_{Z1,ESR} = \frac{1}{2\pi \bullet C5 \bullet R6}$$

This case is the best situation for loop compensation since no extra pole to add phase shift. The zero created with the ESR also helps reverse phase shift added by the LC filter.

In the output voltage feedback network block there is one pole (denoted P4) and one zero (denoted Z2). The locations of the pole and zero are

$$f_{P4} = \frac{1}{2\pi \bullet \frac{R1 \bullet R2}{R1 + R2} \bullet C1} = \frac{1}{2\pi \bullet C1 \bullet (R1//R2)}$$

$$f_{Z2} = \frac{1}{2\pi \bullet C1 \bullet R1}$$

In this block C1 and R1 create the zero and C1 together with the parallel combination of R1 and R2 generates the pole. Adding a capacitor in parallel with R2 is not effective here. It does not change the zero location and move the pole closer to this zero and cancels out its effect on phase margin.

From Figure 4 we can derive the DC expression for the output voltage.

$$V_O = (1 + \frac{R1}{R2}) \bullet V_{REF}$$

From this equation and the equations of the pole and zero locations, it can be seen that pole and zero locations of this block have the following relationship

$$\frac{f_{P4}}{f_{Z2}} = \frac{V_O}{V_{REF}}$$

This relationship means that when the output voltage $V_O$ is approaching the chip reference voltage, $V_{REF}$, the zero in the sampling network has diminishing effect on boosting the loop phase margin. In other words, the value if adding C1 is more apparent when the output voltage is high relative to $V_{REF}$ and becomes smaller at lower output voltages. Therefore, the use of this capacitor is optional for low voltage conversions (e.g. 1.2 V output or lower).

To make the zero $f_{Z2}$ work for compensation of the control loop it should to be placed at a frequency that is less than or equal to the frequency of the LC double pole location.

Block 3 is a DC transfer block and therefore has no pole and zero. It only affects the DC gain of open loop transfer function. This can affect phase margin as increasing the DC loop gain can increase the loop bandwidth and reduce phase margin and visa versa.

The amplifier compensation block is where the designer works hard to compensate the loop to achieve an unconditionally stable closed loop system. This block generally has two poles (denoted P5 and P6) and one zero (denoted Z3) as shown in the equation. The locations of these poles and zero are

$$f_{P5} = 0$$

$$f_{P6} = \frac{1}{2\pi \bullet R5 \bullet \frac{C2 \bullet C3}{C2 + C3}}$$

$$f_{Z3} = \frac{1}{2\pi \bullet R5 \bullet C2}$$

To make the zero $f_{Z3}$ and pole $f_{P6}$ work for increasing phase margin the zero should be placed at a frequency lower than and the pole much higher than the LC double pole frequency. In general, as soon as the output LC filter is determined, the dominant double pole is fixed. Then the compensation design will be a "try and use" process based on above theory. Usually a network analyzer is used to confirm the loop stability. To make a control system stable the solution is infinite, meaning there are lots of combinations of C1, C2, C3, R1, R4 and R5 that can make the system stable. But a designer's job is to find the optimized one that both makes the system stable and has the best transient response.

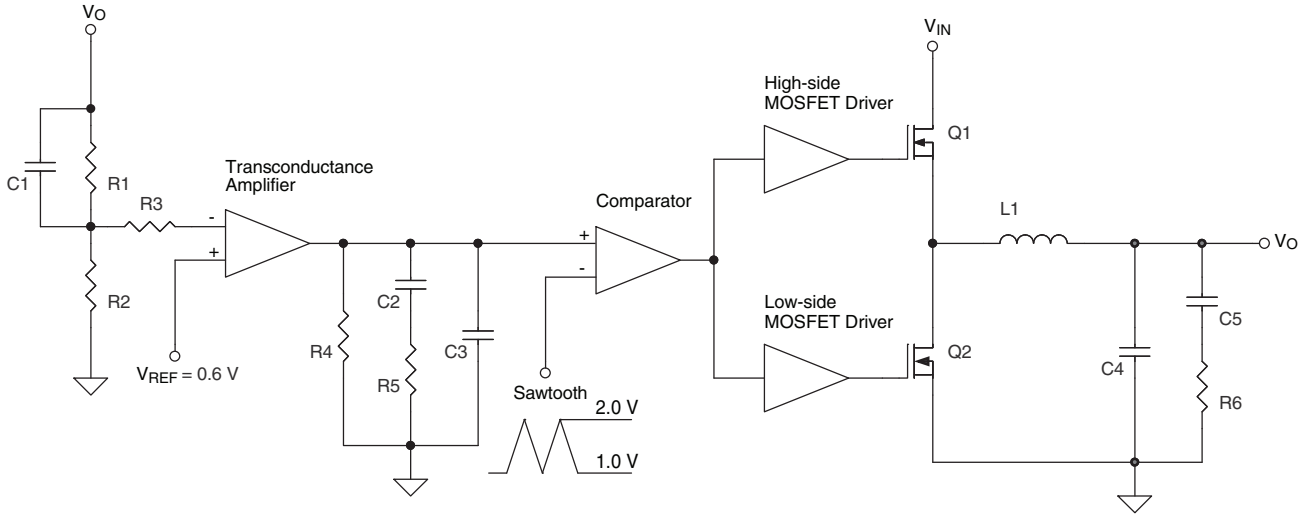



**Figure 4. Control and Compensation Network**

**PCB Layout**

As in the design of any switching dc-to-dc converter, a good PCB layout ensures successful transition from design to production. One of a few drawbacks of switching converters is the noise generated by the high frequency switching and coupled by parasitic inductance and capacitance. However, noise levels can be reduced or minimized if a PCB is well laid out.

The following is a guidance on SiC413 layout.

Input Capacitors: C1 through to C6 are the input capacitors. They are placed side by side together to form a block and this block sits right beside SiC413's $V_{IN}$ and GND pins. This placement minimizes the distance between $V_{IN}$ pin, capacitors and chip's ground, which minimizes the possibility of noise injected in $V_{IN}$ pin.

Also the MLCC with smallest value (0.01 µF) is placed closest to $V_{IN}$ pin, and then MLCC with larger values (0.1 µF, 10 µF) and the last, the electrolytic. This is because their ESRs are getting larger and larger from small value MLCC to large value MLCC and then electrolytic capacitor.

Output Capacitors: C17 through to C20 are the output capacitors. They are placed the same way as input capacitors.

Decoupling Capacitors of $V_{REG}$: C7 and C8, are placed right beside GND pin on their negative sides. Their positive sides are connected to the chip's $V_{REG}$ pin through two vias from the bottom of the PCB. The trace distance should be kept less than 10 mm.

Boot Capacitor: C14 is the boot capacitor. R5 is added to allow flexibility for adjusting the high-side MOSFET driving current to reduce possible noise.

Compensation Network: C9, C10, R6 and R10 form this network. These components should be placed in a tight group. This group then should be in close proximity to the COMP pin. Trace lengths between the components should be minimized.

Output Sampling Network: R7, C15, R9 and R11 constitute the output voltage sampling network. These components should be placed in a tight grouping and in close proximity to the FB pin. Since SiC413 has only one GND pin, this makes the chip more sensitive to noise coming from GND. Therefore R11 is added to perform as a filter to remove any possible noise from ground.

Grounding: Separate analog and power ground paths are recommended for optimal noise reduction in the SiC413CB converter. These grounds should both be connected at the GND pin. Connect the ground pin of the input and output capacitors to the power ground. Connect the ground pin for the $V_{REG}$ decoupling caps, the compensation network grounds, and the output voltage sampling network grounds to the analog ground. It is preferred to use low inductance ground planes when ever possible. If single sided board is being used then try to keep the ground traces short and going a star configuration at the GND pin.

Power Traces: The power path is formed starting at VIN. It then branches to $P_{GND}$ and $V_{SW}$ to $V_{OUT}$. The trace thickness for the power path should be kept to a minimum of 50 mils. Placement of components should focus on keeping these traces as short as possible to minimize parasitic inductance and resistances. They have minimum 50 mil trace width (at the $V_{IN}$ pin area) and this segment is very short, which is good enough for the power level handled by this chip.

Figure 6 and Figure 7 below show a recommended board layout for converters using SiC413CB.

### SIC413 SCHEMATIC FOR THE SUGGESTED PCB LAYOUT

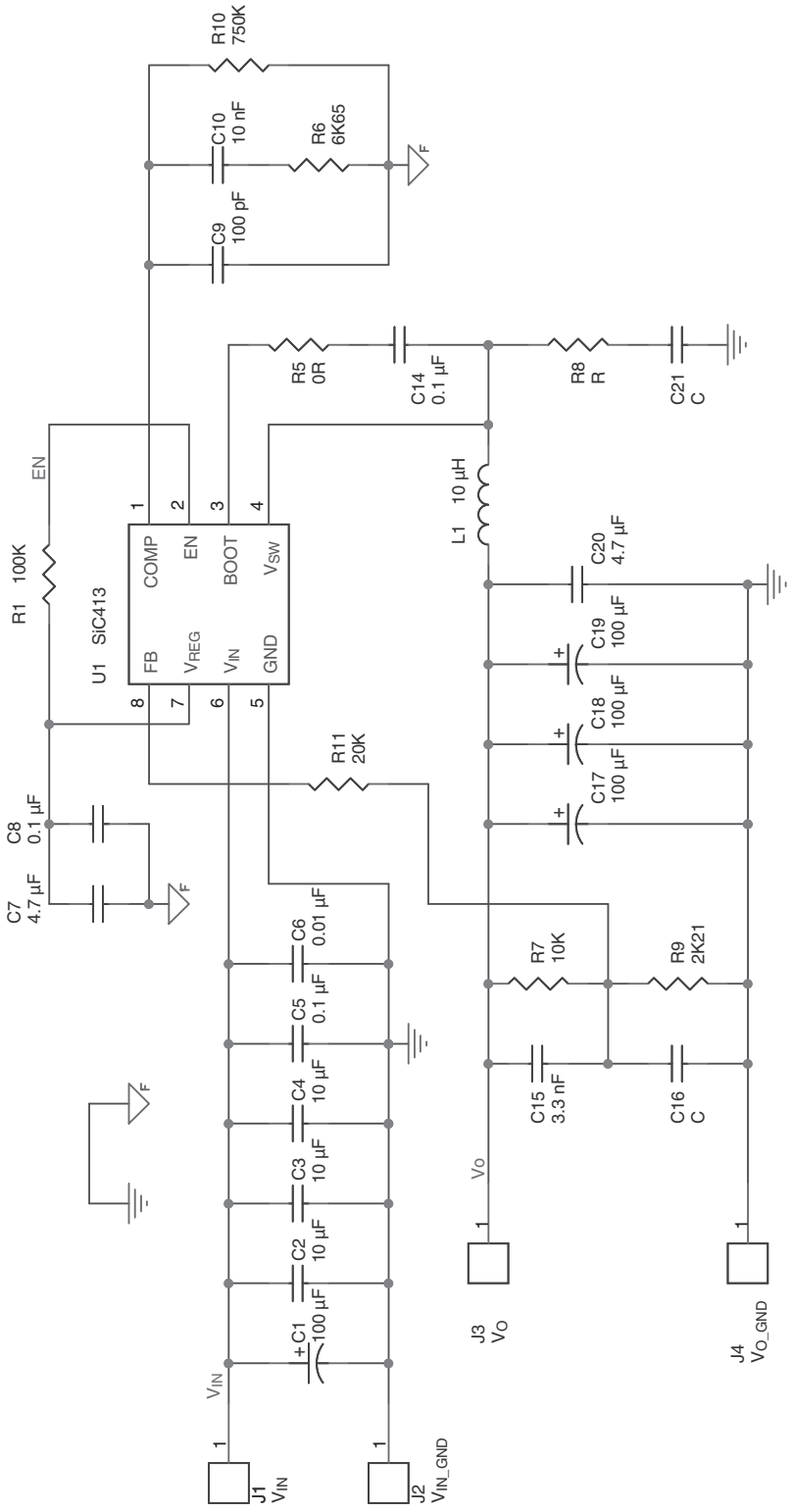



**Figure 5. Reference Board Schematic**

## SUGGESTED PCB LAYOUT

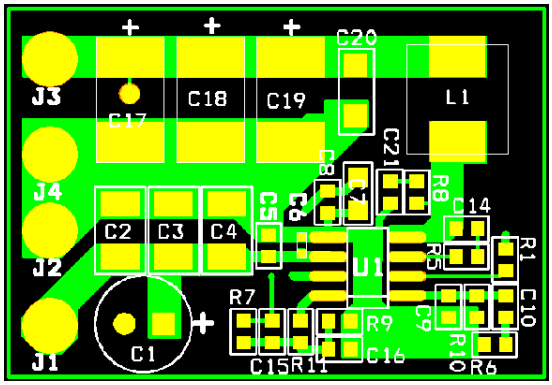



Figure 6. PCB Layout - Top Layer

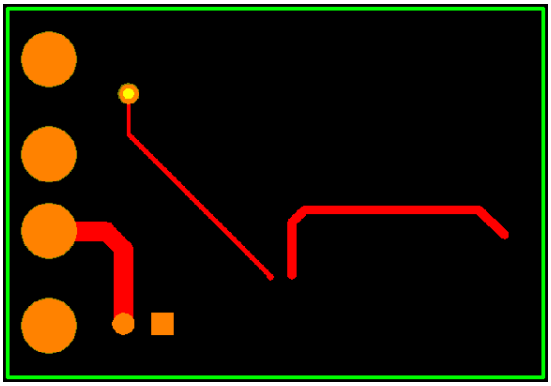


Figure 7. PCB Layout - Bottom Layer

**BILL OF MATERIALS FOR THE SUGGESTED PCB LAYOUT** $V_{IN}$ = 12 V, $V_{OUT}$ = 3.3 V

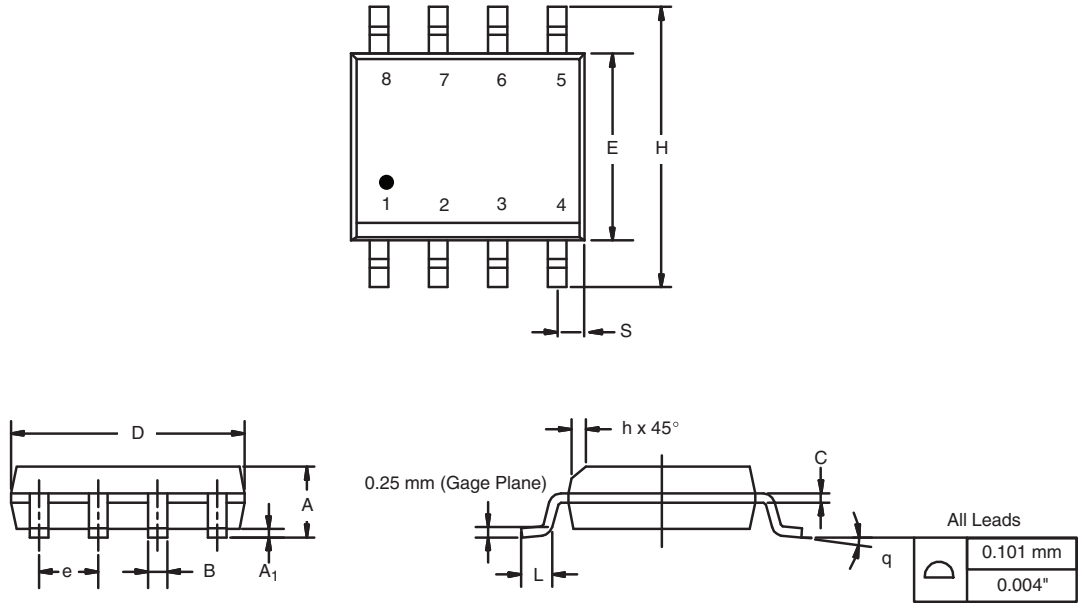
| Item | QTY | Reference | Part | Voltage | PCB Footprint | Part Number | Manufacturer |
|---|---|---|---|---|---|---|---|
| 1 | 1 | C1 | 100 µF | 35 V | D6.3X11.2-D0.6X2.5 | ECA-1VHG101I | Panasonic |
| 2 | 3 | C2, C3, C4 | 10 µF | 25 V | SM/C_1210 | TMK325B7106MN-T | Taiyo Yuden |
| 3 | 3 | C5, C8, C14 | 0.1 µF | 50 V | SM/C_0603 | VJ0603Y104KXACW1BC | Vishay |
| 4 | 1 | C6 | 0.01 µF | 50 V | SM/C_0402 | VJ0402Y103KXACW1BC | Vishay |
| 5 | 1 | C7 | 4.7 µF | 10 V | SM/C_0805 | LMK212B7475KG-T | Taiyo Yuden |
| 6 | 1 | C9 | 100 pF | 50 V | SM/C_0603 | VJ0603Y102KXACW1BC | Vishay |
| 7 | 2 | C10, C15 | 3.3 nF | 50 V | SM/C_0603 | VJ0603Y333KXACW1BC | Vishay |
| 8 | 2 | C16, C21 | Not populated | 50 V | SM/C_0603 | | Vishay |
| 9 | 1 | C17 | 100 µF | 20 V | 595D-D | 595D107X9020D2T | Vishay |
| 10 | 2 | C18, C19 | 100 µF | 20 V | 595D-D | 595D107X9020D2T | Vishay |
| 11 | 1 | C20 | 4.7 µF | 16 V | SM/C_1206 | C3216X7R1C106M | TDK |
| 12 | 1 | J1 | $V_{IN}$ | | Probe Hook | 1540-2 | Keystone |
| 13 | 1 | J2 | $V_{IN\_GND}$ | | Probe Hook | 1540-2 | Keystone |
| 14 | 1 | J3 | $V_O$ | | Probe Hook | 1540-2 | Keystone |
| 15 | 1 | J4 | $V_{O\_GND}$ | | Probe Hook | 1540-2 | Keystone |
| 16 | 1 | L1 | 10 µH | | IHLP2525 | IHLP2525EZER100M01 | Vishay |
| 17 | 1 | R1 | 100K | 50 V | SM/C_0603 | CRCW0603100KFKEA | Vishay |
| 18 | 1 | R5 | 0R | 50 V | SM/C_0603 | CRCW06030000FKEA | Vishay |
| 19 | 1 | R6 | 6K65 | 50 V | SM/C_0603 | CRCW06036K65FKEA | Vishay |
| 20 | 1 | R7 | 10K | 50 V | SM/C_0603 | CRCW060310K0FKEA | Vishay |
| 21 | 1 | R8 | Not populated | 50 V | SM/C_0603 | | Vishay |
| 22 | 1 | R9 | 2K21 | 50 V | SM/C_0603 | CRCW06032K21FKEA | Vishay |
| 23 | 1 | R10 | 750K | 50 V | SM/C_0603 | CRCW0603750KFKEA | Vishay |
| 24 | 1 | R11 | 20K | 50V | SM/C_0603 | CRCW060320K0FKEA | Vishay |
| 25 | 1 | U1 | SiC413 | | SO-8 | SiC413 | Vishay |

# SiC413

Vishay Siliconix

## PACKAGE DIMENSIONS

**SOIC (NARROW): 8-LEAD**
JEDEC Part Number: MS-012




| DIM. | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| | Min. | Max. | Min. | Max. |
| A | 1.35 | 1.75 | 0.053 | 0.069 |
| $A_1$ | 0.10 | 0.20 | 0.004 | 0.008 |
| B | 0.35 | 0.51 | 0.014 | 0.020 |
| C | 0.19 | 0.25 | 0.0075 | 0.010 |
| D | 4.80 | 5.00 | 0.189 | 0.196 |
| E | 3.80 | 4.00 | 0.150 | 0.157 |
| e | 1.27 BSC | | 0.050 BSC | |
| H | 5.80 | 6.20 | 0.228 | 0.244 |
| h | 0.25 | 0.50 | 0.010 | 0.020 |
| L | 0.50 | 0.93 | 0.020 | 0.037 |
| q | 0° | 8° | 0° | 8° |
| S | 0.44 | 0.64 | 0.018 | 0.026 |
| ECN: C-06527-Rev. I, 11-Sep-06<br>DWG: 5498 | | | | |

**Figure 10. SO-8 dimensions**

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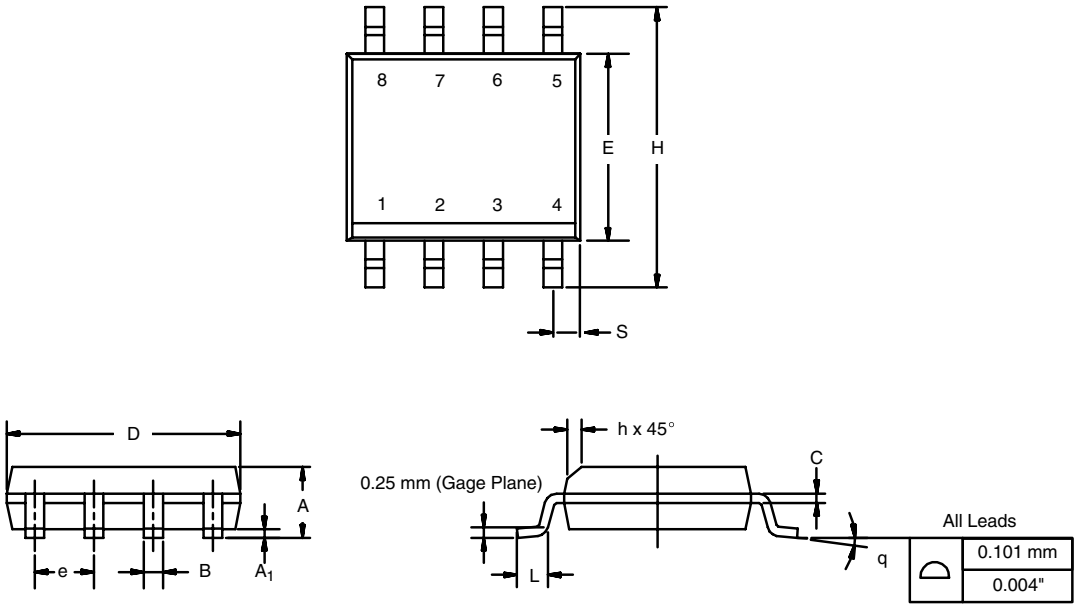
# Package Information

Vishay Siliconix

**SOIC (NARROW): 8-LEAD**

JEDEC Part Number: MS-012




| DIM | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
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| e | 1.27 BSC | | 0.050 BSC | |
| H | 5.80 | 6.20 | 0.228 | 0.244 |
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| S | 0.44 | 0.64 | 0.018 | 0.026 |
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