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SIC417CD-T1-E3

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microBUCK™ SiC417

10-A, 28-V Integrated Buck Regulator with Programmable LDO

DESCRIPTION

The Vishay Siliconix SiC417 is an advanced stand-alone synchronous buck regulator featuring integrated power MOSFETs, bootstrap diode, and a programmable LDO in a space-saving MLPQ 5 x 5 - 32 pin package.

The SiC417 is capable of operating with all ceramic solutions and switching frequencies up to 1 MHz. The programmable frequency, synchronous operation and selectable power-save allow operation at high efficiency across the full range of load current. The internal programmable LDO may be used to supply 5 V for the gate drive circuits or it may be bypassed with an external 5 V for optimum efficiency and used to drive external N-channel MOSFETs or other loads. Additional features include cycle-by-cycle current limit, voltage soft-start, under-voltage protection, programmable over-current protection, soft shutdown and selectable power-save. The Vishay Siliconix SiC417 also provides an enable input and a power good output.

PRODUCT SUMMARY	
Input Voltage Range	3 V to 28 V
Output Voltage Range	0.5 V to 5.5 V
Operating Frequency	200 kHz to 1 MHz
Continuous Output Current	10 A
Peak Efficiency	95 % at 300 kHz
Package	MLPQ 5 mm x 5 mm

FEATURES

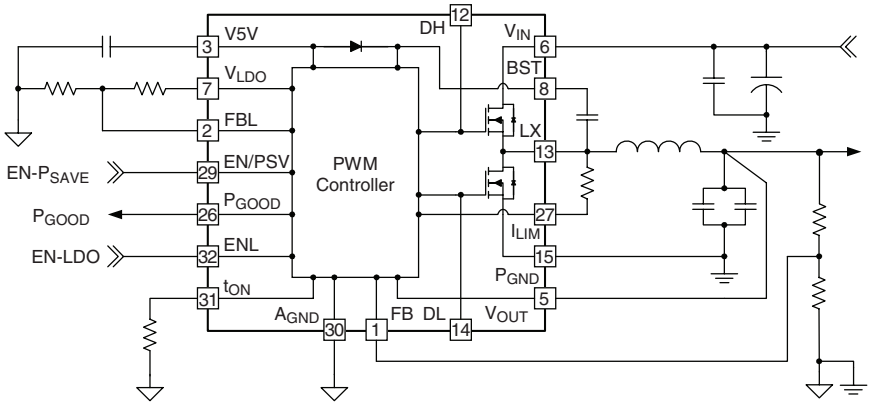
- High efficiency > 92 %
- Internal power MOSFETs:
  - High-side $R_{DS(ON)}$ = 27 mΩ
  - Low-side $R_{DS(ON)}$ = 9 mΩ
- Integrated bootstrap diode
- Integrated configurable 150 mA LDO with bypass logic
- Temperature compensated current limit
- Pseudo fixed-frequency adaptive on-time control
- All ceramic solution enabled
- Programmable input UVLO threshold
- Independent enable pin for switcher and LDO
- Selectable ultra-sonic power-save mode
- Internal soft-start and soft-shutdown
- 1 % internal reference voltage
- Power good output and over voltage protection
- **Halogen-free according to IEC 61249-2-21 definition**
- **Compliant to RoHS directive 2002/95/EC**

Pb-free
RoHS COMPLIANT
HALOGEN FREE

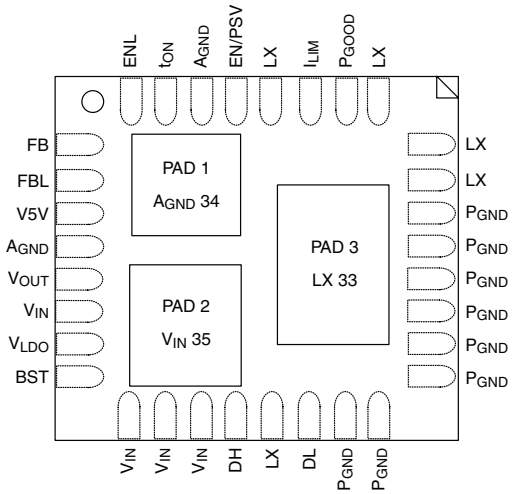
APPLICATIONS

- Notebook, desktop and server computers
- Digital HDTV and digital consumer applications
- Networking and telecommunication equipment
- Printers, DSL and STB applications
- Embedded applications
- Point of load power supplies

TYPICAL APPLICATION CIRCUIT



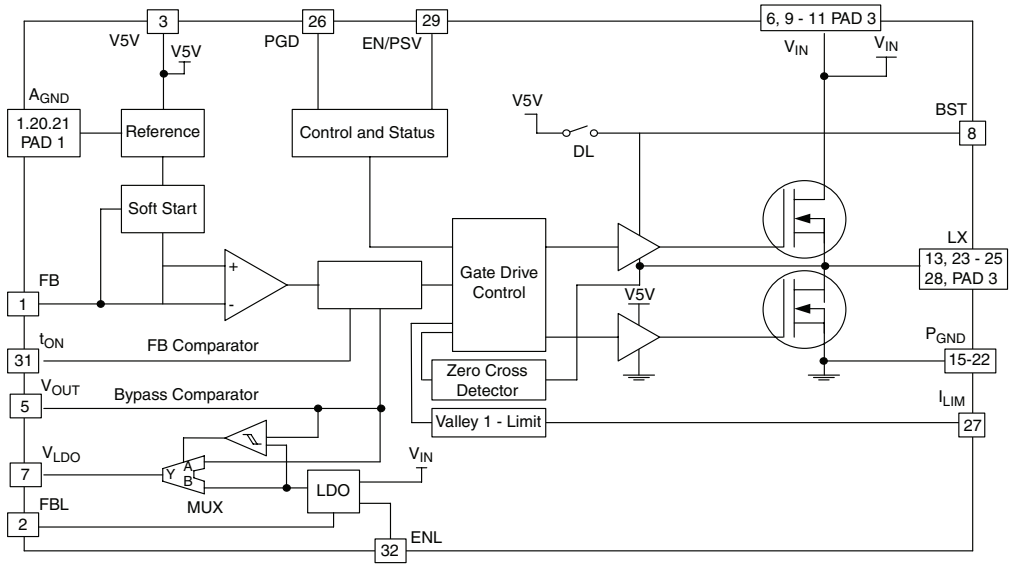
PIN CONFIGURATION



PIN DESCRIPTION		
Pin Number	**Symbol**	**Description**
1	FB	Feedback input for switching regulator. Connect to an external resistor divider from output to program the output voltage.
2	FBL	Feedback input for the LDO. Connect to an external resistor divider from V_{LDO} to program the V_{LDO} output.
3	V5V	5 V power input for internal analog circuits and gate drives. Connect to external 5 V supply or configure the LDO for 5 V and connect to V_{LDO}.
4, 30, PAD 1	A_{GND}	Analog ground.
5	V_{OUT}	Output voltage input to the SiC417. Additionally, may be used to bypass LDO to supply V_{LDO} directly.
6, 9 - 11, PAD 2	V_{IN}	Input supply voltage.
7	V_{LDO}	LDO output.
8	BST	Bootstrap pin. A capacitor is connected between BST to LX to develop the floating voltage for the high-side gate drive.
12	DH	High-side gate drive - do not connect this pin.
14	DL	Low-side gate drive - do not connect this pin.
13, 23 - 25, 28, PAD 3	LX	Switching (Phase) node.
15-22	P_{GND}	Power ground.
26	P_{GOOD}	Open-drain power good indicator. High impedance indicates power is good. An external pull-up resistor is required.
27	I_{LIM}	Current limit sense point - to program the current limit connect a resistor from I_{LIM} to LX.
29	EN/PSV	Tri-state pin. Enable input for switching regulator. Connect EN to A_{GND} to disable the switching regulator. Float pin for forced continuous and pull high for power-save mode.
31	t_{ON}	On-time set input. Set the on-time by a series resistor to the input supply voltage.
32	ENL	Enable input for the LDO. Connect ENL to A_{GND} to disable the LDO.

ORDERING INFORMATION	
Part Number	**Package**
SiC417CD-T1-E3	MLPQ55-32
SiC417DB	Evaluation board

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS T_A = 25 °C, unless otherwise noted				
Parameter	**Symbol**	**Min.**	**Max.**	**Unit**
LX to P_{GND} Voltage	V_{LX}	- 0.3	+ 30	V
LX to P_{GND} Voltage (transient - 100 ns)	V_{LX}	- 2	+ 30	
V_{IN} to P_{GND} Voltage	V_{IN}	- 0.3	+ 30	
V_{EN} Maximum Voltage	V_{EN}	- 0.3	V_{IN}	
BST Bootstrap to LX; V5V to P_{GND}		- 0.3	+ 6.0	
A_{GND} to P_{GND}	V_{AG-PG}	- 0.3	+ 0.3	
EN/PSV, P_{GOOD}, I_{LIM}, V_{OUT}, V_{LDO}, FB, FBL to GND		- 0.3	+ (V5V + 0.3)	
t_{ON} to P_{GND}		- 0.3	+ (V5V - 1.5)	
BST to P_{GND}		- 0.3	+ 35	

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating/conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS					
Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Unit**
Input Voltage	V_{IN}	3.0		28	V
V5V to P_{GND}	V5V	4.5		5.5	
V_{OUT} to P_{GND}	V_{OUT}	0.5		5.5	

Note:
For proper operation, the device should be used within the recommended conditions.

THERMAL RESISTANCE RATINGS					
Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Unit**
Storage Temperature	T_{STG}	- 40		+ 150	°C
Maximum Junction Temperature	T_J	-		150	
Operation Junction Temperature	T_J	- 25		+ 125	

THERMAL RESISTANCE RATINGS					
Thermal Resistance, Junction-to-Ambient[b] High-Side MOSFET Low-Side MOSFET PWM Controller and LDO Thermal Resistance			25 20 50		°C/W
Peak IR Reflow Temperature	T_{Reflow}	-		260	°C

Notes:
a. This device is ESD sensitive. Use of standard ESD handling precautions is required.
b. Calculated from package in still air, mounted to 3 x 4.5 (in), 4 layer FR4 PCB with thermal vias under the exposed pad per JESD51 standards.

Exceeding the above specifications may result in permanent damage to the device or device malfunction. Operation outside of the parameters specifiifed in the Electrical Characteristicsw section is not recommended.

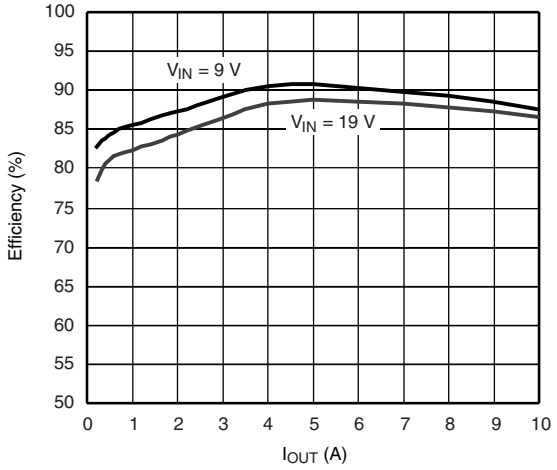
ELECTRICAL SPECIFICATIONS						
Parameter	**Symbol**	**Test Conditions Unless Specified** V_{IN} = 12 V, V5V = 5 V, T_A = + 25 °C for typ., - 25 °C to + 85 °C for min. and max., T_J = < 125 °C	**Min.**	**Typ.**	**Max.**	**Unit**
Input Supplies						
V_{IN} Input Voltage	V_{IN}		3		28	V
V5V Voltage	V5V		4.5		5.5	
V_{IN} UVLO Threshold Voltage[a]	V_{IN_UV+}	Sensed at ENL pin, rising edge	2.4	2.6	2.95	
	V_{IN_UV-}	Sensed at ENL pin, falling edge	2.235	2.4	2.565	
V_{IN} UVLO Hysteresis	$V_{IN\_UV\_HY}$	EN/PSV = High		0.2		
V5V UVLO Threshold Voltage	V_{5V_UV+}	Measured at V5V pin, rising edge	3.7	3.9	4.1	
	V_{5V_UV-}	Measured at V5V pin, falling edge	3.5	3.6	3.75	
V5V UVLO Hysteresis	$V_{5V\_UV\_HY}$			0.3		
V_{IN} Supply Current	I_{IN}	EN/PSV, ENL = 0 V, V_{IN} = 28 V		8.5	20	µA
		Standby mode: ENL = V5V, EN/PSV = 0 V		130		
V5V Supply Current	I_{5V}	EN/PSV, ENL = 0 V		3	7	
		EN/PSV = V5V, no load (f_{SW} = 25 kHz), V_{FB} > 500 mV[b]		2		mA
		f_{SW} = 250 kHz, EN/PSV = floating, no load[b]		10		
Controller						
F_B On-Time Threshold	V_{FB-TH}	Static V_{IN} and load, - 40 °C to + 85 °C	0.495	0.5	0.505	V
Frequency Range	F_{PWM}	continuous mode	200		1000	kHz
Bootstrap Switch Resistance				10		Ω
Timing						
On-Time	t_{ON}	Continuous mode operation V_{IN} = 15 V, V_{OUT} = 5 V, f_{SW} = 300 kHz, R_{ton} = 133 kΩ	999	1110	1220	ns
Minimum On-Time[b]	t_{ON}			50		
Minimum Off-Time[b]	t_{OFF}			250		
Soft Start						
Soft Start Time[b]	t_{SS}	$I_{OUT} = I_{LIM}/2$		0.85		ms
Analog Inputs/Outputs						
V_{OUT} Input Resistance	R_{O-IN}			500		kΩ
Current Sense						
Zero-Crossing Detector Threshold Voltage	$V_{Sense-th}$	$LX-P_{GND}$	- 3	0	+ 3	mV
Power Good						
Power Good Threshold Voltage	PG_V_{TH}	Internal reference 500 mV	- 10 %		+ 20 %	V
Start-Up Delay Time	PG_T_d	V_{EN} = 0 V		2		ms
Fault (noise-immunity) Delay Time[b]	PG_I_{CC}	V_{EN} = 0 V		5		µs
Power Good Leakage Current	PG_I_{LK}	V_{EN} = 0 V			1	µA
Power Good On-Resistance	PG_R_{DS-ON}	V_{EN} = 0 V		10		Ω

ELECTRICAL SPECIFICATIONS

Parameter	Symbol	Test Conditions Unless Specified V_{IN} = 12 V, V5V = 5 V, T_A = + 25 °C for typ., - 25 °C to + 85 °C for min. and max., T_J = < 125 °C	Min.	Typ.	Max.	Unit
Fault Protection						
I_{LIM} Source Current	I_{LIM}			10		µA
Valley Current Limit		R_{ILIM} = 5.9 kΩ	6	8	10	A
I_{LIM} Comparator Offset Voltage	V_{ILM-LK}	With respect to A_{GND}	- 10	0	+ 10	mV
Output Under-Voltage Fault	V_{OUV_Fault}	V_{FB} with respect to Internal 500 mV reference, 8 consecutive clocks		- 25		%
Smart Power-Save Protection Threshold Voltage[b]	P_{SAVE_VTH}	V_{FB} with respect to internal 500 mV reference		+ 10		%
Over-Voltage Protection Threshold		V_{FB} with respect to internal 500 mV reference		+ 20		
Over-Voltage Fault Delay[b]	$t_{OV-Delay}$			5		µs
Over Temperature Shutdown[b]	T_{Shut}	10 °C hysteresis		150		°C
Logic Inputs/Outputs						
Logic Input High Voltage	V_{IN+}	EN, ENL, PSV	2			V
Logic Input Low Voltage	V_{IN-}				0.4	
EN/PSV Input Bias Current	I_{EN-}	EN/PSV = V5V or A_{GND}	- 10		+ 10	µA
ENL Input Bias Current		V_{IN} = 28 V		11	18	
FBL, FB Input Bias Current	FBL_I_{LK}	FBL, FB = V5V or A_{GND}	- 1		+ 1	
Linear Dropout Regulator						
FBL Accuracy	FBL_{ACC}	V_{LDO} load = 10 mA	0.735	0.75	0.765	V
LDO Current Limit	LDO_I_{LIM}	Start-up and foldback, V_{IN} = 12 V		85		mA
		Operating current limit, V_{IN} = 12 V	135	200		
V_{LDO} to V_{OUT} Switch-Over Threshold[c]	$V_{LDO-BPS}$		- 140		+ 140	mV
V_{LDO} to V_{OUT} Non-Switch-Over Threshold[c]	$V_{LDO-NBPS}$		- 450		+ 450	
V_{LDO} to V_{OUT} Switch-Over Resistance	R_{LDO}	V_{OUT} = 5 V		2		Ω
LDO Drop Out Voltage[d]		From V_{IN} to V_{VLDO}, V_{VLDO} = + 5 V, I_{VLDO} = 100 mA		1.2		V

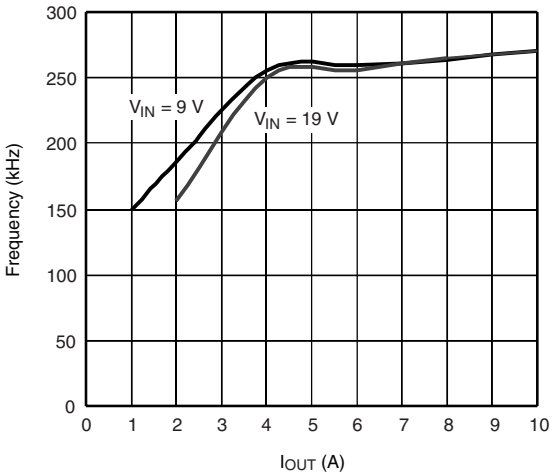
Notes:
a. $V_{IN\ UVLO}$ is programmable using a resistor divider from V_{IN} to ENL to A_{GND}. The ENL voltage is compared to an internal reference.
b. Guaranteed by design.
c. The switch-over threshold is the maximum voltage diff erential between the V_{LDO} and V_{OUT} pins which ensures that V_{LDO} will internally switch-over to V_{OUT}. The non-switch-over threshold is the minimum voltage diff erential between the V_{LDO} and V_{OUT} pins which ensures that V_{LDO} will not switch-over to V_{OUT}.
d. The LDO drop out voltage is the voltage at which the LDO output drops 2 % below the nominal regulation point.

ELECTRICAL CHARACTERISTICS

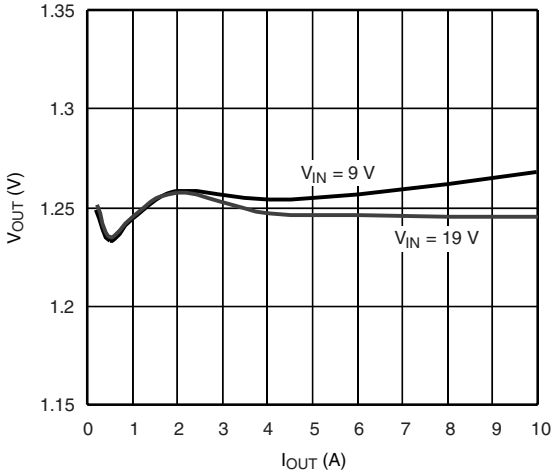


Efficiency vs. Output Current (V_{OUT} = 1.2 V)

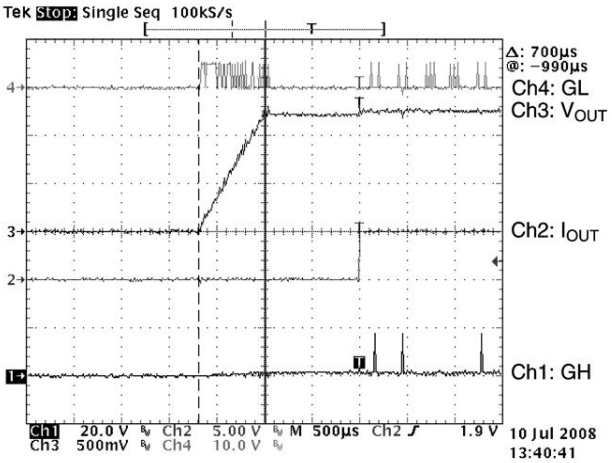
ELECTRICAL CHARACTERISTICS



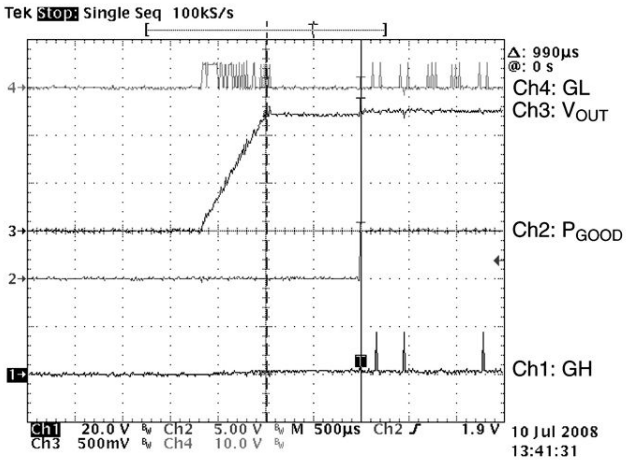
Frequency vs. I_{OUT}, (V_{OUT} = 1.2 V)



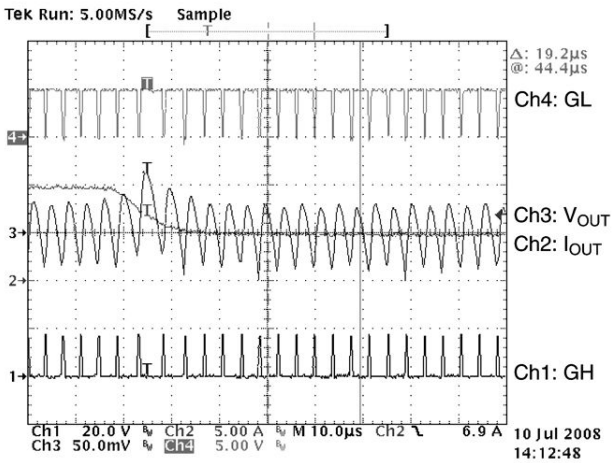
Load Regulation, (V_{OUT} = 1.2 V)



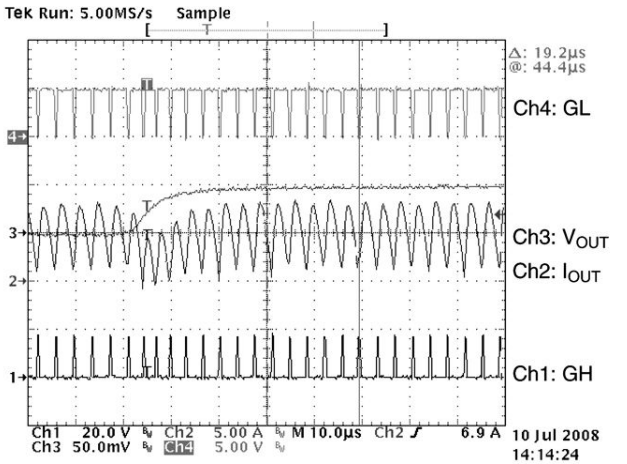
Start up Time: V_{IN} = 12 V, V_{OUT} = 1.2 V, I_{OUT} = 0 A



P_{GOOD} Delay after Start up Time: V_{IN} = 12 V, V_{OUT} = 1.2 V, I_{OUT} = 0 A

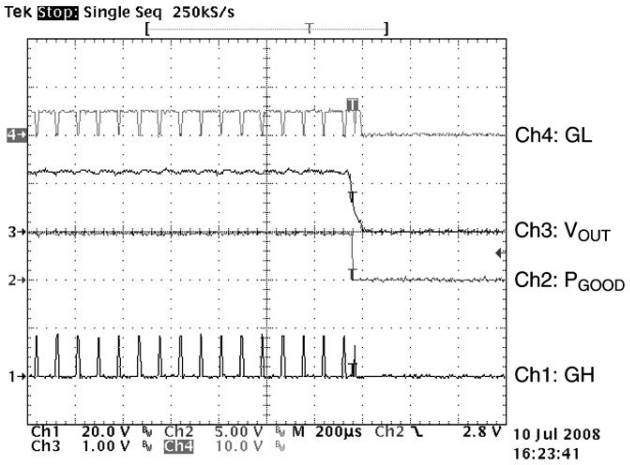


Transient Response: V_{IN} = 12 V, V_{OUT} = 1.2 V, I_{OUT} = 10 A to 5 A, dI/dt = 0.5 A/µs

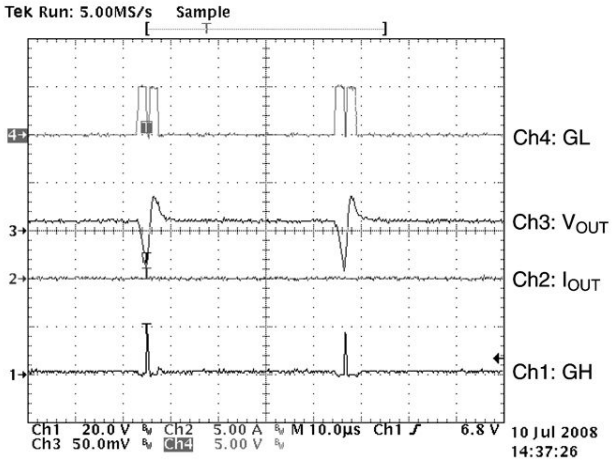


Transient Response: V_{IN} = 12 V, V_{OUT} = 1.2 V, I_{OUT} = 5 A to 10 A, dI/dt = 0.5 A/µs

ELECTRICAL CHARACTERISTICS



Over Current Protection: V_{IN} = 12 V, V_{OUT} = 1.2 V



Ultra-Sonic Power-Save at I_{OUT} = 0 A

APPLICATIONS INFORMATION

SiC417 Synchronous Buck Converter

The SiC417 is a step down synchronous buck dc-to-dc converter with integrated power FETs and programmable LDO. The SiC417 is capable of 10 A operation at very high efficiency in a tiny 5 mm x 5 mm - 32 pin package. The programmable operating frequency range of 200 kHz to 1 MHz, enables the user to optimize the solution for minimum board space and optimum efficiency.

The buck controller employs pseudo-fixed frequency adaptive on-time control. This control scheme allows fast transient response thereby lowering the size of the power components used in the system.

Input Voltage Range

The SiC417 requires two input supplies for normal operation: V_{IN} and V5V. V_{IN} operates over the wide range from 3 V to 28 V. V5V requires a 5 V supply input that can be an external source or the internal LDO configured to supply 5 V. When V_{IN} is less than ~ 6 V then an external 5 V supply must be tied to V5V.

Pseudo-Fixed Frequency Adaptive On-Time Control

The PWM control method used for the SiC417 is pseudo-fixed frequency, adaptive on-time, as shown in figure 1. The ripple voltage generated at the output capacitor ESR is used as a PWM ramp signal. This ripple is used to trigger the on-time of the controller.

The adaptive on-time is determined by an internal oneshot timer. When the one-shot is triggered by the output ripple, the device sends a single on-time pulse to the highside MOSFET. The pulse period is determined by V_{OUT} and V_{IN}; the period is proportional to output voltage and inversely proportional to input voltage. With this adaptive on-time arrangement, the device automatically anticipates the on-time needed to regulate V_{OUT} for the present V_{IN} condition and at the selected frequency.

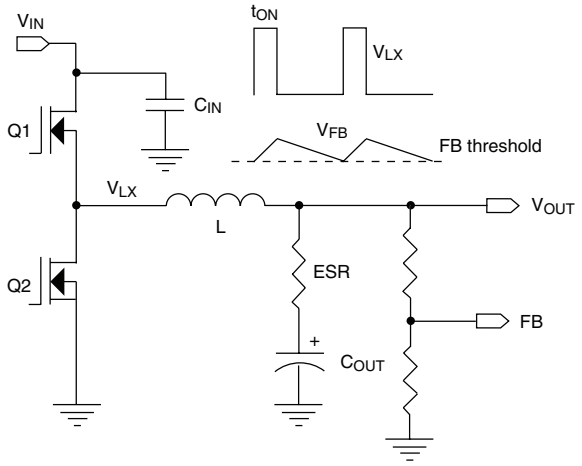


Figure 1 - Output Ripple and PWM Control Method

The adaptive on-time control has significant advantages over traditional control methods used in the controllers today.

- Reduced component count by eliminating DCR sense or current sense resistor as no need of a sensing inductor current.
- Reduced Saves external components used for compensation by eliminating the no error amplifier and other components.
- Ultra fast transient response because of fast loop, absence of error amplifier speeds up the transient response.
- Predictable frequency spread because of constant on-time architecture.
- Fast transient response enables operation with minimum output capacitance

Overall, superior performance compared to fixed frequency architectures.

On-Time One-Shot Generator (t_{ON}) and Operating Frequency

The SiC417 have an internal on-time one-shot generator which is a comparator that has two inputs. The FB Comparator output goes high when VFB is less than the internal 500 mV reference. This feeds into the gate drive and turns on the high-side MOSFET, and also starts the one-shot timer. The one-shot timer uses an internal comparator and a capacitor. One comparator input is connected to V_{OUT}, the other input is connected to the capacitor. When the on-time begins, the internal capacitor charges from zero volts through a current which is proportional to V_{IN}. When the capacitor voltage reaches V_{OUT}, the on-time is completed and the high-side MOSFET turns off. The figure 2 shows the on-chip implementation of on-time generation.

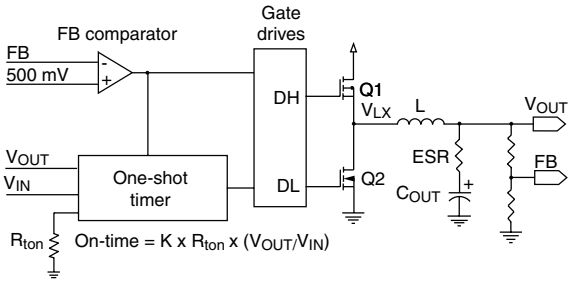


Figure 2 - On-Time Generation

This method automatically produces an on-time that is proportional to V_{OUT} and inversely proportional to V_{IN}. Under steady-state conditions, the switching frequency can be determined from the on-time by the following equation.

$$f_{SW} = \frac{V_{OUT}}{t_{ON} \times V_{IN}}$$

The SiC417 uses an external resistor to set the ontime which indirectly sets the frequency. The on-time can be programmed to provide operating frequency from 200 kHz to 1 MHz using a resistor between the t_{ON} pin and ground. The resistor value is selected by the following equation.

$$R_{ton} = \frac{(t_{ON} - 10\ ns) \times V_{IN}}{25\ pF \times V_{OUT}}$$

The maximum R_{TON} value allowed is shown by the following equation.

$$R_{ton\_MAX} = \frac{V_{IN\_MIN}}{15\ \mu A}$$

V_{OUT} Voltage Selection

The switcher output voltage is regulated by comparing V_{OUT} as seen through a resistor divider at the FB pin to the internal 500 mV reference voltage, see figure 3.

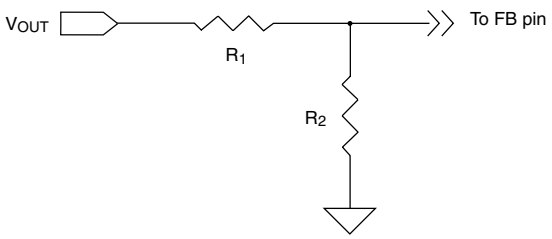


Figure 3 - Output Voltage Selection

As the control method regulates the valley of the output ripple voltage, the DC output voltage V_{OUT} is off set by the output ripple according to the following equation.

$$V_{OUT} = 0.5 \times (1 + R_1/R_2) + V_{RIPPLE}/2$$

Enable and Power-Save Inputs

The EN/PSV and ENL inputs are used to enable or disable the switching regulator and the LDO.

When EN/PSV is low (grounded), the switching regulator is off and in its lowest power state. When off, the output of the switching regulator soft-discharges the output into a 15 Ω internal resistor via the V_{OUT} pin.

When EN/PSV is allowed to float, the pin voltage will fl oat to 1.5 V. The switching regulator turns on with power-save disabled and all switching is in forced continuous mode.

When EN/PSV is high (above 2.0 V), the switching regulator turns on with ultra-sonic power-save enabled. The SiC417 ultra-sonic power-save operation maintains a minimum switching frequency of 25 kHz, for applications with stringent audio requirements.

The ENL input is used to control the internal LDO. This input serves a second function by acting as a $V_{IN\ UVLO}$ sensor for the switching regulator.

The LDO is off when ENL is low (grounded). When ENL is a logic high but below the $V_{IN\ UVLO}$ threshold (2.6 V typical), then the LDO is on and the switcher is off. When ENL is above the $V_{IN\ UVLO}$ threshold, the LDO is enabled and the switcher is also enabled if the EN/PSV pin is not grounded.

Forced Continuous Mode Operation

The SiC417 operates the switcher in Forced Continuous Mode (FCM) by floating the EN/PSV pin (see figure 4). In this mode one of the power MOSFETs is always on, with no intentional dead time other than to avoid cross-conduction. This feature results in uniform frequency across the full load range with the trade-off being poor efficiency at light loads due to the high-frequency switching of the MOSFETs.

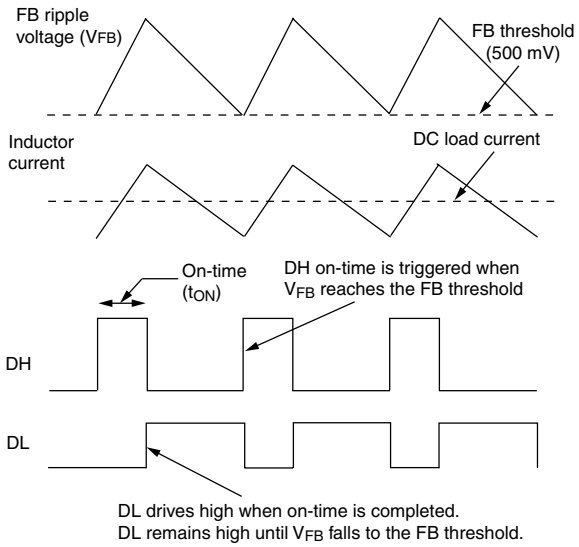


Figure 4 - Forced Continuous Mode Operation

Ultrasonic Power-Save Operation

The SiC417 provides ultra-sonic power-save operation at light loads, with the minimum operating frequency fixed at 25 kHz. This is accomplished using an internal timer that monitors the time between consecutive high-side gate pulses.

If the time exceeds 40 µs, DL drives high to turn the low-side MOSFET on. This draws current from V_{OUT} through the inductor, forcing both V_{OUT} and V_{FB} to fall. When V_{FB} drops to the 500 mV threshold, the next DH on-time is triggered.

After the on-time is completed the high-side MOSFET is turned off and the low-side MOSFET turns on, the low-side MOSFET remains on until the inductor current ramps down to zero, at which point the low-side MOSFET is turned off.

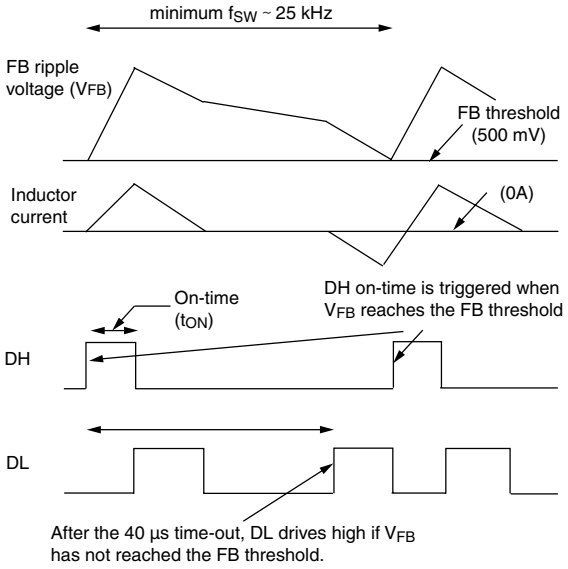


Figure 5 - Ultrasonic power-save Operation

Because the on-times are forced to occur at intervals no greater than 40 µs, the frequency will not fall below ~ 25 kHz. Figure 5 shows ultra-sonic power-save operation.

Benefits of Ultrasonic Power-Save

Having a fixed minimum frequency in power-save has some significant advantages as below:

- The minimum frequency of 25 kHz is outside the audible range of human ear. This makes the operation of the SiC417 very quiet.
- The output voltage ripple seen in power-save mode is significant lower than conventional power-save, which improves efficiency at light loads.
- Lower ripple in power-save also makes the power component selection easier.

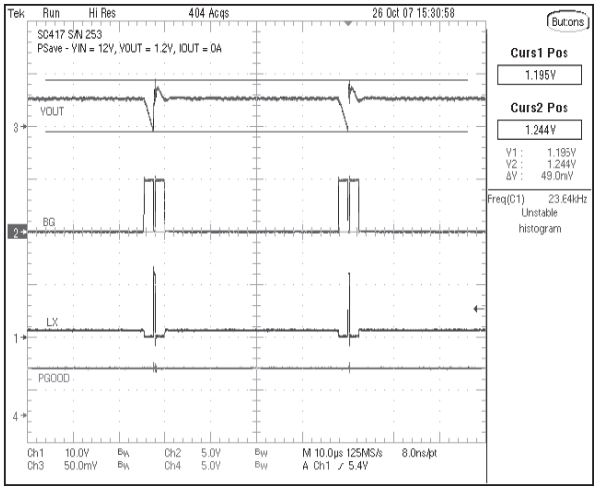


Figure 6 - Ultrasonic Power-Save Operation Mode

Figure 6 shows the behavior under power-save and continuous conduction mode at light loads.

Smart Power-Save Protection

Active loads may leak current from a higher voltage into the switcher output. Under light load conditions with power-savepower-save enabled, this can force V_{OUT} to slowly rise and reach the over-voltage threshold, resulting in a hard shutdown. Smart power-save prevents this condition.

When the FB voltage exceeds 10 % above nominal (exceeds 550 mV), the device immediately disables power-save, and DL drives high to turn on the low-side MOSFET. This draws current from V_{OUT} through the inductor and causes V_{OUT} to fall. When V_{FB} drops back to the 500 mV trip point, a normal t_{ON} switching cycle begins.

This method prevents a hard OVP shutdown and also cycles energy from V_{OUT} back to V_{IN}. It also minimizes operating power by avoiding forced conduction mode operation. Figure 7 shows typical waveforms for the smart power-save feature.

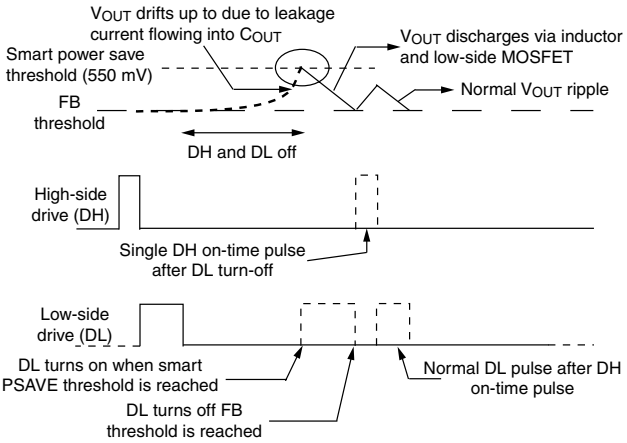


Figure 7 - Smart Power-Save

Current Limit Protection

The SiC417 features programmable current limit capability, which is accomplished by using the $R_{DS(ON)}$ of the lower MOSFET for current sensing. The current limit is set by R_{ILIM} resistor. The R_{ILIM} resistor connects from the I_{LIM} pin to the LX pin which is also the drain of the low-side MOSFET.

When the low-side MOSFET is on, an internal ~ 10 µA current flows from the I_{LIM} pin and the R_{ILIM} resistor, creating a voltage drop across the resistor. While the low-side MOSFET is on, the inductor current flows through it and creates a voltage across the $R_{DS(ON)}$. The voltage across the MOSFET is negative with respect to ground.

If this MOSFET voltage drop exceeds the voltage across R_{ILIM}, the voltage at the I_{LIM} pin will be negative and current limit will activate. The current limit then keeps the low-side MOSFET on and will not allow another high-side on-time, until the current in the low-side MOSFET reduces enough to bring the I_{LIM} voltage back up to zero. This method regulates the inductor valley current at the level shown by I_{LIM} in figure 8.

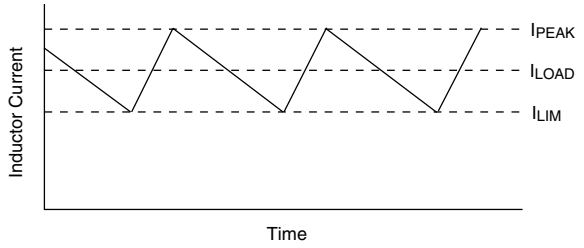


Figure 8 - Valley Current Limit

Setting the valley current limit to 10 A results in a 10 A peak inductor current plus peak ripple current. In this situation, the average (load) current through the inductor is 10 A plus one-half the peak-to-peak ripple current.

The internal 10 µA current source is temperature compensated at 4100 ppm in order to provide tracking with the $R_{DS(ON)}$. The R_{ILIM} value is calculated by the following equation.

$$R_{ILIM} = 735 \times I_{LIM}$$

Note that because the low-side MOSFET with low $R_{DS(ON)}$ is used for current sensing, the PCB layout, solder connections, and PCB connection to the LX node must be done carefully to obtain good results. Refer to the layout guidelines for information.

Soft-Start of PWM Regulator

Soft-start is achieved in the PWM regulator by using an internal voltage ramp as the reference for the FB Comparator. The voltage ramp is generated using an internal charge pump which drives the reference from zero to 500 mV in ~ 1.2 mV increments, using an internal ~ 500 kHz oscillator. When the ramp voltage reaches 500 mV, the ramp is ignored and the FB comparator switches over to a fixed 500 mV threshold. During soft-start the output voltage tracks the internal ramp, which limits the start-up inrush current and provides a controlled softstart profile for a wide range of applications. Typical softstart ramp time is 850 µs. During soft-start the regulator turns off the low-side MOSFET on any cycle if the inductor current falls to zero. This prevents negative inductor current, allowing the device to start into a pre-biased output.

Power Good Output

The power good (P_{GOOD}) output is an open-drain output which requires a pull-up resistor. When the output voltage is 10 % below the nominal voltage, P_{GOOD} is pulled low. It is held low until the output voltage returns above - 8 % of nominal. P_{GOOD} is held low during start-up and will not be allowed to transition high until soft-start is completed (when V_{FB} reaches 500 mV) and typically 2 ms has passed.

P_{GOOD} will transition low if the V_{FB} pin exceeds + 20 % of nominal, which is also the over-voltage shutdown threshold (600 mV). P_{GOOD} also pulls low if the EN/PSV pin is low when V5V is present.

Output Over-Voltage Protection

Over-voltage protection becomes active as soon as the device is enabled. The threshold is set at 500 mV + 20 % (600 mV). When V_{FB} exceeds the OVP threshold, DL latches high and the low-side MOSFET is turned on. DL remains high and the controller remains off , until the EN/PSV input is toggled or V5V is cycled. There is a 5 µs delay built into the OVP detector to prevent false transitions. P_{GOOD} is also low after an OVP event.

Output Under-Voltage Protection

When V_{FB} falls 25 % below its nominal voltage (falls to 375 mV) for eight consecutive clock cycles, the switcher is shut off and the DH and DL drives are pulled low to tristate the MOSFETs. The controller stays off until EN/PSV is toggled or V5V is cycled.

V5V UVLO, and POR

Under-voltage lock-out (UVLO) circuitry inhibits switching and tri-states the DH/DL drivers until V5V rises above 3.9 V. An internal Power-On Reset (POR) occurs when V5V exceeds 3.9 V, which resets the fault latch and soft-start

counter to prepare for soft-start. The SiC417 then begins a soft-start cycle. The PWM will shut off if V5V falls below 3.6 V.

LDO Regulator

The SiC417 features an integrated LDO regulator with a programmable output voltage from 0.75 V to 5.25 V using external resistors, when an external supply is used to power V5V. The feedback pin (FBL) for the LDO is regulated to 750 mV. There is also an enable pin (ENL) for the LDO that provides independent control. The LDO voltage can also be used to provide the bias voltage for the switching regulator, when V_{LDO} is tied to V5V. More detail can be found in the On Chip LDO bias section coming up.

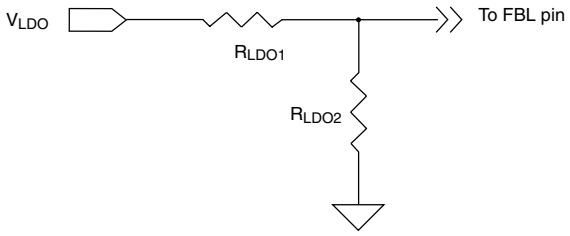


Figure 9 - LDO Start-Up

The LDO output voltage is set by the following equation.

$$V_{LDO} = 750\ mV \times \left(1 + \frac{R_{LDO1}}{R_{LDO2}}\right)$$

A minimum capacitance of 1 µF referenced to AGND is normally required at the output of the LDO for stability. If the LDO is providing bias power to the device, then a minimum 0.1 µF capacitor referenced to A_{GND} is required along with a minimum 1.0 µF capacitor referenced to P_{GND} to filter the gate drive pulses. Refer to the layout guideline section.

LDO Start-up

Before start-up, the LDO checks the status of the following signals to ensure proper operation can be maintained.

1. ENL pin
2. V_{LDO} output
3. V_{IN} input voltage

When the ENL pin is high and V_{IN} is above the UVLO point, the LDO will begin start-up. During the initial phase, when the LDO output voltage is near zero, the LDO initiates a current-limited start-up (typically 85 mA) to charge the output capacitor. When V_{LDO} has reached 90 % of the final value (as sensed at the FBL pin), the LDO current limit is increased to ~ 200 mA and the LDO output is quickly driven to the nominal value by the internal LDO regulator.

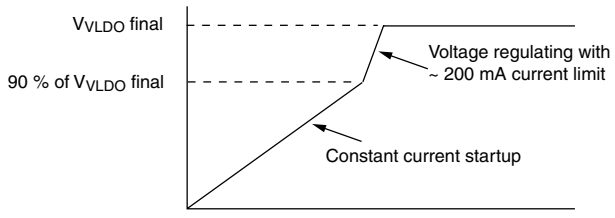


Figure 10 - LDO Start-Up

LDO Switchover Function

The SiC417 includes a switch-over function for the LDO. The switch-over function is designed to increase efficiency by using the more efficient dc-to-dc converter to power the LDO output, avoiding the less efficient LDO regulator when possible. The switch-over function connects the V_{LDO} pin directly to the V_{OUT} pin using an internal switch. When the switch-over is complete the LDO is turned off, which results in a power savings and maximizes efficiency. If the LDO output is used to bias the SiC417, then after switch-over the device is self-powered from the switching regulator with the LDO turned off.

The switch-over logic waits for 32 switching cycles before it starts the switch-over. There are two methods that determine the switch-over of V_{LDO} to V_{OUT}.

In the first method, the LDO is already in regulation and the dc-to-dc converter is later enabled. As soon as the P_{GOOD} output goes high, the 32 cycles are started. The voltages at the V_{LDO} and V_{OUT} pins are then compared; if the two voltages are within ± 300 mV of each other, the V_{LDO} pin connects to the V_{OUT} pin using an internal switch, and the LDO is turned off.

In the second method, the dc-to-dc converter is already running and the LDO is enabled. In this case the 32 cycles are started as soon as the LDO reaches 90 % of its final value. At this time, the V_{LDO} and V_{OUT} pins are compared, and if within ± 300 mV the switch-over occurs and the LDO is turned off.

Benefits of having a switchover circuit

The switchover function is designed to get maximum efficiency out of the dc-to-dc converter. The efficiency for an LDO is very low especially for high input voltages. Using the switchover function we tie any rails connected to V_{LDO} through a switch directly to V_{OUT}. Once switchover is complete LDO is turned off which saves power. This gives us the maximum efficiency out of the SiC417.

If the LDO output is used to bias the SiC417, then after switchover the V_{OUT} self biases the SiC417 and operates in self-powered mode.

Steps to follow when using the on chip LDO to bias the SiC417:

- Always tie the V5V to V_{LDO} before enabling the LDO
- Enable the LDO before enabling the switcher
- LDO has a current limit of 85 mA at start-up with 12 V_{IN}, so do not connect any load between V_{LDO} and ground
- The current limit for the LDO goes up to 200 mA once the V_{LDO} reaches 90 % of its final values and can easily supply the required bias current to the IC.

Switch-over Limitations on V_{OUT} and V_{LDO}

Because the internal switch-over circuit always compares the V_{OUT} and V_{LDO} pins at start-up, there are limitations on permissible combinations of V_{OUT} and V_{LDO}. Consider the case where V_{OUT} is programmed to 1.5 V and V_{LDO} is programmed to 1.8 V. After start-up, the device would connect V_{OUT} to V_{LDO} and disable the LDO, since the two voltages are within the ± 300 mV switch-over window.

To avoid unwanted switch-over, the minimum difference between the voltages for V_{OUT} and V_{LDO} should be ± 500 mV.
It is not recommended to use the switch-over feature for an output voltage less than 3 V since this does not provide sufficient voltage for the gate-source drive to the internal p-channel switch-over MOSFET.

Switch-Over MOSFET Parasitic Diodes

The switch-over MOSFET contains parasitic diodes that are inherent to its construction, as shown in figure 11.

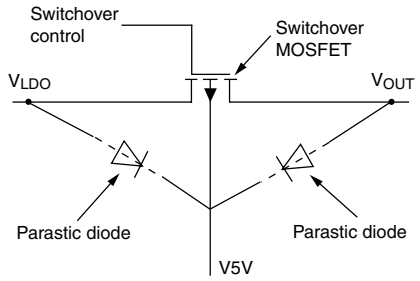


Figure 11 - Switch-over MOSFET Parasitic Diodes

There are some important design rules that must be followed to prevent forward bias of these diodes. The following two conditions need to be satisfied in order for the parasitic diodes to stay off.
- V5V ≥ V_{LDO}
- V5V ≥ V_{OUT}

If either V_{LDO} or V_{OUT} is higher than V5V, then the respective diode will turn on and the SiC417 operating current will flow through this diode. This has the potential of damaging the device.

ENL Pin and V_{IN} UVLO

The ENL pin also acts as the switcher under-voltage lockout for the V_{IN} supply. The V_{IN} UVLO voltage is programmable via a resistor divider at the V_{IN}, ENL and A_{GND} pins.
ENL is the enable/disable signal for the LDO. In order to implement the V_{IN} UVLO there is also a timing requirement that needs to be satisfied.
If the ENL pin transitions low within 2 switching cycles and is < 1 V, then the LDO will turn off but the switcher remains on.
If ENL goes below the V_{IN} UVLO threshold and stays above 1 V, then the switcher will turn off but the LDO remains on.
The V_{IN} UVLO function has a typical threshold of 2.6 V on the V_{IN} rising edge. The falling edge threshold is 2.4 V.
Note that it is possible to operate the switcher with the LDO disabled, but the ENL pin must be below the logic low threshold (0.4 V maximum).

ENL Logic Control of PWM Operation

When the ENL input is driven above 2.6 V, it is impossible to determine if the LDO output is going to be used to power the device or not. In self-powered operation where the LDO will power the device, it is necessary during the LDO start-up to hold the PWM switching off until the LDO has reached 90 % of the final value. This is to prevent overloading the current-limited LDO output during the LDO start-up. However, if the switcher was previously operating (with EN/PSV high but ENL at ground, and V5V supplied externally), then it is undesirable to shut down the switcher.
To prevent this, when the ENL input is taken above 2.6 V (above the V_{IN} UVLO threshold), the internal logic checks the P_{GOOD} signal. If P_{GOOD} is high, then the switcher is already running and the LDO will run through the start-up cycle without affecting the switcher. If P_{GOOD} is low, then the LDO will not allow any PWM switching until the LDO output has reached 90 % of it's final value.

On-Chip LDO Bias the SiC417

The following steps must be followed when using the onchip LDO to bias the device.
- Connect V5V to V_{LDO} before enabling the LDO.
- The LDO has an initial current limit of 85 mA at start-up with 12 V_{IN}, therefore, do not connect any external load to V_{LDO} during start-up.
- When V_{LDO} reaches 90 % of its final value, the LDO current limit increases to 200 mA. At this time the LDO may be used to supply the required bias current to the device.
- Switching will be held off until V_{LDO} reaches regulation.

Attempting to operate in self-powered mode in any other configuration can cause unpredictable results and may damage the device.

Design Procedure

When designing a switch mode power supply, the input voltage range, load current, switching frequency, and inductor ripple current must be specified.
The maximum input voltage (V_{INMAX}) is the highest specified input voltage. The minimum input voltage (V_{INMIN}) is determined by the lowest input voltage after evaluating the voltage drops due to connectors, fuses, switches, and PCB traces.
The following parameters define the design:
- Nominal output voltage (V_{OUT})
- Static or DC output tolerance
- Transient response
- Maximum load current (I_{OUT})

There are two values of load current to evaluate - continuous load current and peak load current. Continuous load current relates to thermal stresses which drive the selection of the inductor and input capacitors. Peak load current determines instantaneous component stresses and filtering requirements such as inductor saturation, output capacitors, and design of the current limit circuit.
The following values are used in this design:
- V_{IN} = 12 V ± 10 %
- V_{OUT} = 1.05 V ± 4 %
- f_{SW} = 250 kHz
- Load = 10 A maximum

Frequency Selection

Selection of the switching frequency requires making a trade-off between the size and cost of the external filter components (inductor and output capacitor) and the power conversion efficiency.
The desired switching frequency is 250 kHz which results from using component selected for optimum size and cost.
A resistor (R_{TON}) is used to program the on-time (indirectly setting the frequency) using the following equation.

$$R_{ton} = \frac{(t_{ON} - 10\ ns) \times V_{IN}}{25\ pF \times V_{OUT}}$$

To select R_{TON}, use the maximum value for V_{IN}, and for t_{ON} use the value associated with maximum V_{IN}.

$$t_{ON} = \frac{V_{OUT}}{V_{INMAX.} \times f_{SW}}$$

t_{ON} = 318 ns at 13.2 V_{IN}, 1.05 V_{OUT}, 250 kHz
Substituting for R_{TON} results in the following solution
R_{TON} = 154.9 kΩ, use R_{TON} = 154 kΩ.

Inductor Selection

In order to determine the inductance, the ripple current must first be defined. Low inductor values result in smaller size but create higher ripple current which can reduce efficiency. Higher inductor values will reduce the ripple current and voltage and for a given DC resistance are more efficient. However, larger inductance translates directly into larger packages and higher cost. Cost, size, output ripple, and efficiency are all used in the selection process.
The ripple current will also set the boundary for power-save operation. The switching will typically enter power-save mode when the load current decreases to 1/2 of the ripple current. For example, if ripple current is 4 A then power-save operation will typically start for loads less than 2 A. If ripple current is set at 40 % of maximum load current, then power-save will start for loads less than 20 % of maximum current.
The inductor value is typically selected to provide a ripple current that is between 25 % to 50 % of the maximum load current. This provides an optimal trade-off between cost, efficiency, and transient performance.
During the DH on-time, voltage across the inductor is (V_{IN}-V_{OUT}). The equation for determining inductance is shown next.

$$L = \frac{(V_{IN} - V_{OUT}) \times t_{ON}}{I_{RIPPLE}}$$

Example

In this example, the inductor ripple current is set equal to 50 % of the maximum load current. Thus ripple current will be 50 % x 10 A or 5 A. To find the minimum inductance needed, use the V_{IN} and T_{ON} values that correspond to V_{INMAX}.

$$L = \frac{(13.2 - 1.05) \times 318\ ns}{5\ A} = 77\ \mu H$$

A slightly larger value of 0.88 µH is selected. This will decrease the maximum I_{RIPPLE} to 4.4 A.

Note that the inductor must be rated for the maximum DC load current plus 1/2 of the ripple current. The ripple current under minimum V_{IN} conditions is also checked using the following equations.

$$T_{ON\_VINMIN} = \frac{25\ pF \times R_{TON} \times V_{OUT}}{V_{INMIN}}$$

$$I_{RIPPLE} = \frac{(V_{IN} - V_{OUT}) \times T_{ON}}{L}$$

$$I_{RIPPLE\_VIN} = \frac{(10.8 - 1.05) \times 384\ ns}{0.88\ \mu H} = 4.25\ A$$

Capacitor Selection

The output capacitors are chosen based on required ESR and capacitance. The maximum ESR requirement is controlled by the output ripple requirement and the DC tolerance. The output voltage has a DC value that is equal to the valley of the output ripple plus 1/2 of the peak-to-peak ripple. Change in the output ripple voltage will lead to a change in DC voltage at the output.
The design goal is that the output voltage regulation be ± 4 % under static conditions. The internal 500 mV reference tolerance is 1 %. Allowing 1 % tolerance from the FB resistor divider, this allows 2 % tolerance due to V_{OUT} ripple.
Since this 2 % error comes from 1/2 of the ripple voltage, the allowable ripple is 4 %, or 42 mV for a 1.05 V output.
The maximum ripple current of 4.4 A creates a ripple voltage across the ESR. The maximum ESR value allowed is shown by the following equations.

$$ESR_{MAX} = \frac{V_{RIPPLE}}{I_{RIPPLEMAX}} = \frac{42\ mV}{4.4\ A}$$

$$ESR_{MAX} = 9.5\ m\Omega$$

The output capacitance is usually chosen to meet transient requirements. A worst-case load release, from maximum load to no load at the exact moment when inductor current is at the peak, determines the required capacitance. If the load release is instantaneous (load changes from maximum to zero in < 1 µs), the output capacitor must absorb all the inductor's stored energy. This will cause a peak voltage on the capacitor according to the following equation.

$$COUT_{MIN} = \frac{L\ (I_{OUT} + \frac{1}{2} \times I_{RIPPLEMAX})^2}{(V_{PEAK})^2 - (V_{OUT})^2}$$

Assuming a peak voltage V_{PEAK} of 1.150 (100 mV rise upon load release), and a 10 A load release, the required capacitance is shown by the next equation.

$$COUT_{MIN} = \frac{0.88\ \mu H\ (10 + \frac{1}{2} \times 4.4)^2}{(1.15)^2 - (1.05)^2}$$

$$COUT_{MIN} = 595\ \mu F$$

If the load release is relatively slow, the output capacitance can be reduced. At heavy loads during normal switching, when the FB pin is above the 500 mV reference, the DL

output is high and the low-side MOSFET is on. During this time, the voltage across the inductor is approximately - V_{OUT}. This causes a down-slope or falling di/dt in the inductor. If the load dI/dt is not much faster than the - dI/dt in the inductor, then the inductor current will tend to track the falling load current. This will reduce the excess inductive energy that must be absorbed by the output capacitor, therefore a smaller capacitance can be used.
The following can be used to calculate the needed capacitance for a given dI_{LOAD}/dt:
Peak inductor current is shown by the next equation.
$I_{LPK} = I_{MAX} + 1/2 \times I_{RIPPLEMAX}$
$I_{LPK} = 10 + 1/2 \times 4.4 = 12.2$ A
Rate of change of load current = dI_{LOAD}/dt
I_{MAX} = maximum load release = 10 A

$$C_{OUT} = I_{LPK} \times \frac{L \times \frac{I_{LPK}}{V_{OUT}} - \frac{I_{MAX}}{dI_{LOAD}} \times dt}{2 (V_{PK} - V_{OUT})}$$

Example

$$\text{Load } \frac{dI_{LOAD}}{dt} = \frac{2.5 \text{ A}}{\mu s}$$

This would cause the output current to move from 10 A to zero in 4 µs as shown by the following equation.

$$C_{OUT} = 12.2 \times \frac{0.88 \text{ µH} \times \frac{12.2}{1.05} - \frac{10}{2.5} \times 1 \text{ µs}}{2 (1.15 - 1.05)}$$

$$C_{OUT} = 379 \text{ µF}$$

Note that C_{OUT} is much smaller in this example, 379 µF compared to 595 µF based on a worst-case load release. To meet the two design criteria of minimum 379 µF and maximum 9 mΩ ESR, select two capacitors rated at 220 µF and 15 mΩ ESR.
It is recommended that an additional small capacitor be placed in parallel with C_{OUT} in order to filter high frequency switching noise.

Stability Considerations
Unstable operation is possible with adaptive on-time controllers, and usually takes the form of double-pulsing or ESR loop instability.
Double-pulsing occurs due to switching noise seen at the FB input or because the FB ripple voltage is too low. This causes the FB comparator to trigger prematurely after the 250 ns minimum off-time has expired. In extreme cases the noise can cause three or more successive on-times. Double-pulsing will result in higher ripple voltage at the output, but in most applications it will not affect operation.
This form of instability can usually be avoided by providing the FB pin with a smooth, clean ripple signal that is at least 10 mV_{p-p}, which may dictate the need to increase the ESR of the output capacitors. It is also imperative to provide a proper PCB layout as discussed in the Layout Guidelines section.

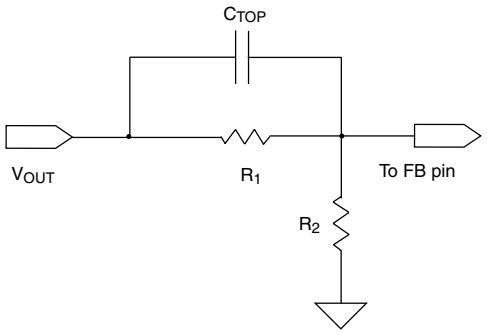


Figure 13 - Capacitor Coupling to FB Pin

Another way to eliminate doubling-pulsing is to add a small (~ 10 pF) capacitor across the upper feedback resistor, as shown in figure 13. This capacitor should be left unpopulated until it can be confirmed that double-pulsing exists. Adding the C_{TOP} capacitor will couple more ripple into FB to help eliminate the problem. An optional connection on the PCB should be available for this capacitor.
ESR loop instability is caused by insufficient ESR. The details of this stability issue are discussed in the ESR Requirements section. The best method for checking stability is to apply a zero-to-full load transient and observe the output voltage ripple envelope for overshoot and ringing. Ringing for more than one cycle after the initial step is an indication that the ESR should be increased.
One simple way to solve this problem is to add trace resistance in the high current output path. A side effect of adding trace resistance is output decreased load regulation.

ESR Requirements
A minimum ESR is required for two reasons. One reason is to generate enough output ripple voltage to provide10 mV_{p-p} at the FB pin (after the resistor divider) to avoid double-pulsing.
The second reason is to prevent instability due to insufficient ESR. The on-time control regulates the valley of the output ripple voltage. This ripple voltage is the sum of the two voltages. One is the ripple generated by the ESR, the other is the ripple due to capacitive charging and discharging during the switching cycle. For most applications the minimum ESR ripple voltage is dominated by the output capacitors, typically SP or POSCAP devices. For stability the ESR zero of the output capacitor should be lower than approximately one-third the switching frequency. The formula for minimum ESR is shown by the following equation.

$$ESR_{MIN} = \frac{3}{2 \times \pi \times C_{OUT} \times f_{SW}}$$

For applications using ceramic output capacitors, the ESR is normally too small to meet the above ESR criteria. In these applications it is necessary to add a small virtual ESR network composed of two capacitors and one resistor, as shown in figure 14. This network creates a ramp voltage

across C_L, analogous to the ramp voltage generated across the ESR of a standard capacitor. This ramp is then capacitive-coupled into the FB pin via capacitor C_C.

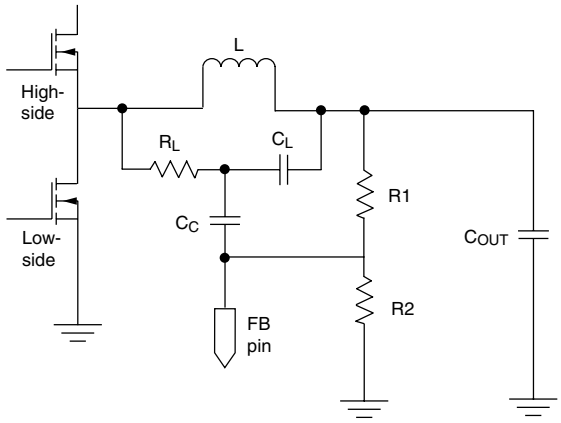


Figure 14 - Virtual ESR Ramp Current

Dropout Performance

The output voltage adjusts range for continuous-conduction operation is limited by the fixed 250 ns (typical) minimum off-time of the one-shot. When working with low input voltages, the duty-factor limit must be calculated using worst-case values for on and off times. The duty-factor limitation is shown by the next equation.

$$DUTY = \frac{T_{ON(MIN)}}{T_{ON(MIN)} \times T_{OFF(MAX)}}$$

The inductor resistance and MOSFET on-state voltage drops must be included when performing worst-case dropout duty-factor calculations.

System DC Accuracy (V_{OUT} Controller)

Three factors affect V_{OUT} accuracy: the trip point of the FB error comparator, the ripple voltage variation with line and load, and the external resistor tolerance. The error comparator off set is trimmed so that under static conditions it trips when the feedback pin is 500 mV, 1 %.

The on-time pulse from the SiC417 in the design example is calculated to give a pseudo-fixed frequency of 250 kHz. Some frequency variation with line and load is expected. This variation changes the output ripple voltage. Because constant on-time converters regulate to the valley of the output ripple, ½ of the output ripple appears as a DC regulation error. For example, if the output ripple is 50 mV with V_{IN} = 6 V, then the measured DC output will be 25 mV above the comparator trip point. If the ripple increases to 80 mV with V_{IN} = 25 V, then the measured DC output will be 40 mV above the comparator trip. The best way to minimize this effect is to minimize the output ripple.

To compensate for valley regulation, it may be desirable to use passive droop. Take the feedback directly from the output side of the inductor and place a small amount of trace resistance between the inductor and output capacitor.

This trace resistance should be optimized so that at full load the output droops to near the lower regulation limit. Passive droop minimizes the required output capacitance because the voltage excursions due to load steps are reduced as seen at the load.

The use of 1 % feedback resistors contributes up to 1 % error. If tighter DC accuracy is required, 0.1 % resistors should be used.

The output inductor value may change with current. This will change the output ripple and therefore will have a minor effect on the DC output voltage. The output ESR also affects the output ripple and thus has a minor effect on the DC output voltage.

Switching Frequency Variations

The switching frequency will vary depending on line and load conditions. The line variations are a result of fixed propagation delays in the on-time one-shot, as well as unavoidable delays in the external MOSFET switching. As V_{IN} increases, these factors make the actual DH on-time slightly longer than the ideal on-time. The net effect is that frequency tends to falls slightly with increasing input voltage. The switching frequency also varies with load current as a result of the power losses in the MOSFETs and the inductor. For a conventional PWM constant-frequency converter, as load increases the duty cycle also increases slightly to compensate for IR and switching losses in the MOSFETs and inductor.

A constant on-time converter must also compensate for the same losses by increasing the effective duty cycle (more time is spent drawing energy from V_{IN} as losses increase). The on-time is essentially constant for a given V_{OUT}/V_{IN} combination, to off set the losses the off-time will tend to reduce slightly as load increases. The net effect is that switching frequency increases slightly with increasing load.

SiC417 EVALUATION BOARD SCHEMATIC

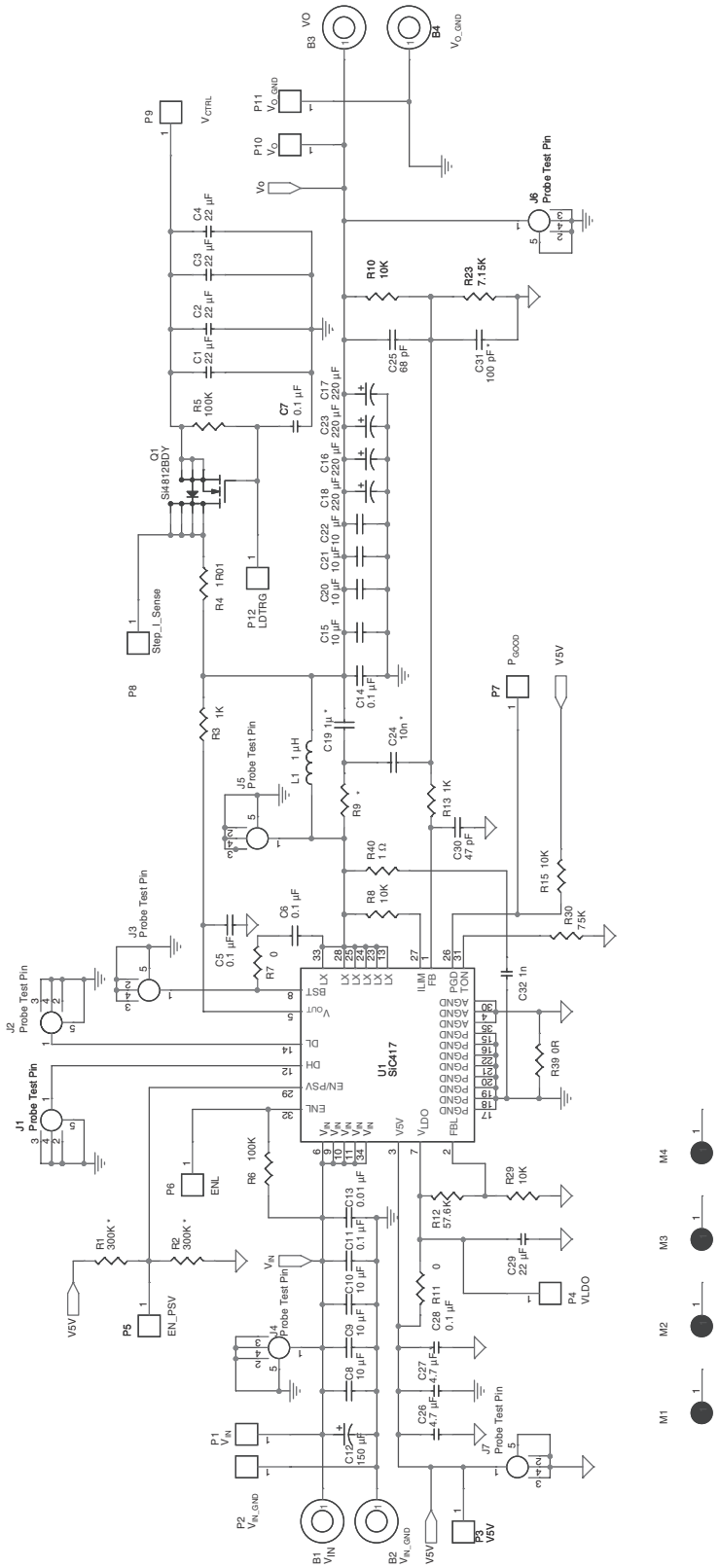


Figure 15. Evaluation Board Schematic

BILL OF MATERIALS

Reference Designator	Value	Voltage	Footprint	Part Number	Manufacturer
B1, B2, B3, B4			SOLDER-BANANA	575-4	Keystone
C29	22 µF	16 V	SM/C_1210	GRM32ER71C226ME18L	Murata
C5	0.1 µF	10 V	SM/C_0402	C0402C104K8RAC7867	Vishay
C6	0.1 µF	10 V	SM/C_0805	C0402C104K8RAC7867	Vishay
C11, C14, C28	0.1 µF	50 V	SM/C_0603	VJ0603Y104KXACW1BC	Vishay
C8, C9, C10	10 µF	25 V	SM/C_1210	TMK325B7106MN-T	Taiyo Yuden
C12	150 µF	35 V	D8X11.5-D0.6X3.5	EEU-FM1V151	Panasonic
C13	0.01 µF	50 V	SM/C_0402	VJ0402Y103KXACW1BC	Vishay
C15, C20, C21, C22	10 µF	16 V	SM/C_1206	GRM31CR71C106KAC7L	
C16, C17, C18, C23	220 µF	10 V	595D-D	593D227X0010E2TE3	Vishay
C19	1 µF		SM/C_0603		
C24	10 nF		SM/C_0603		
C25	100 pF	50 V	SM/C_0402	VJ0402A101JXACW1BC	Vishay
C26	4.7 µF	10 V	SM/C_0805	LMK212B7475KG-T	Taiyo Yuden
C27	4.7 µF	10 V	SM/C_0805	LMK212B7475KG-T	Taiyo Yuden
C30	47 pF		SM/C_0402	VJ0402A470JXACW1BC	
C31	100 pF		SM/C_0402	VJ0402Y101KXQCW1BC	Vishay
C32	1000 pF	50 V	SM/C_0805	VJ0805A102KXA	Vishay
J1, J2, J3, J4, J5, J6, J7	Probe test pin		Lecroy Probe Pin	PK007-015	Lecroy
L1	1 µH		IHLP4040	IHLP4040DZER1R0M01	Vishay
M1, M2, M3, M4	M HOLE2		Stacking Spacer	8834	Keystone
P1, P2, P3, P4, P5, P6, P7, P8, P9, P10, P11, P12	V_{IN}, GND etc.		Probe Hook	1540-2	Keystone
R1	300K	50 V	SM/C_0603	CRCW060310K0FKEA	Vishay
R2	300K	50 V	SM/C_0603	CRCW06030000FKEA	Vishay
R3, R13	1K		SM/C_0402	CRCW04021K00FKED	Vishay
R6	100K	50 V	SM/C_0603	CRCW0603100KFKEA	Vishay
R7, R11	0R		SM/C_0603	CRCW06030000Z0EA	Vishay
R8, R10, R15, R29	10K		SM/C_0603	MCR03EZHF1002	ROHM
R9			SM/C_0603		
R12	57.6K		SM/C_0603	CRCW060357K6FKEA	Vishay
R23	7.15K		SM/C_0603	CRCW06037K15FKEA	Vishay
R30	75K		SM/C_0603	CRCW0603154KFKEA	Vishay
R39	0R		SM/C_0402	CRCW04020000Z0ED	Vishay
R40	1Ω		SM/C_0805	CRCW08051R00FNEA	Vishay
U1	SiC417		QFN5X5_32 leads + 3 pads		Vishay
Optional Cicuitry for Transient Response Testing					
Q1	Si4812BDY	30 V	SO-8	Si4812BDY	Vishay
R4	1R01	200 V	C_2512	CRCW25121R00FKTA	Vishay
R5	100K	50 V	SM/C_0603	CRCW0603100KFKEA	Vishay
C7	0.1 µF	50 V	SM/C_0603	VJ0603Y104KXACW1BC	Vishay
C1, C2, C3, C4	22 µF	16 V	SM/C_1210	GRM32ER71C226ME18L	Murata

PCB LAYOUT OF THE EVALUATION BOARD

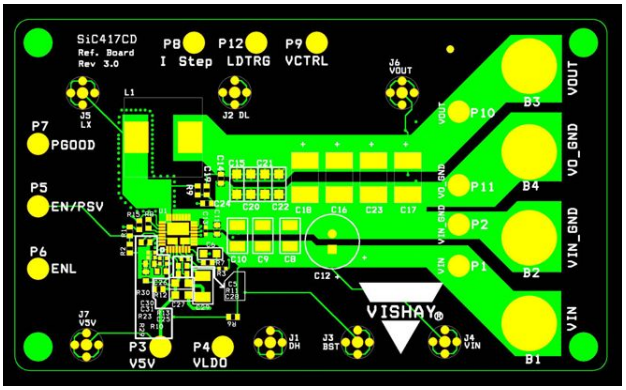


Figure 16. PCB Layout - Top Layer

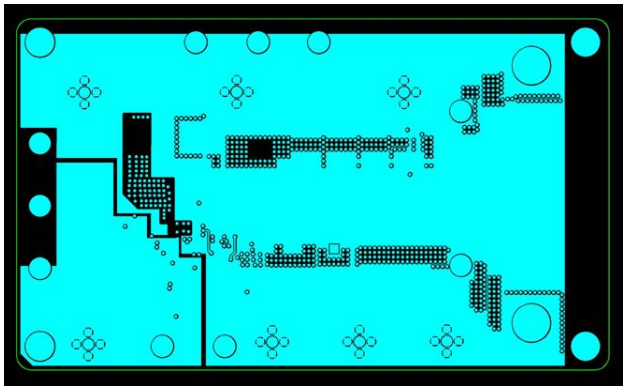


Figure 17. PCB Layout - MidLayer1

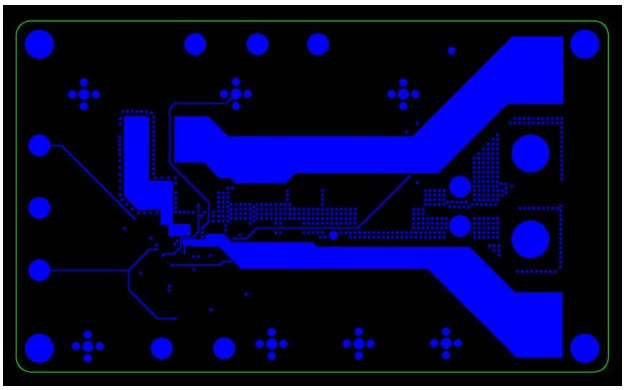


Figure 18. PCB Layout - MidLayer2

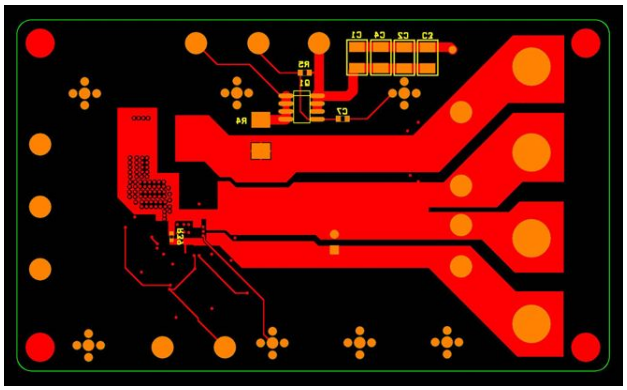
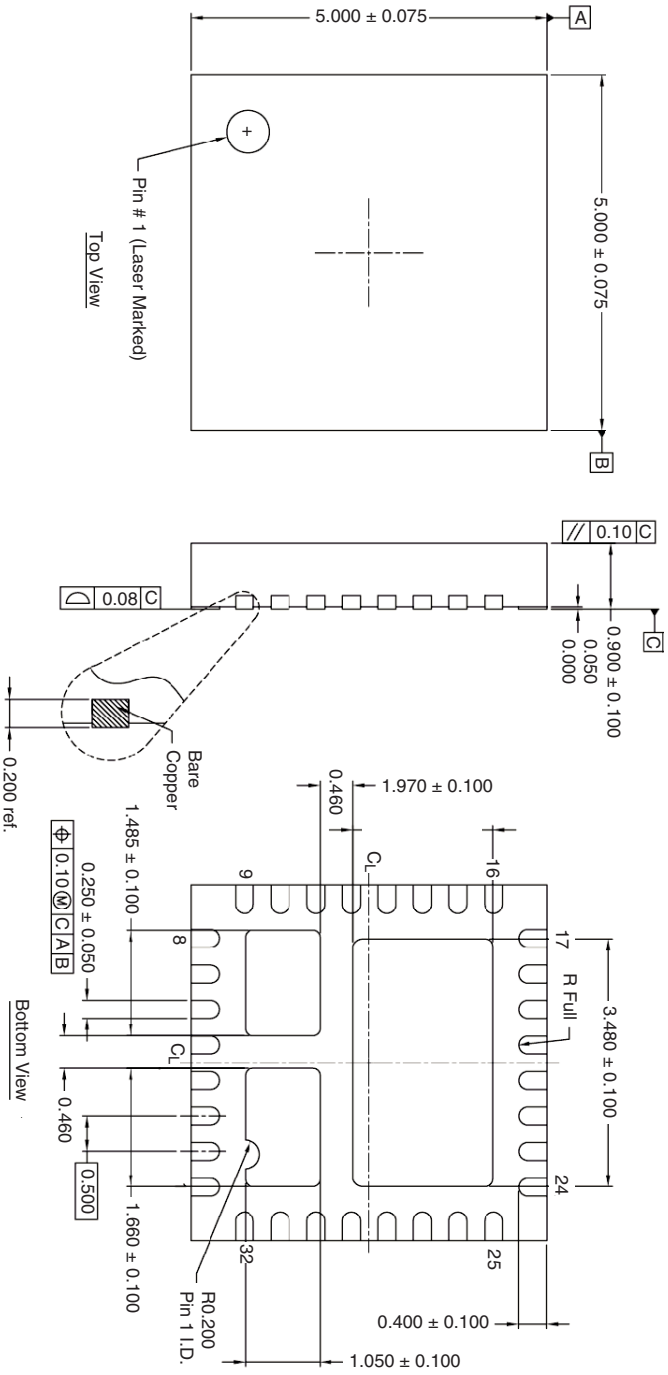


Figure 19. PCB Layout - Bottom Layer

PACKAGE DIMENSIONS AND MARKING INFO



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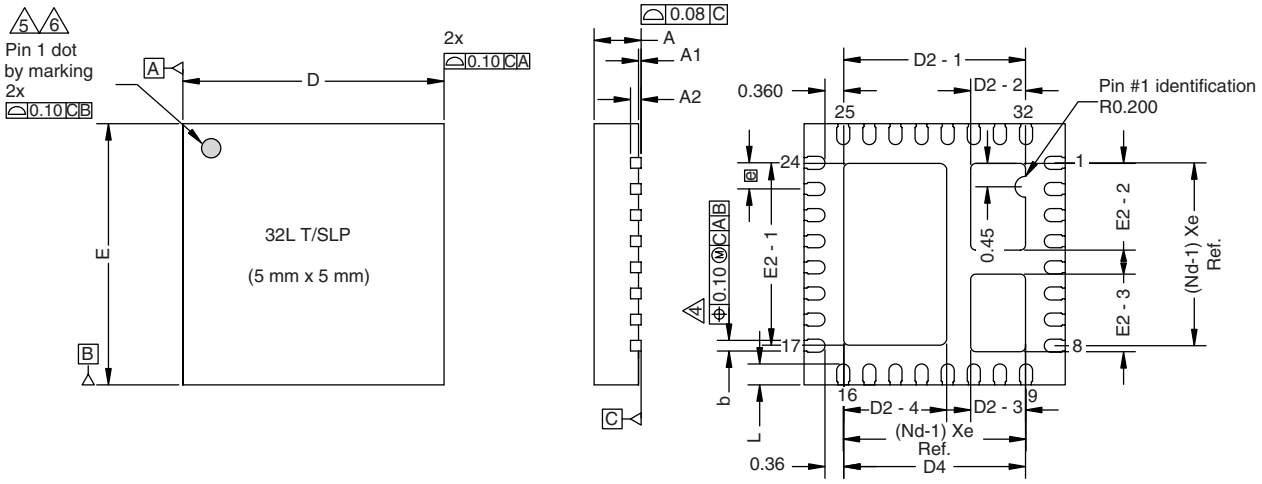
PowerPAK® MLP55-32L CASE OUTLINE



Top View Side View Bottom View

DIM	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.80	0.85	0.90	0.031	0.033	0.035
A1(8)	0.00	-	0.05	0.000	-	0.002
A2		0.20 REF.			0.008 REF.	
b(4)	0.20	0.25	0.30	0.078	0.098	0.011
D		5.00 BSC			0.196 BSC	
e		0.50 BSC			0.019 BSC	
E		5.00 BSC			0.196 BSC	
L	0.35	0.40	0.45	0.013	0.015	0.017
N(3)		32			32	
Nd(3)		8			8	
Ne(3)		8			8	
D2 - 1	3.43	3.48	3.53	0.135	0.137	0.139
D2 - 2	1.00	1.05	1.10	0.039	0.041	0.043
D2 - 3	1.00	1.05	1.10	0.039	0.041	0.043
D2 - 4	1.92	1.97	2.02	0.075	0.077	0.079
E2 - 1	3.43	3.48	3.53	0.135	0.137	0.139
E2 - 2	1.61	1.66	1.71	0.063	0.065	0.067
E2 - 3	1.43	1.48	1.53	0.056	0.058	0.060
ECN: T-08957-Rev. A, 29-Dec-08 DWG: 5983						

Notes

1. Use millimeters as the primary measurement.
2. Dimensioning and tolerances conform to ASME Y14.5M. - 1994.
3. N is the number of terminals.
   Nd is the number of terminals in X-direction and Ne is the number of terminals in Y-direction.
4. Dimension b applies to plated terminal and is measured between 0.20 mm and 0.25 mm from terminal tip.
5. The pin #1 identifier must be existed on the top surface of the package by using indentation mark or other feature of package body.
6. Exact shape and size of this feature is optional.
7. Package warpage max. 0.08 mm.
8. Applied only for terminals.

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