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SiZ700DT

Vishay Siliconix

N-Channel 20-V (D-S) MOSFETs

PRODUCT SUMMARY

	V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A)	Q _g (Typ.)
Channel-1	20	0.0086 at V _{GS} = 10 V	16 ^a	9.5 nC
		0.0108 at V _{GS} = 4.5 V	16 ^a	
Channel-2	20	0.0058 at V _{GS} = 10 V	16 ^a	27 nC
		0.0066 at V _{GS} = 4.5 V	16 ^a	

FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET® Power MOSFETs
- 100 % R_g Tested
- Compliant to RoHS Directive 2002/95/EC

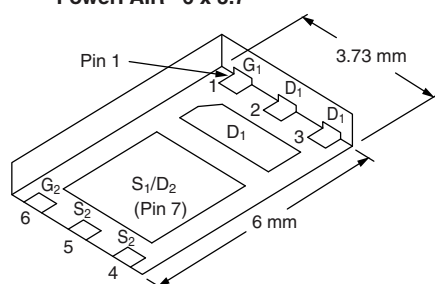
APPLICATIONS

- Notebook System Power
- POL



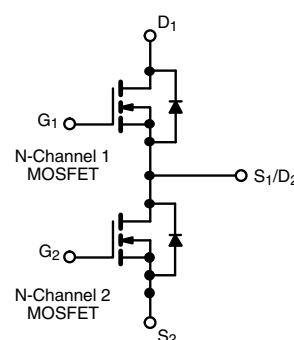
RoHS
COMPLIANT
HALOGEN
FREE

PowerPAIR® 6 x 3.7



Ordering Information:

SiZ700DT-T1-GE3 (Lead (Pb)-free and Halogen-free)



ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)

Parameter		Symbol	Channel-1	Channel-2	Unit
Drain-Source Voltage		V _{DS}	20	20	V
Gate-Source Voltage		V _{GS}	± 16		
Continuous Drain Current (T _J = 150 °C)	T _C = 25 °C	I _D	16 ^a	16 ^a	A
	T _C = 70 °C		16 ^a	16 ^a	
	T _A = 25 °C		13.1 ^{b, c}	17.3 ^{b, c}	
	T _A = 70 °C		10.5 ^{b, c}	13.9 ^{b, c}	
Pulsed Drain Current		I _{DM}	60	60	A
Source Drain Current Diode Current	T _C = 25 °C	I _S	14.7	16 ^a	
	T _A = 25 °C		1.96 ^{b, c}	2.3 ^{b, c}	
Maximum Power Dissipation	T _C = 25 °C	P _D	2.36	2.8	W
	T _C = 70 °C		1.5	1.78	
	T _A = 25 °C		1.4 ^{b, c}	1.47 ^{b, c}	
	T _A = 70 °C		0.9 ^{b, c}	0.94 ^{b, c}	
Operating Junction and Storage Temperature Range		T _J , T _{stg}	- 55 to 150		°C
Soldering Recommendations (Peak Temperature) ^{d, e}			260		

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Channel-1		Channel-2		Unit
		Typ.	Max.	Typ.	Max.	
Maximum Junction-to-Ambient ^{b, f}	R _{thJA}	39	53	33	45	°C/W
Maximum Junction-to-Case (Drain)	R _{thJC}	5.7	7.1	3.7	4.6	

Notes:

a. Package limited.

b. Surface mounted on 1" x 1" FR4 board.

c. t = 10 s.

d. See solder profile (www.vishay.com/doc?73257). The PowerPAIR is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

e. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.

f. Maximum under steady state conditions is 90 °C/W for channel-1 and 85 °C/W for channel-2.

Document Number: 69090

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SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)								
Parameter	Symbol	Test Conditions		Min.	Typ.	Max.	Unit	
Static								
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA	Ch-1	20			V	
		V _{GS} = 0 V, I _D = 250 μA	Ch-2	20				
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	I _D = 250 μA	Ch-1		21		mV/°C	
		I _D = 250 μA	Ch-2		21			
V _{GS(th)} Temperature Coefficient	ΔV _{GS(th)} /T _J	I _D = 250 μA	Ch-1		- 5.8		mV/°C	
		I _D = 250 μA	Ch-2		- 5.8			
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	Ch-1	0.8		2.2	V	
		V _{DS} = V _{GS} , I _D = 250 μA	Ch-2	0.8		2.2		
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 16 V	Ch-1			± 100	nA	
			Ch-2			± 100		
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 20 V, V _{GS} = 0 V	Ch-1			1	μA	
		V _{DS} = 20 V, V _{GS} = 0 V	Ch-2			1		
		V _{DS} = 20 V, V _{GS} = 0 V, T _J = 55 °C	Ch-1			10		
		V _{DS} = 20 V, V _{GS} = 0 V, T _J = 55 °C	Ch-2			10		
On-State Drain Current ^b	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 10 V	Ch-1	30			A	
		V _{DS} ≥ 5 V, V _{GS} = 10 V	Ch-2	30				
Drain-Source On-State Resistance ^b	R _{DS(on)}	V _{GS} = 10 V, I _D = 15 A	Ch-1		0.007	0.0086	Ω	
		V _{GS} = 10 V, I _D = 20 A	Ch-2		0.0047	0.0058		
		V _{GS} = 4.5 V, I _D = 10 A	Ch-1		0.0088	0.0108		
		V _{GS} = 4.5 V, I _D = 15 A	Ch-2		0.0054	0.0066		
Forward Transconductance ^b	g _{fs}	V _{DS} = 10 V, I _D = 15 A	Ch-1		60		S	
		V _{DS} = 10 V, I _D = 20 A	Ch-2		100			
Dynamic ^a								
Input Capacitance	C _{iss}	Channel-1 V _{DS} = 10 V, V _{GS} = 0 V, f = 1 MHz	Ch-1		1300		pF	
			Ch-2		3860			
Output Capacitance	C _{oss}		Ch-1		290			
			Ch-2		760			
Reverse Transfer Capacitance	C _{rss}	Channel-2 V _{DS} = 10 V, V _{GS} = 0 V, f = 1 MHz	Ch-1		132			
			Ch-2		350			
Total Gate Charge	Q _g	V _{DS} = 10 V, V _{GS} = 10 V, I _D = 15 A	Ch-1		20	35	nC	
		V _{DS} = 10 V, V _{GS} = 10 V, I _D = 20 A	Ch-2		55	85		
		Channel-1 V _{DS} = 10 V, V _{GS} = 4.5 V, I _D = 15 A	Ch-1		9.5	15		
			Ch-2		27	45		
Gate-Source Charge	Q _{gs}	Channel-2 V _{DS} = 10 V, V _{GS} = 4.5 V, I _D = 20 A	Ch-1		3.2			
			Ch-2		9.2			
Gate-Drain Charge	Q _{gd}		Ch-1		2.4			
			Ch-2		7.1			
Gate Resistance	R _g	f = 1 MHz	Ch-1	0.3	1.3	2.6	Ω	
			Ch-2	0.2	1	2		

Notes:

a. Guaranteed by design, not subject to production testing.

b. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %.



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SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)								
Parameter	Symbol	Test Conditions		Min.	Typ.	Max.	Unit	
Dynamic ^a								
Turn-On Delay Time	t _{d(on)}	Channel-1 V _{DD} = 10 V, R _L = 10 Ω I _D ≅ 1 A, V _{GEN} = 4.5 V, R _g = 1 Ω	Ch-1		9	15	ns	
			Ch-2		13	20		
Rise Time	t _r		Ch-1		8	15		
			Ch-2		8	15		
Turn-Off Delay Time	t _{d(off)}	Channel-2 V _{DD} = 10 V, R _L = 10 Ω I _D ≅ 1 A, V _{GEN} = 4.5 V, R _g = 1 Ω	Ch-1		25	40		
			Ch-2		52	80		
Fall Time	t _f		Ch-1		8	15		
			Ch-2		15	25		
Turn-On Delay Time	t _{d(on)}	Channel-1 V _{DD} = 10 V, R _L = 10 Ω I _D ≅ 1 A, V _{GEN} = 10 V, R _g = 1 Ω	Ch-1		8	15		
			Ch-2		12	20		
Rise Time	t _r		Ch-1		9	15		
			Ch-2		8	15		
Turn-Off Delay Time	t _{d(off)}	Channel-2 V _{DD} = 10 V, R _L = 10 Ω I _D ≅ 1 A, V _{GEN} = 10 V, R _g = 1 Ω	Ch-1		25	40		
			Ch-2		47	75		
Fall Time	t _f		Ch-1		8	15		
			Ch-2		10	15		
Drain-Source Body Diode Characteristics								
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C	Ch-1			14.7	A	
			Ch-2			16		
Pulse Diode Forward Current ^a	I _{SM}		Ch-1			60		
			Ch-2			60		
Body Diode Voltage	V _{SD}	I _S = 2 A, V _{GS} = 0 V	Ch-1		0.8	1.2	V	
		I _S = 2.3 A, V _{GS} = 0 V	Ch-2		0.8	1.2		
Body Diode Reverse Recovery Time	t _{rr}	Channel-1 I _F = 2 A, dI/dt = 100 A/μs, T _J = 25 °C	Ch-1		25	50	ns	
			Ch-2		40	80		
Body Diode Reverse Recovery Charge	Q _{rr}		Channel-2 I _F = 2.3 A, dI/dt = 100 A/μs, T _J = 25 °C	Ch-1		13	25	nC
				Ch-2		31	60	
Reverse Recovery Fall Time	t _a			Ch-1		12		ns
				Ch-2		21		
Reverse Recovery Rise Time	t _b			Ch-1		13		
				Ch-2		19		

Notes:

a. Guaranteed by design, not subject to production testing.

b. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

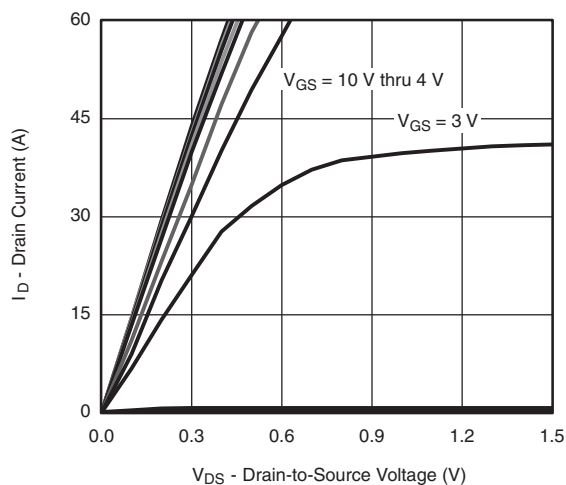
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

SiZ700DT

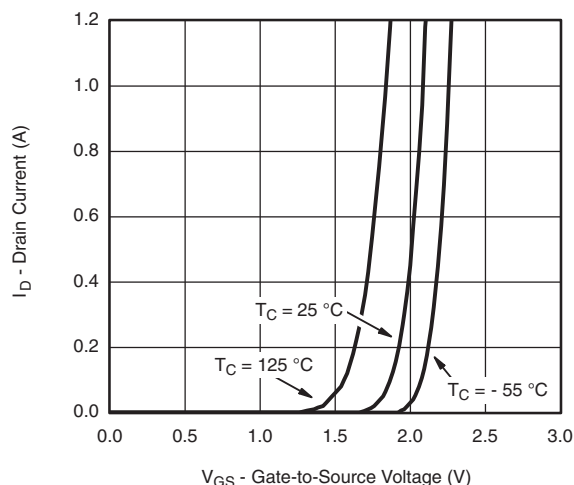
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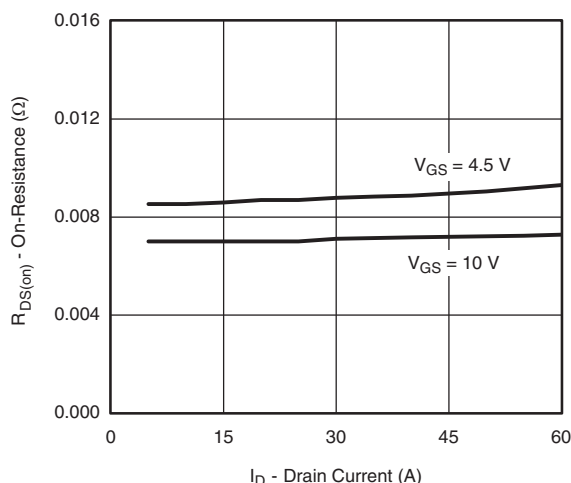
CHANNEL-1 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



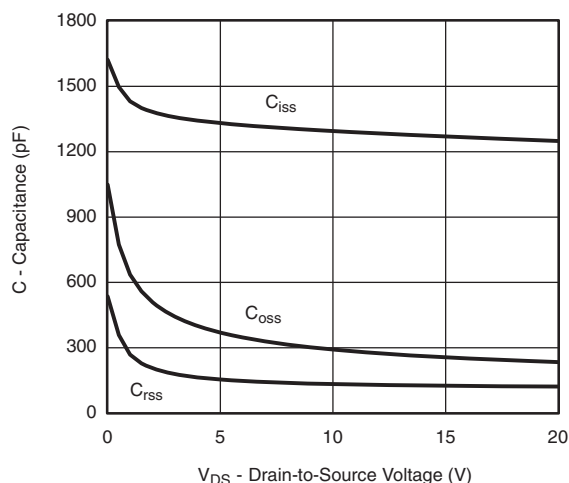
Output Characteristics



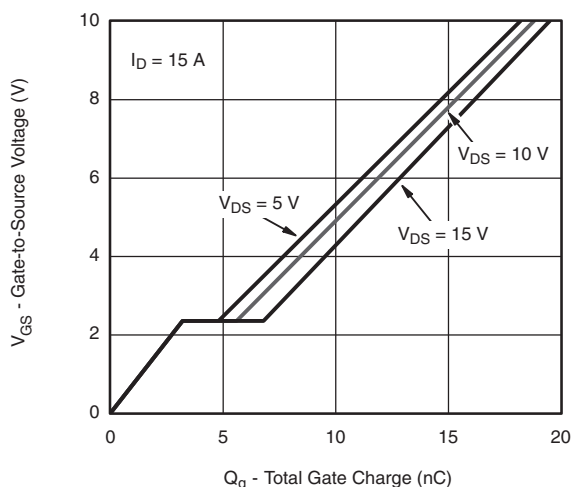
Transfer Characteristics



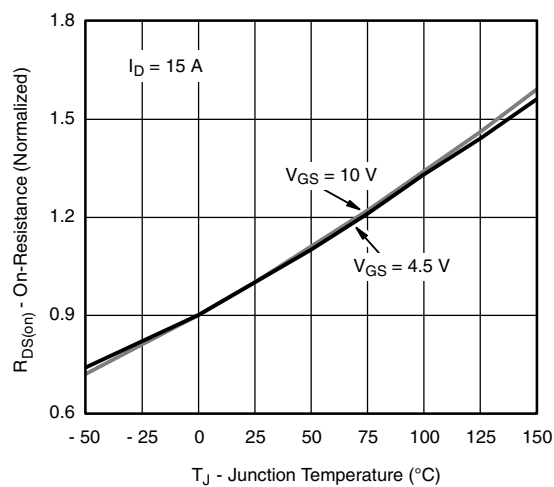
On-Resistance vs. Drain Current



Capacitance



Gate Charge



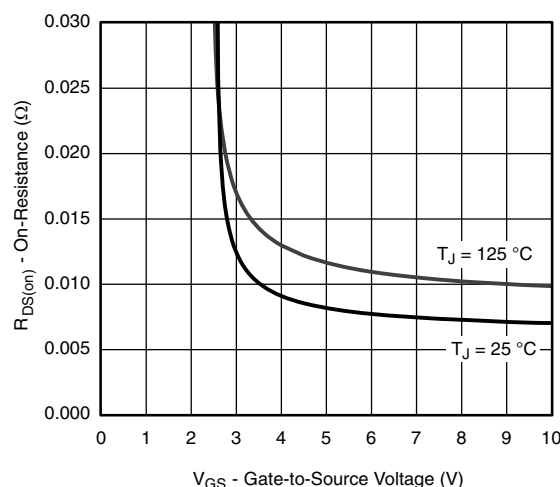
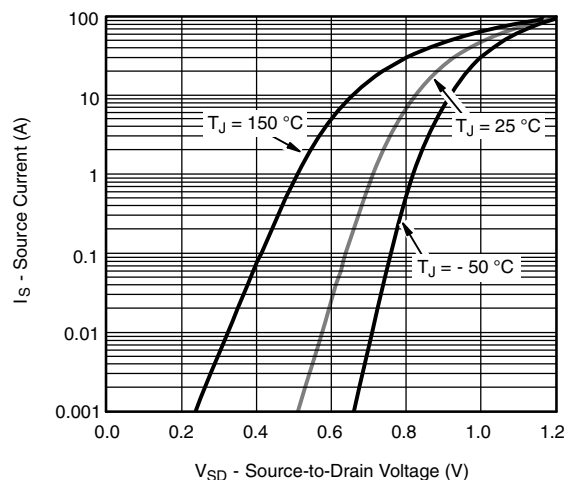
On-Resistance vs. Junction Temperature



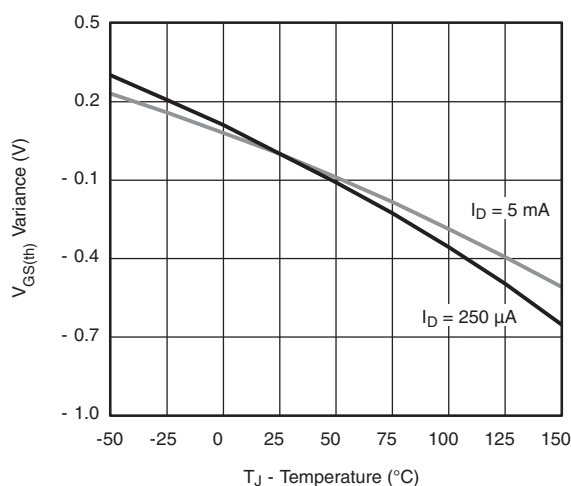
SiZ700DT

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CHANNEL-1 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

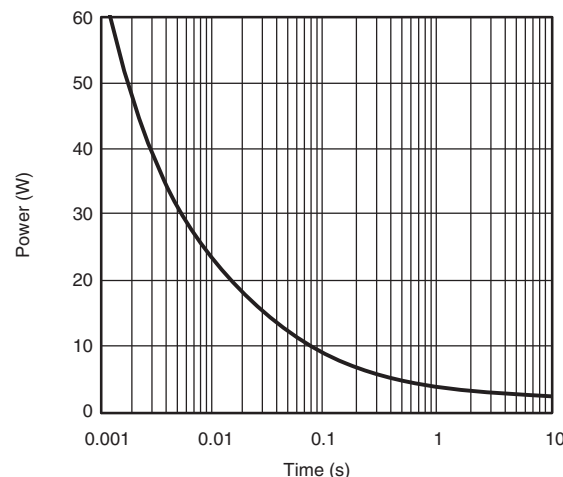


Source-Drain Diode Forward Voltage

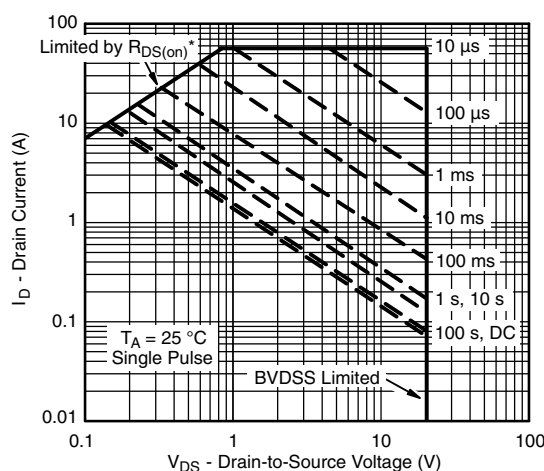


Threshold Voltage

On-Resistance vs. Gate-to-Source Voltage



Single Pulse Power



* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

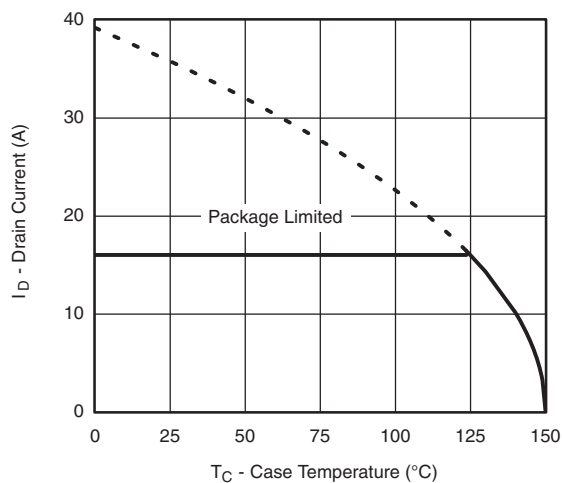
Safe Operating Area, Junction-to-Ambient

SiZ700DT

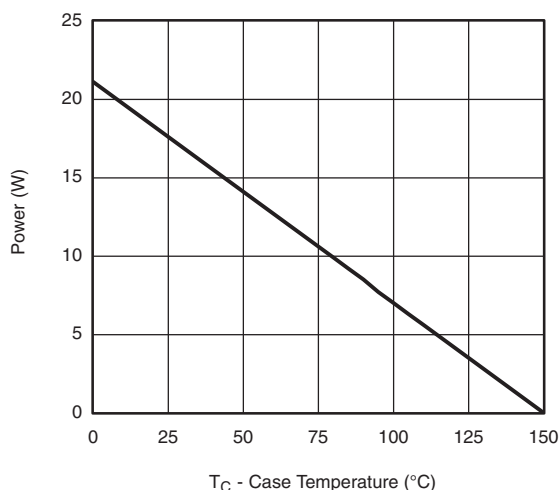
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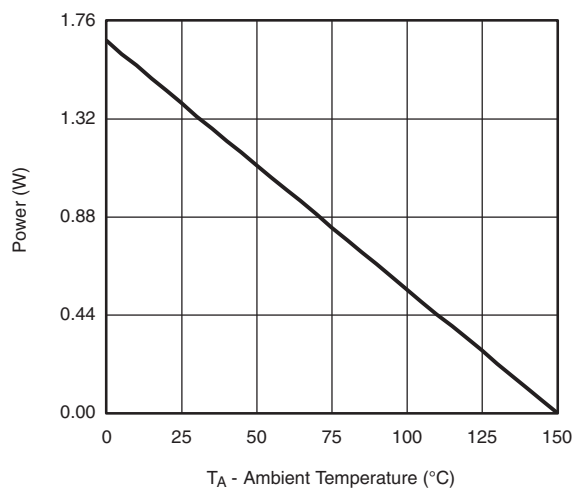
CHANNEL-1 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Current Derating*



Power, Junction-to-Case



Power, Junction-to-Ambient

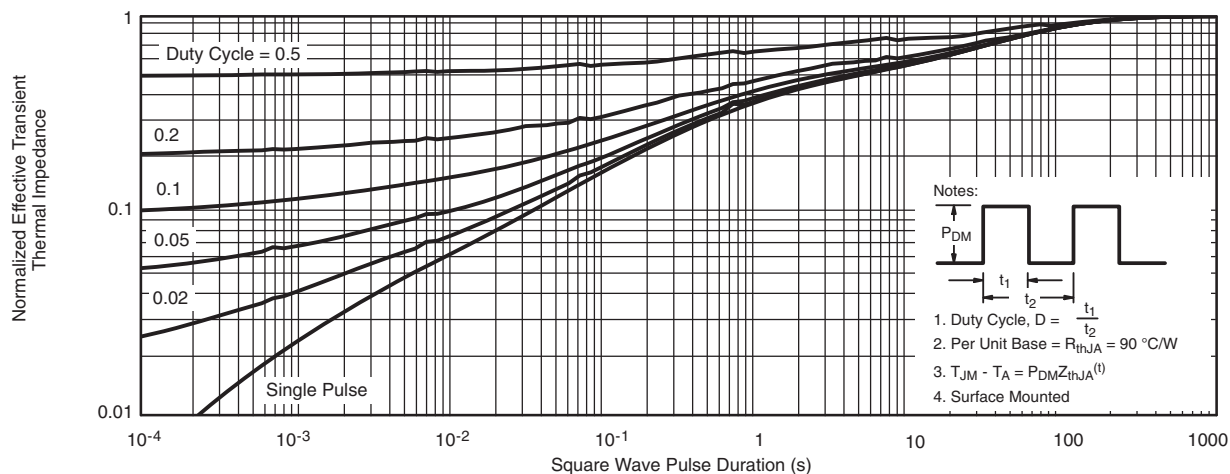
* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



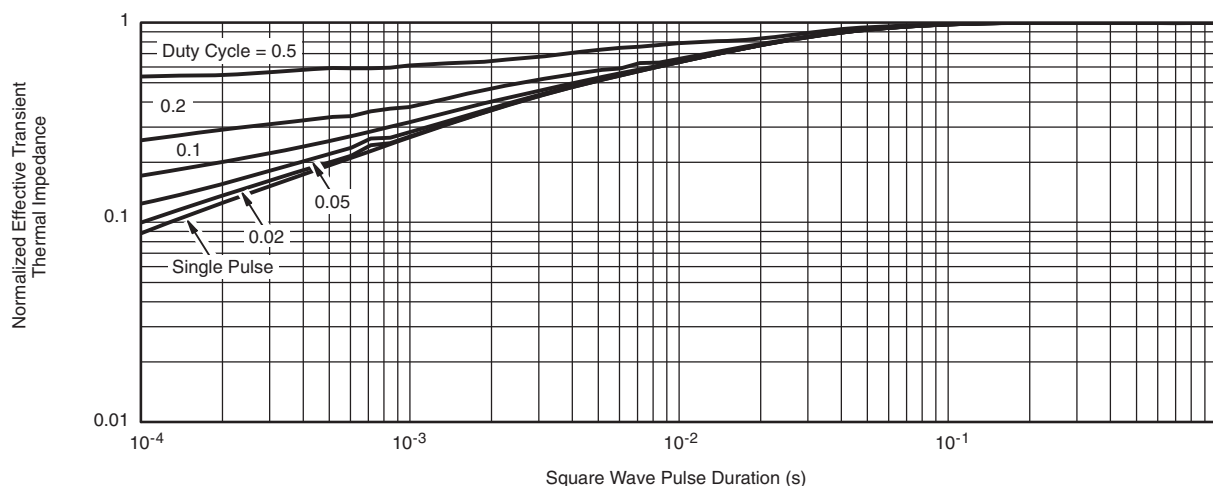
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CHANNEL-1 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



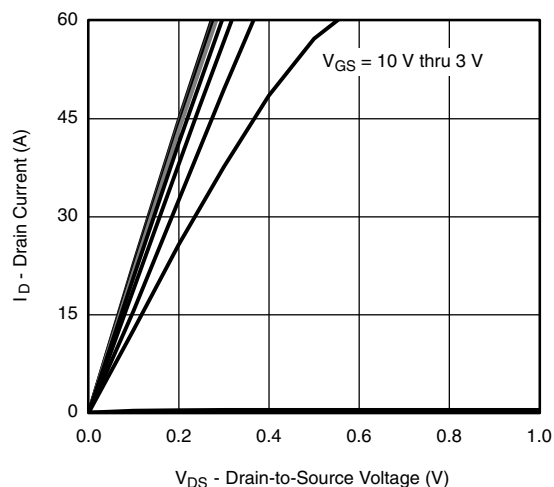
Normalized Thermal Transient Impedance, Junction-to-Case

SiZ700DT

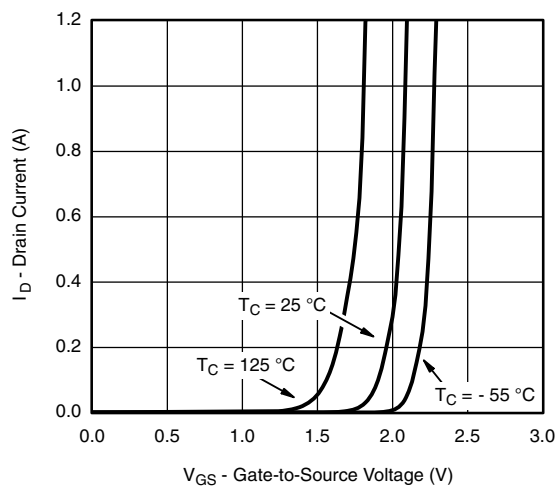
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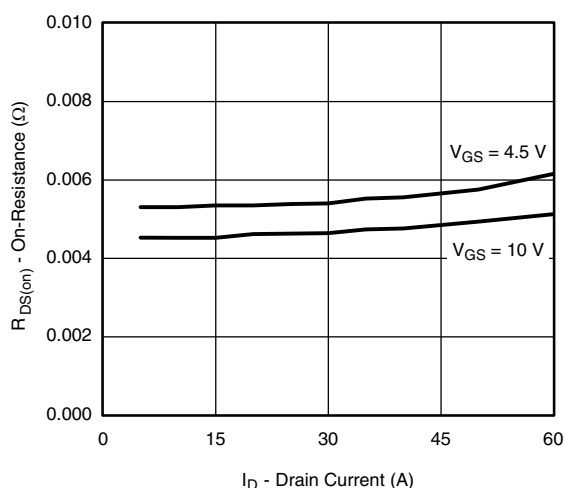
CHANNEL-2 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



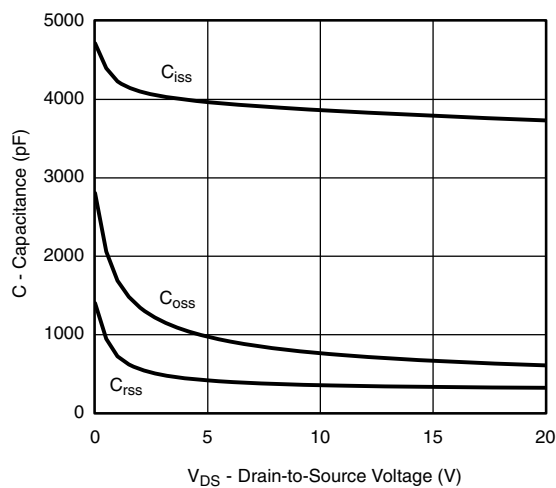
Output Characteristics



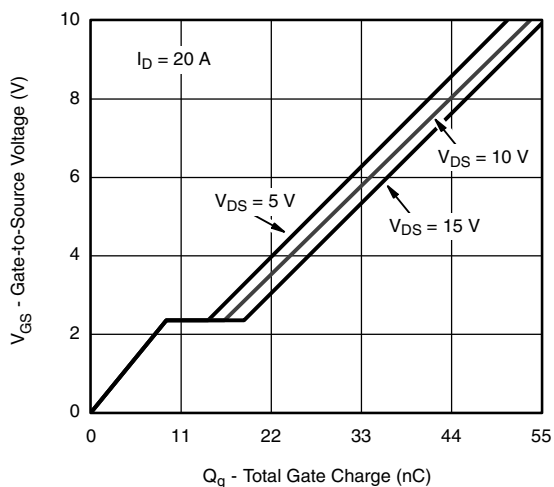
Transfer Characteristics



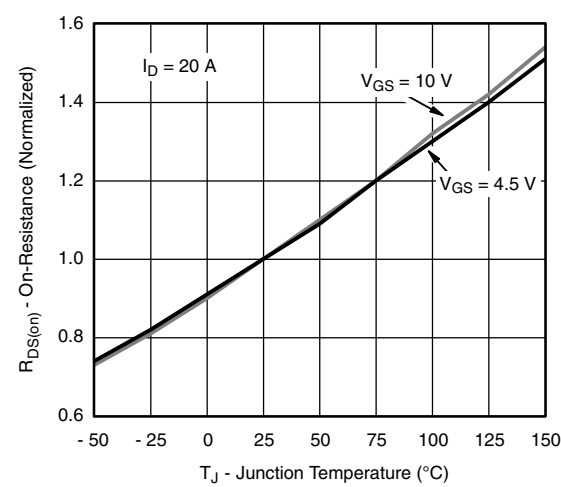
On-Resistance vs. Drain Current



Capacitance



Gate Charge



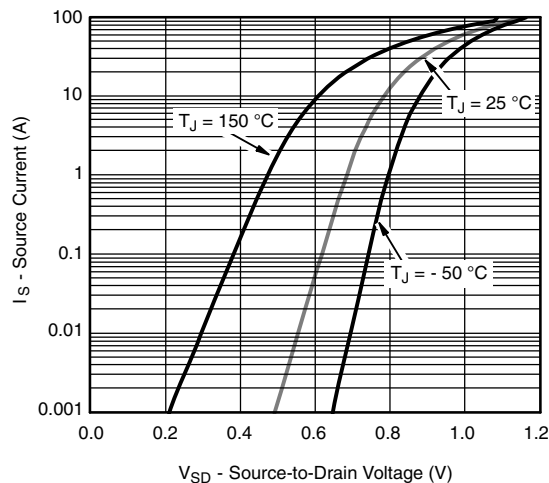
On-Resistance vs. Junction Temperature



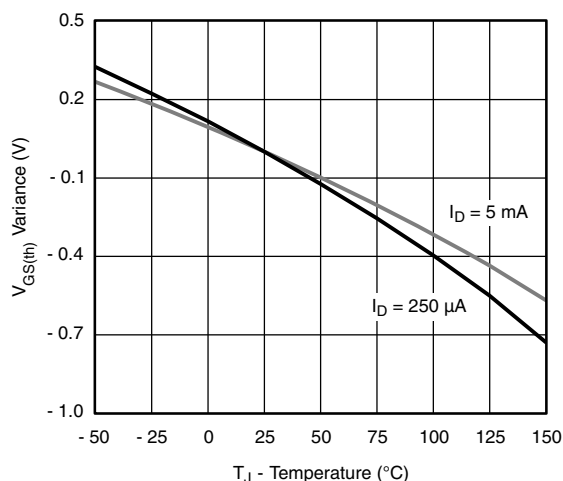
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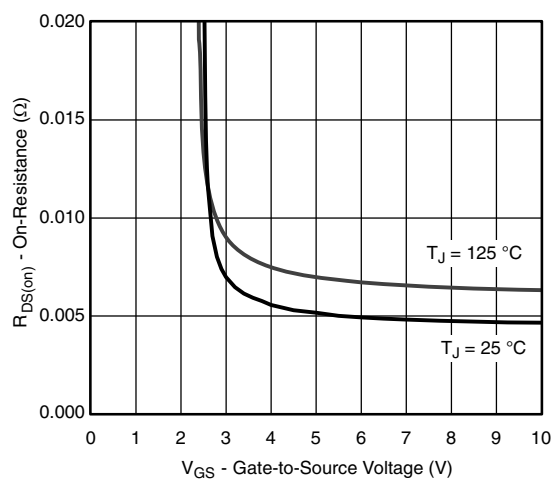
CHANNEL-2 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



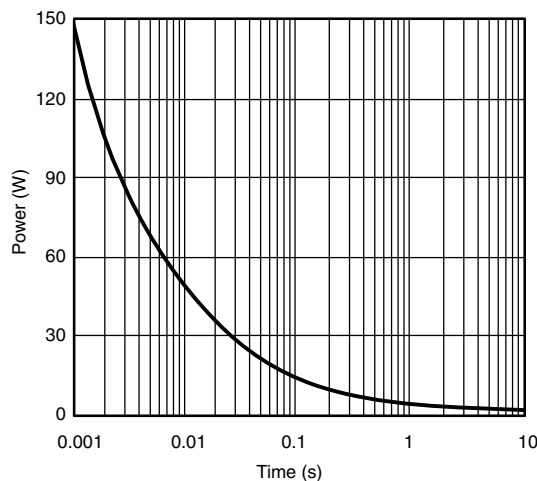
Source-Drain Diode Forward Voltage



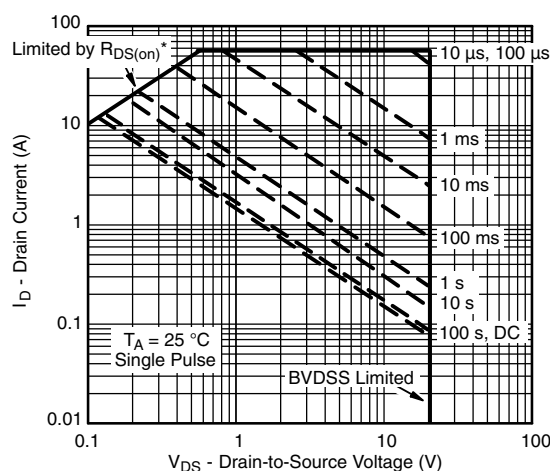
Threshold Voltage



On-Resistance vs. Gate-to-Source Voltage



Single Pulse Power



* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

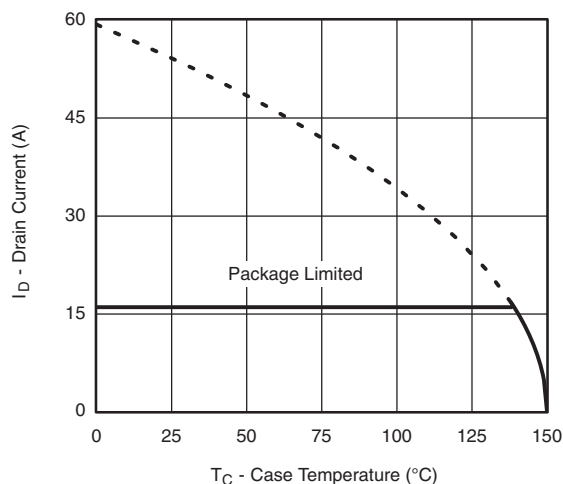
Safe Operating Area, Junction-to-Ambient

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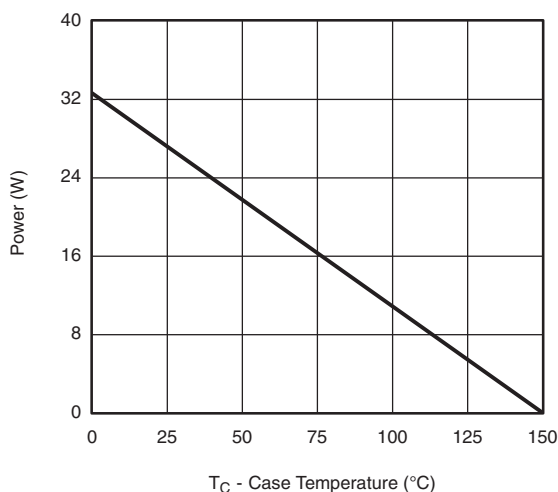
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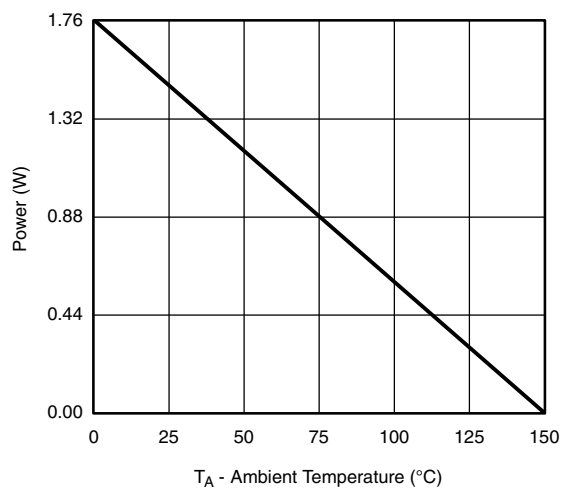
CHANNEL-2 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Current Derating*



Power, Junction-to-Case



Power, Junction-to-Ambient

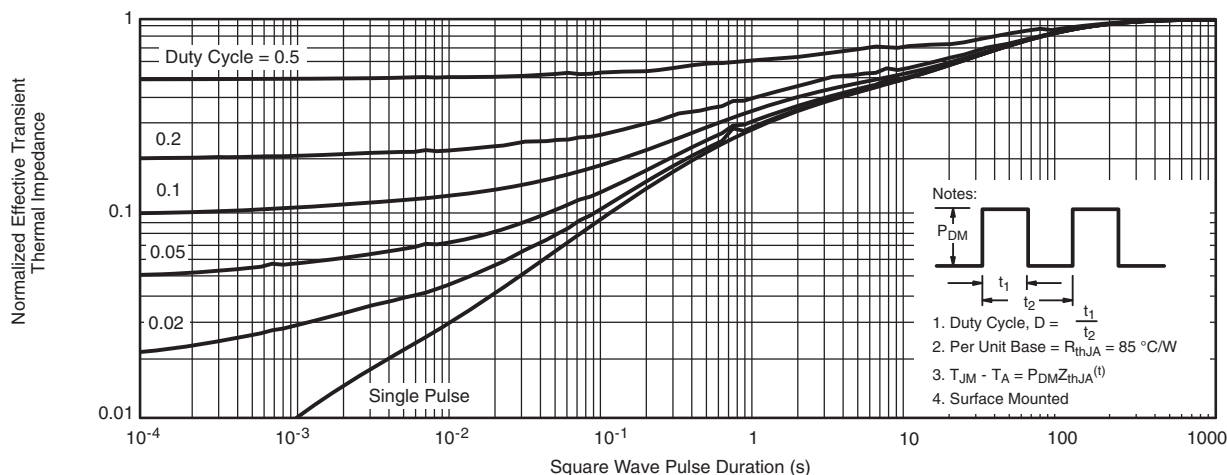
* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



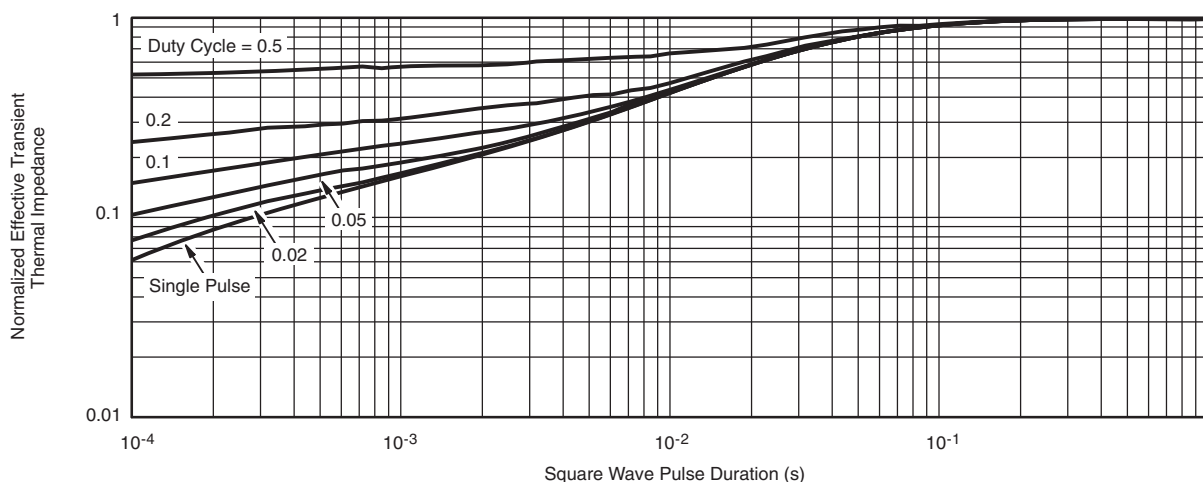
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CHANNEL-2 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

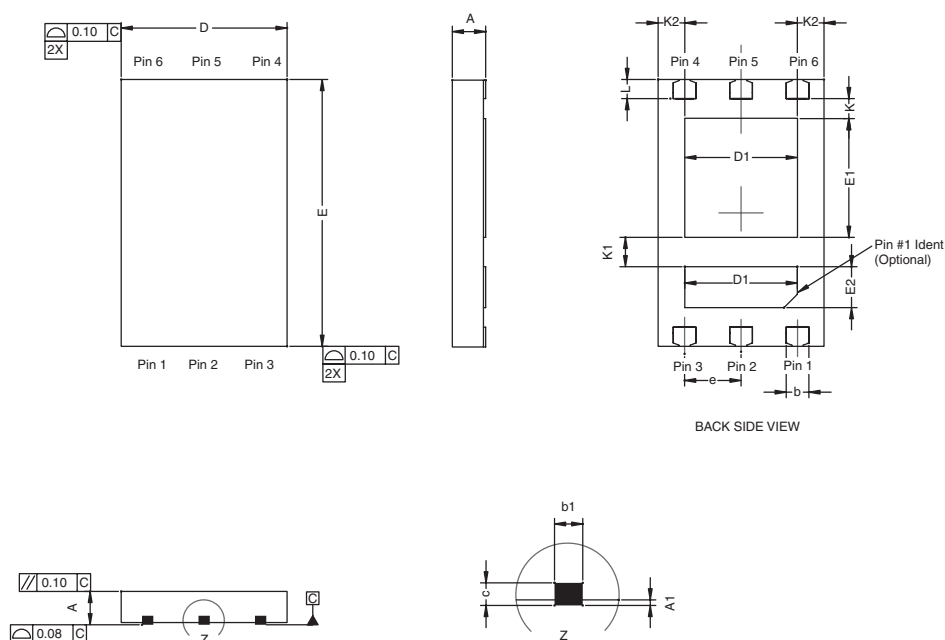
Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?69090.



Package Information

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PowerPAIR™ 6 x 3.7 CASE OUTLINE



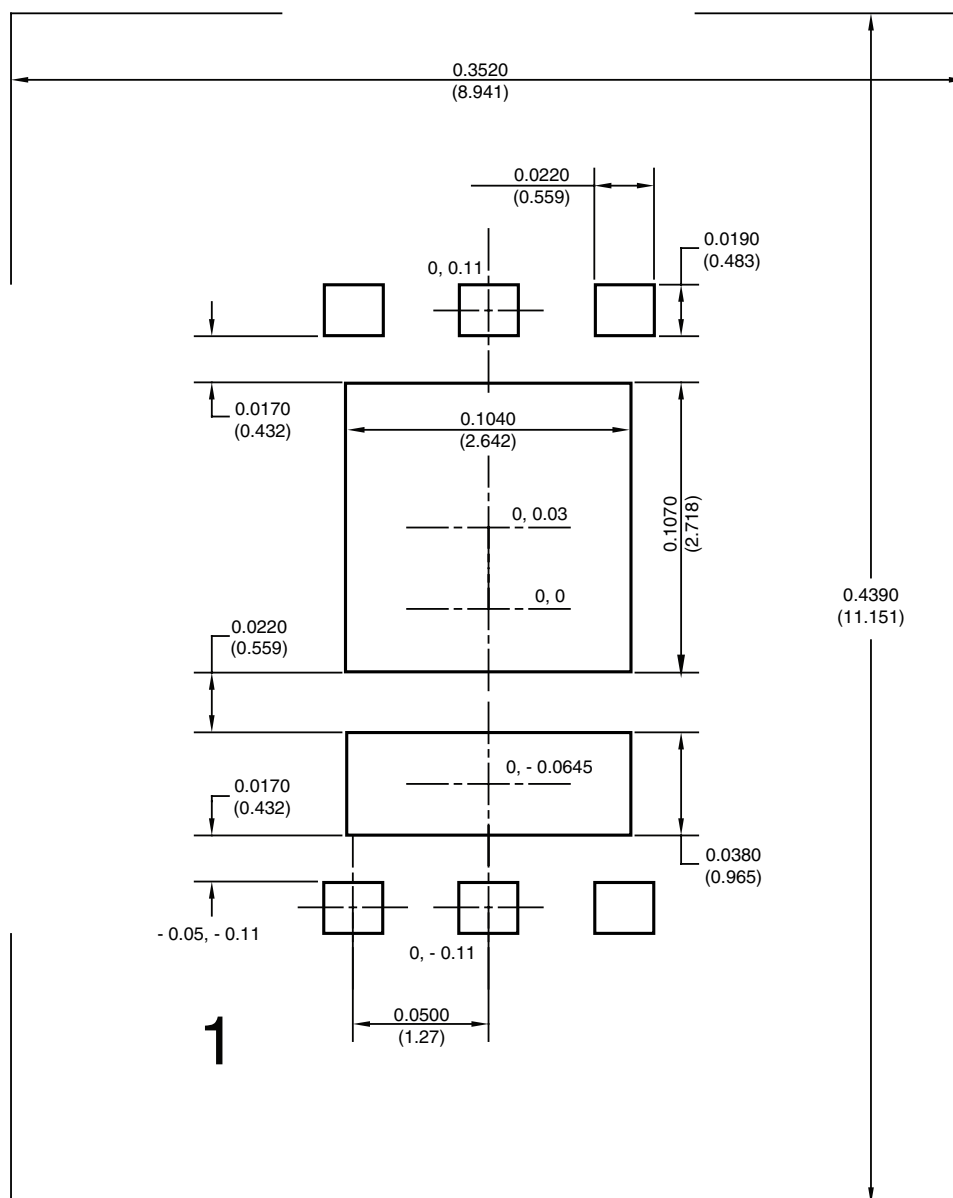
DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.028	0.030	0.032
A1	0.00	-	0.05	0.000	-	0.002
b	0.46	0.51	0.56	0.018	0.020	0.022
b1	0.20	0.25	0.38	0.008	0.010	0.015
C	0.18	0.20	0.23	0.007	0.008	0.009
D	3.65	3.73	3.81	0.144	0.147	0.150
D1	2.41	2.53	2.65	0.095	0.100	0.104
E	5.92	6.00	6.08	0.233	0.236	0.239
E1	2.62	2.67	2.72	0.103	0.105	0.107
E2	0.87	0.92	0.97	0.034	0.036	0.038
e	1.27 BSC			0.05 BSC		
K	0.45 TYP.			0.018 TYP.		
K1	0.66 TYP.			0.026 TYP.		
K2	0.60 TYP.			0.024 TYP.		
L	0.38	0.43	0.48	0.015	0.017	0.019
ECN: S-82772-Rev. B, 17-Nov-08						
DWG: 5979						



PAD Pattern

Vishay Siliconix

RECOMMENDED PAD FOR PowerPAIR™ 6 x 3.7



Recommended PAD for PowerPAIR 6 x 3.7
Dimensions in inches (mm)
Keep-out 0.3520 (8.94) x 0.4390 (11.151)



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