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Vishay/Siliconix SQJ412EP-T1-GE3

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Datasheet of SQJ412EP-T1-GE3 - MOSFET N-CH 40V 32A PPAK SO-8

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SQJ412EP

Vishay Siliconix

Automotive N-Channel 40 V (D-S) 175 °C MOSFET

PRODUCT SUMMARY	
V _{DS} (V)	40
$R_{DS(on)}(\Omega)$ at $V_{GS} = 10 \text{ V}$	0.0041
$R_{DS(on)}(\Omega)$ at $V_{GS} = 4.5 \text{ V}$	0.0052
I _D (A)	32
Configuration	Single



FEATURES

- TrenchFET® Power MOSFET
- AEC-Q101 Qualified^d
- 100 % R_g and UIS Tested
- Material categorization: For definitions of compliance please see www.vishav.com/doc?99912





HALOGEN FREE

PowerPAK® SO-8L Single	Ý
6.15 mm	G
s ¹	N-Channel MOSFET

ORDERING INFORMATION	
Package	PowerPAK SO-8L
Lead (Pb)-free and Halogen-free	SQJ412EP-T1-GE3

ABSOLUTE MAXIMUM RATINGS (T	_C = 25 °C, unles	s otherwise noted	l)	
PARAMETER		SYMBOL	LIMIT	UNIT
Drain-Source Voltage		V_{DS}	40	V
Gate-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current ^a	T _C = 25 °C	1	32	
Continuous Drain Current	T _C = 125 °C	I _D	32	
Continuous Source Current (Diode Conduction)a		I _S	32	А
Pulsed Drain Current ^b		I _{DM}	128	
Single Pulse Avalanche Current	L = 0.1 mH	I _{AS}	53	
Single Pulse Avalanche Energy	L=0.1 mH	E _{AS}	140	mJ
Maximum Dawar Dissinationh	T _C = 25 °C	Р	83	W
Maximum Power Dissipation ^b	T _C = 125 °C	P_D	27	VV
Operating Junction and Storage Temperature Ra	nge	T _J , T _{stg}	- 55 to + 175	°C
Soldering Recommendations (Peak Temperature))e, f		260	C

THERMAL RESISTANCE RATINGS				
PARAMETER		SYMBOL	LIMIT	UNIT
Junction-to-Ambient	PCB Mount ^c	R_{thJA}	65	°C/W
Junction-to-Case (Drain)		R_{thJC}	1.8	C/VV

Notes

- a. Package limited.
- b. Pulse test; pulse width $\leq 300~\mu s,$ duty cycle $\leq 2~\%.$
- c. When mounted on 1" square PCB (FR-4 material).
- d. Parametric verification ongoing.
- See Solder Profile (www.vishav.com/doc?73257). The PowerPAK SO-8L. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.

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PARAMETER	SYMBOL	TES	T CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static				I.	•		
Drain-Source Breakdown Voltage	V _{DS}	$V_{GS} = 0$, $I_D = 250 \mu A$		40	-	-	W
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} =	= V _{GS} , I _D = 250 μA	1.5	2.0	2.5	V
Gate-Source Leakage	I _{GSS}	V _{DS} =	$0 \text{ V}, \text{ V}_{GS} = \pm 20 \text{ V}$	-	-	± 100	nA
		V _{GS} = 0 V	V _{DS} = 40 V	-	-	1	
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V	V _{DS} = 40 V, T _J = 125 °C	-	-	50	μΑ
		V _{GS} = 0 V	V _{DS} = 40 V, T _J = 175 °C	-	-	150	•
On-State Drain Current ^a	I _{D(on)}	V _{GS} = 10 V	$V_{DS} \ge 5 V$	30	-	-	Α
		V _{GS} = 10 V	I _D = 10.3 A	-	0.0035	0.0041	Ω
Dunin Course On Otata Basistanas		V _{GS} = 10 V	I _D = 10.3 A, T _J = 125 °C	-	0.0053	0.0070	
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = 10 V	I _D = 10.3 A, T _J = 175 °C	-	0.0065	0.0085	
		V _{GS} = 4.5 V	I _D = 8.7 A	-	0.0042	0.0052	
Forward Transconductanceb	9 _{fs}	V _{DS} = 15 V, I _D = 16 A		-	85	-	S
Dynamic ^b					•		
Input Capacitance	C _{iss}			-	4950	5950	
Output Capacitance	Coss	$V_{GS} = 0 V$	$V_{DS} = 20 \text{ V}, f = 1 \text{ MHz}$	-	630	760	pF
Reverse Transfer Capacitance	C _{rss}	1		-	270	330	
Total Gate Charge ^c	Qg			-	80	120	
Gate-Source Charge ^c	Q _{gs}	V _{GS} = 10 V	$V_{DS} = 20 \text{ V}, I_{D} = 10 \text{ A}$	-	13.1	-	nC
Gate-Drain Charge ^c	Q_{gd}	1		-	12.3	-	
Gate Resistance	R_g		f = 1 MHz		0.72	1.08	Ω
Turn-On Delay Time ^c	t _{d(on)}			-	45	55	
Rise Time ^c	t _r	$V_{DD} = 20 \text{ V}, \text{ R}_L = 2 \Omega$ $I_D \cong 10 \text{ A}, \text{ V}_{GEN} = 4.5 \text{ V}, \text{ R}_g = 6 \Omega$		-	150	180	- ns
Turn-Off Delay Time ^c	t _{d(off)}			-	50	60	
Fall Time ^c	t _f			-	55	70	
Source-Drain Diode Ratings and Char-	acteristics ^b				•		
Pulsed Current ^a	I _{SM}			-	-	128	Α
Forward Voltage	V_{SD}	I _F :	= 10 A, V _{GS} = 0	-	0.8	1.1	V

Notes

- a. Pulse test; pulse width $\leq 300~\mu s,$ duty cycle $\leq 2~\%.$
- b. Guaranteed by design, not subject to production testing.
- c. Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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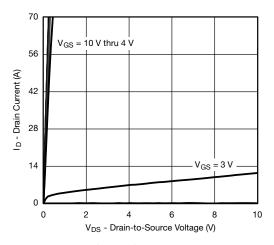
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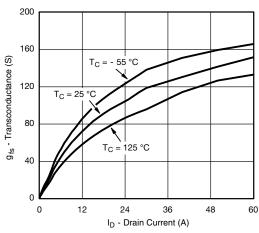
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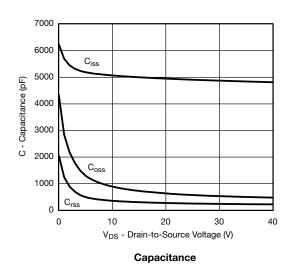
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



Output Characteristics



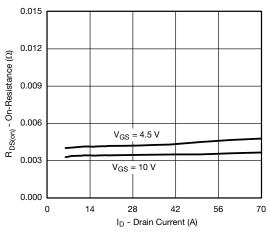
Transconductance



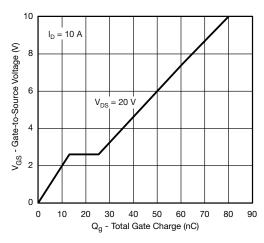
70
56
42
14
T_C = 25 °C
T_C = -55 °C

V_{GS} - Gate-to-Source Voltage (V)

Transfer Characteristics



On-Resistance vs. Drain Current



Gate Charge

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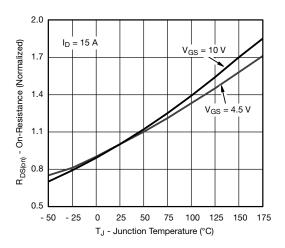
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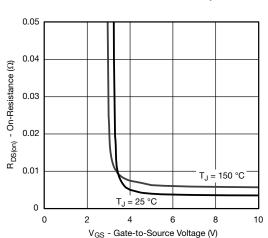
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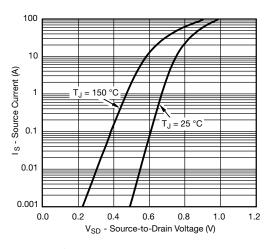
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



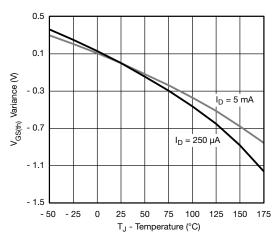
On-Resistance vs. Junction Temperature



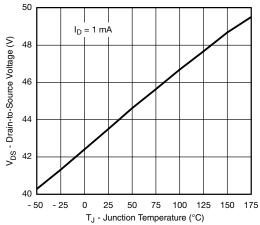
On-Resistance vs. Gate-to-Source Voltage



Source Drain Diode Forward Voltage



Threshold Voltage



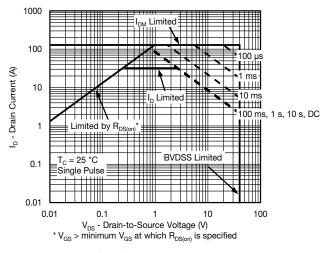
Drain Source Breakdown vs. Junction Temperature



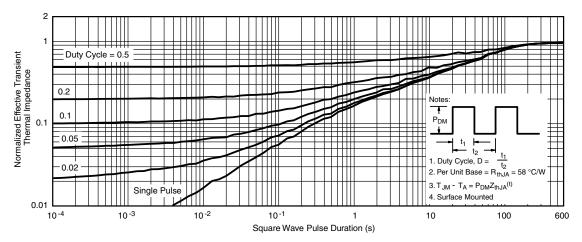
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THERMAL RATINGS (T_A = 25 °C, unless otherwise noted)



Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Ambient

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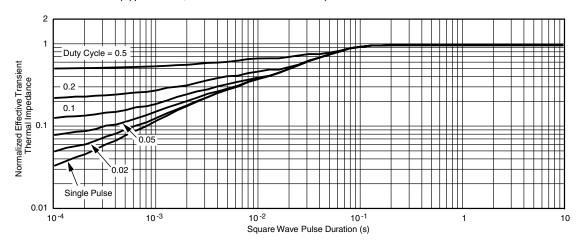


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THERMAL RATINGS (T_A = 25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Case

Note

- The characteristics shown in the two graphs
 - Normalized Transient Thermal Impedance Junction-to-Ambient (25 °C)
 - Normalized Transient Thermal Impedance Junction-to-Case (25 °C) are given for general guidelines only to enable the user to get a "ball park" indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?65935.

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Ordering Information

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PowerPAK® SO-8L

Ordering codes for the SQ rugged series power MOSFETs in the PowerPAK SO-8L package:

DATASHEET PART NUMBER	OLD ORDERING CODE a	NEW ORDERING CODE	
SQJ200EP	-	SQJ200EP-T1_GE3	
SQJ202EP	-	SQJ202EP-T1_GE3	
SQJ401EP	SQJ401EP-T1-GE3	SQJ401EP-T1_GE3	
SQJ402EP	SQJ402EP-T1-GE3	SQJ402EP-T1_GE3	
SQJ403EEP	SQJ403EEP-T1-GE3	SQJ403EEP-T1_GE3	
SQJ403EP	-	SQJ403EP-T1_GE3	
SQJ410EP	SQJ410EP-T1-GE3	SQJ410EP-T1_GE3	
SQJ412EP	SQJ412EP-T1-GE3	SQJ412EP-T1_GE3	
SQJ416EP	-	SQJ416EP-T1_GE3	
SQJ418EP	-	SQJ418EP-T1_GE3	
SQJ422EP	SQJ422EP-T1-GE3	SQJ422EP-T1_GE3	
SQJ423EP		SQJ423EP-T1_GE3	
SQJ431EP	SQJ431EP-T1-GE3	SQJ431EP-T1_GE3	
SQJ443EP	SQJ443EP-T1-GE3	SQJ443EP-T1_GE3	
SQJ444EP	<u>-</u>	SQJ444EP-T1_GE3	
SQJ446EP	-	SQJ446EP-T1_GE3	
SQJ456EP	SQJ456EP-T1-GE3	SQJ456EP-T1_GE3	
SQJ457EP	•	SQJ457EP-T1_GE3	
SQJ459EP	-	SQJ459EP-T1_GE3	
SQJ460AEP	•	SQJ460AEP-T1_GE3	
SQJ461EP	SQJ461EP-T1-GE3	SQJ461EP-T1_GE3	
SQJ463EP	SQJ463EP-T1-GE3	SQJ463EP-T1_GE3	
SQJ465EP	SQJ465EP-T1-GE3	SQJ465EP-T1_GE3	
SQJ469EP	SQJ469EP-T1-GE3	SQJ469EP-T1_GE3	
SQJ474EP	-	SQJ474EP-T1_GE3	
SQJ476EP	-	SQJ476EP-T1_GE3	
SQJ479EP	-	SQJ479EP-T1_GE3	
SQJ486EP	SQJ486EP-T1-GE3	SQJ486EP-T1_GE3	
SQJ488EP	SQJ488EP-T1-GE3	SQJ488EP-T1_GE3	
SQJ500AEP	SQJ500AEP-T1-GE3	SQJ500AEP-T1_GE3	
SQJ840EP	SQJ840EP-T1-GE3	SQJ840EP-T1_GE3	
SQJ844AEP	SQJ844AEP-T1-GE3	SQJ844AEP-T1_GE3	
SQJ850EP	SQJ850EP-T1-GE3	SQJ850EP-T1_GE3	
SQJ858AEP	SQJ858AEP-T1-GE3	SQJ858AEP-T1_GE3	
SQJ868EP	-	SQJ868EP-T1_GE3	
SQJ886EP	SQJ886EP-T1-GE3	SQJ886EP-T1_GE3	
SQJ910AEP	SQJ910AEP-T1-GE3	SQJ910AEP-T1_GE3	
SQJ912AEP	SQJ912AEP-T1-GE3	SQJ912AEP-T1_GE3	
SQJ940EP	SQJ940EP-T1-GE3	SQJ940EP-T1_GE3	
SQJ942EP	SQJ942EP-T1-GE3	SQJ942EP-T1_GE3	
SQJ951EP	SQJ951EP-T1-GE3	SQJ951EP-T1_GE3	
SQJ952EP	-	SQJ952EP-T1_GE3	
SQJ956EP	SQJ956EP-T1-GE3	SQJ956EP-T1_GE3	
SQJ960EP	SQJ960EP-T1-GE3	SQJ960EP-T1_GE3	
SQJ963EP	SQJ963EP-T1-GE3	SQJ963EP-T1_GE3	
SQJ968EP	SQJ968EP-T1-GE3	SQJ968EP-T1_GE3	
SQJ980AEP	SQJ980AEP-T1-GE3	SQJ980AEP-T1_GE3	
SQJ992EP	SQJ992EP-T1-GE3	SQJ992EP-T1_GE3	

Note

a. Old ordering code is obsolete and no longer valid for new orders

Revision: 01-Jul-16 1 Document Number: 65804

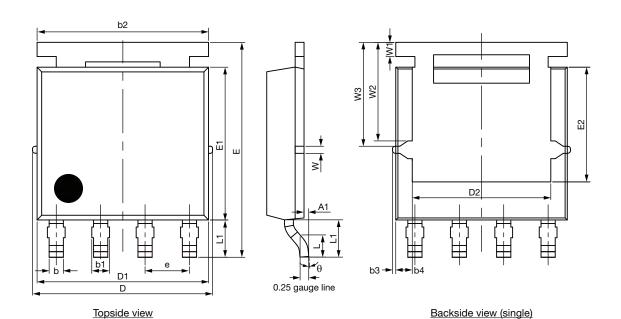


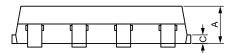


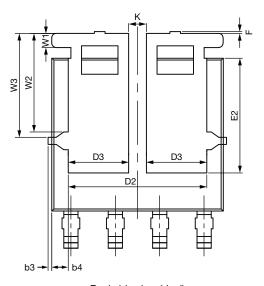
Package Information

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PowerPAK® SO-8L Case Outline for Non-Al Parts







Backside view (dual)

Revision: 16-May-16 Document Number: 69003

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Package Information

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D114	MILLIMETERS			INCHES			
DIM.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
Α	1.00	1.07	1.14	0.039	0.042	0.045	
A1	0.00	-	0.127	0.00	-	0.005	
b	0.33	0.41	0.48	0.013	0.016	0.019	
b1	0.44	0.51	0.58	0.017	0.020	0.023	
b2	4.80	4.90	5.00	0.189	0.193	0.197	
b3		0.094			0.004	•	
b4		0.47			0.019		
С	0.20	0.25	0.30	0.008	0.010	0.012	
D	5.00	5.13	5.25	0.197	0.202	0.207	
D1	4.80	4.90	5.00	0.189	0.193	0.197	
D2	3.86	3.96	4.06	0.152	0.156	0.160	
D3	1.63	1.73	1.83	0.064	0.068	0.072	
е		1.27 BSC			0.050 BSC		
E	6.05	6.15	6.25	0.238	0.242	0.246	
E1	4.27	4.37	4.47	0.168	0.172	0.176	
E2	3.18	3.28	3.38	0.125	0.129	0.133	
F	-	-	0.15	-	-	0.006	
L	0.62	0.72	0.82	0.024	0.028	0.032	
L1	0.92	1.07	1.22	0.036	0.042	0.048	
K		0.51	•		0.020	•	
W		0.23			0.009		
W1	0.41			0.016			
W2	2.82			0.111			
W3		2.96			0.117		
θ	0°	-	10°	0°	-	10°	

ECN: T16-0221-Rev. D, 16-May-16

DWG: 5976

Note

• Millimeters will gover

Revision: 16-May-16 2 Document Number: 69003

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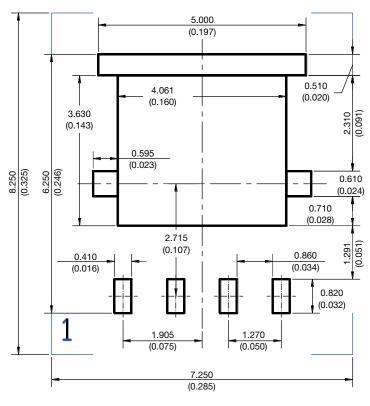
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PAD Pattern

Vishay Siliconix

RECOMMENDED MINIMUM PAD FOR PowerPAK® SO-8L SINGLE



Recommended Minimum Pads Dimensions in mm (inches)



Datasheet of SQJ412EP-T1-GE3 - MOSFET N-CH 40V 32A PPAK SO-8

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Revision: 13-Jun-16 1 Document Number: 91000