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SUD50N04-16P

Vishay Siliconix

N-Channel 40-V (D-S), 175 °C MOSFET

PRODUCT SUMMARY			
V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A) ^{a, c}	Q _g (Typ.)
40	0.016 at V _{GS} = 10 V	20	15.6 nC
	0.018 at V _{GS} = 4.5 V	20	

FEATURES

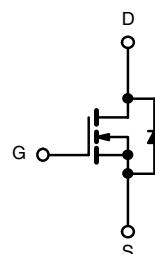
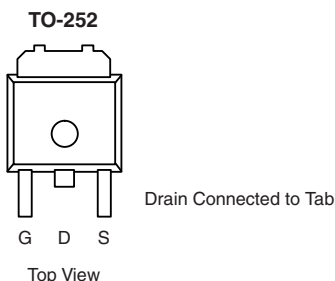
- TrenchFET[®] Power MOSFET
- 100 % R_g and UIS Tested



RoHS
COMPLIANT

APPLICATIONS

- LCD TV Inverter
- Secondary Synchronous Rectification



Ordering Information: SUD50N04-16P-E3 (Lead (Pb)-free)

N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS T _A = 25 °C, unless otherwise noted				
Parameter	Symbol	Limit	Unit	
Drain-Source Voltage	V _{DS}	40	V	
Gate-Source Voltage	V _{GS}	± 16		
Continuous Drain Current (T _J = 150 °C)	I _D	T _C = 25 °C	20 ^c	
		T _C = 100 °C	20 ^c	
		T _A = 25 °C	9.8 ^b	
		T _A = 100 °C	6.8 ^b	
Pulsed Drain Current	I _{DM}	50	A	
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C		20 ^c
		T _A = 25 °C		2.5 ^b
Single Pulse Avalanche Current	I _{AS}	20	mJ	
Avalanche Energy	E _{AS}	20		
Maximum Power Dissipation	P _D	T _C = 25 °C	35.7	
		T _C = 100 °C	17.8	
		T _A = 25 °C	3.1 ^b	
		T _A = 100 °C	1.5 ^b	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to 175	°C	

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^b	Steady State	R _{thJA}	40	50	°C/W
Maximum Junction-to-Case	Steady State	R _{thJC}	3.4	5.3	

Notes:

a. Based on T_C = 25 °C.

b. Surface Mounted on 1" x 1" FR4 board.

c. Package limited.

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SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	40			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 250\text{ }\mu\text{A}$		38		mV/°C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			-5.4		
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	0.8		2.2	V
Gate-Source Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 16\text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 40\text{ V}, V_{GS} = 0\text{ V}$			1	μA
		$V_{DS} = 40\text{ V}, V_{GS} = 0\text{ V}, T_J = 100\text{ }^\circ\text{C}$			20	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}, V_{GS} = 10\text{ V}$	30			A
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 15\text{ A}$		0.0125	0.016	Ω
		$V_{GS} = 4.5\text{ V}, I_D = 10\text{ A}$		0.014	0.018	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 15\text{ V}, I_D = 15\text{ A}$		58		S
Dynamic^b						
Input Capacitance	C_{iss}	$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		1655		pF
Output Capacitance	C_{oss}			200		
Reverse Transfer Capacitance	C_{rss}			152		
Total Gate Charge	Q_g	$V_{DS} = 20\text{ V}, V_{GS} = 10\text{ V}, I_D = 30\text{ A}$		39.2	60	nC
Gate-Source Charge	Q_{gs}	$V_{DS} = 20\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 30\text{ A}$		15.6	24	
Gate-Drain Charge	Q_{gd}			4.2		
Gate Resistance	R_g		$f = 1\text{ MHz}$		2.1	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 20\text{ V}, R_L = 0.66\text{ }\Omega$ $I_D \cong 30\text{ A}, V_{GEN} = 4.5\text{ V}, R_g = 1\text{ }\Omega$		19	30	ns
Rise Time	t_r			120	180	
Turn-Off Delay Time	$t_{d(off)}$			40	60	
Fall Time	t_f			36	55	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 20\text{ V}, R_L = 0.66\text{ }\Omega$ $I_D \cong 30\text{ A}, V_{GEN} = 10\text{ V}, R_g = 1\text{ }\Omega$		8	16	
Rise Time	t_r			22	35	
Turn-Off Delay Time	$t_{d(off)}$			24	36	
Fall Time	t_f			8	16	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	$T_C = 25\text{ }^\circ\text{C}$			20	A
Pulse Diode Forward Current ^a	I_{SM}				50	
Body Diode Voltage	V_{SD}	$I_S = 10\text{ A}$		0.84	1.2	V
Body Diode Reverse Recovery Time	t_{rr}	$I_F = 20\text{ A}, di/dt = 100\text{ A}/\mu\text{s}, T_J = 25\text{ }^\circ\text{C}$		25	38	ns
Body Diode Reverse Recovery Charge	Q_{rr}			22	33	nC
Reverse Recovery Fall Time	t_a			15		ns
Reverse Recovery Rise Time	t_b			10		

Notes:

 a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

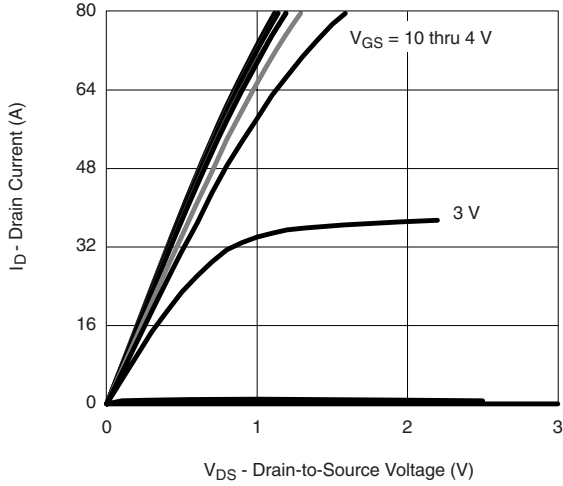
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

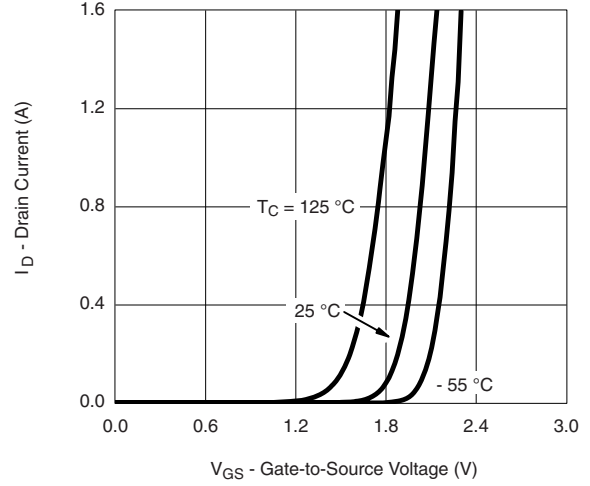


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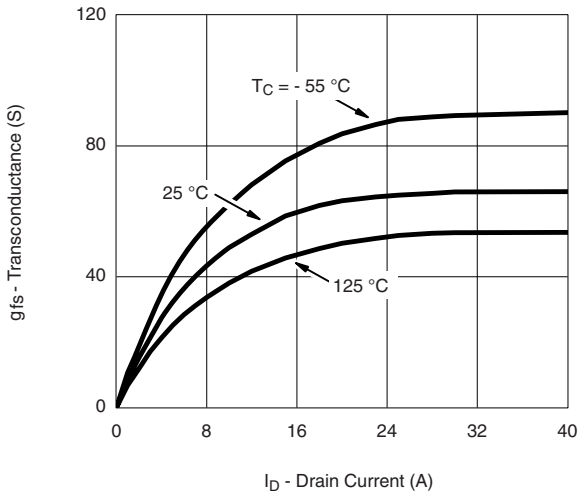
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



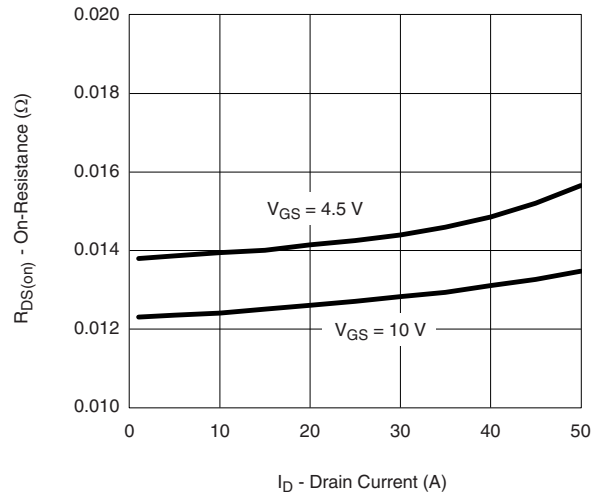
Output Characteristics



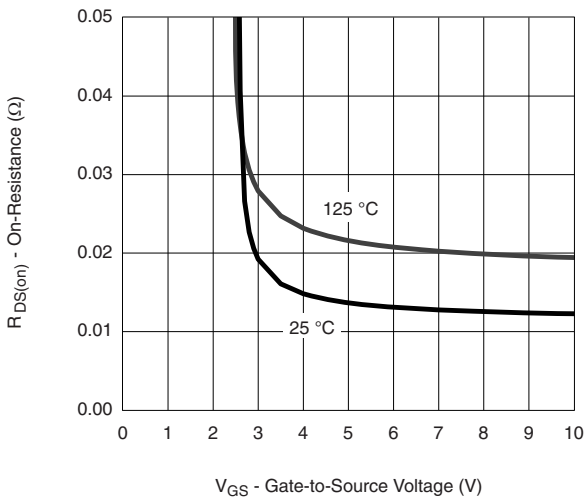
Transfer Characteristics



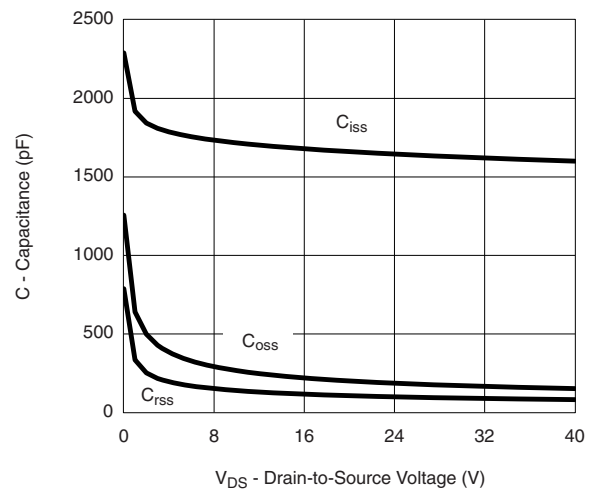
Transconductance



On-Resistance vs. Drain Current



On-Resistance vs. Gate-to-Source Voltage



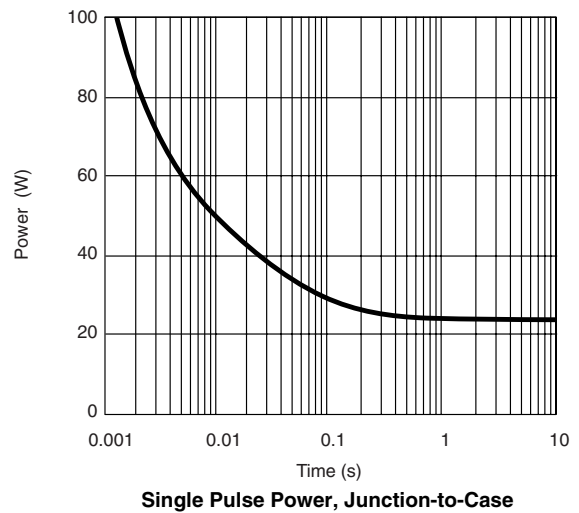
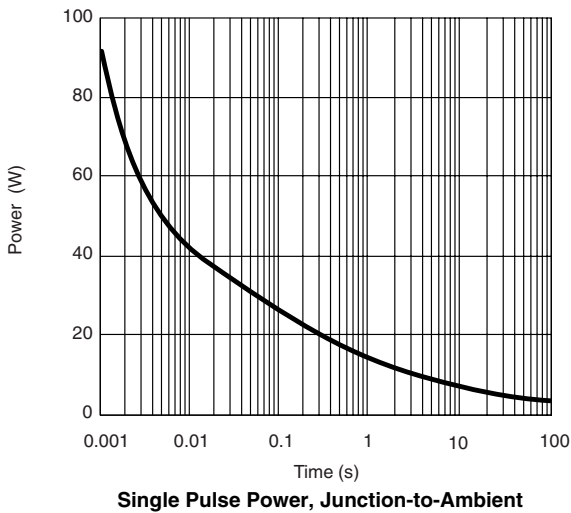
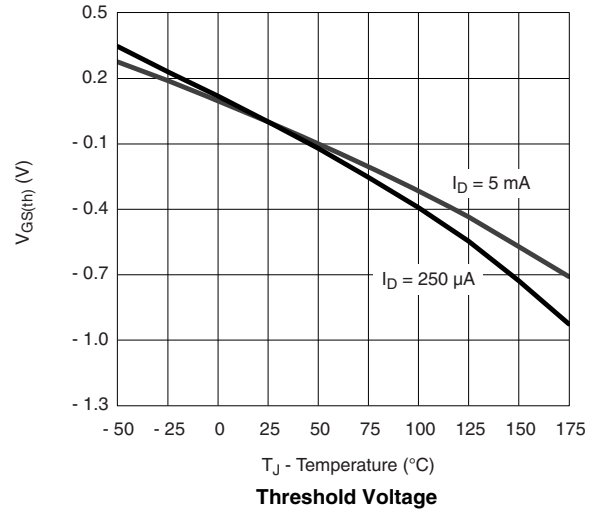
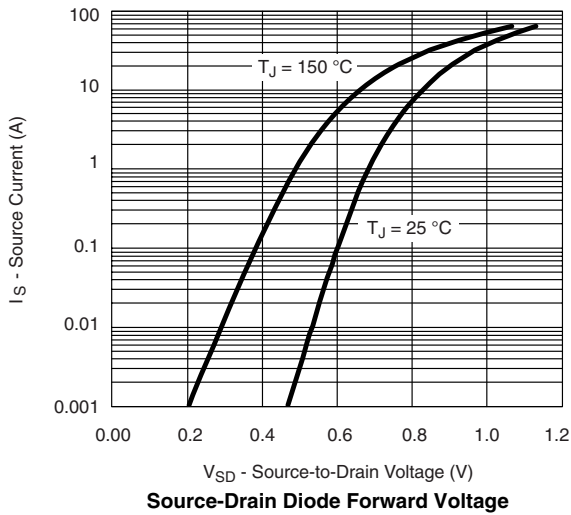
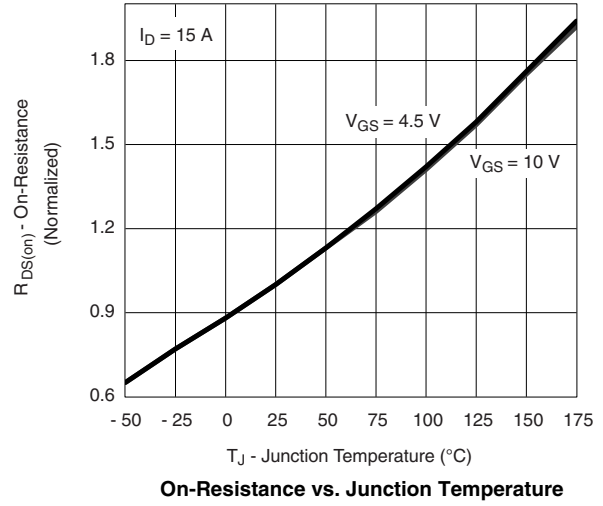
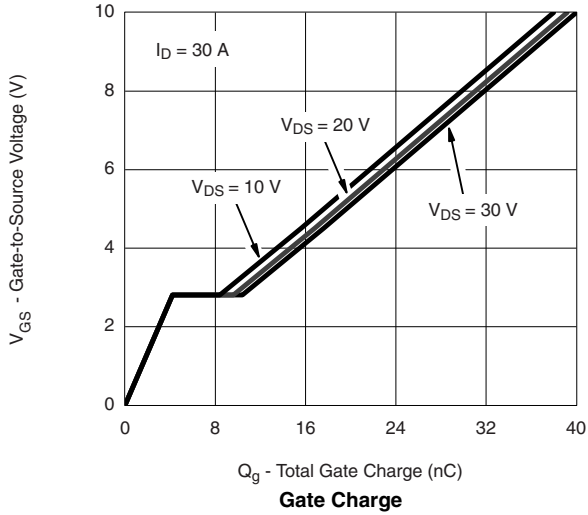
Capacitance

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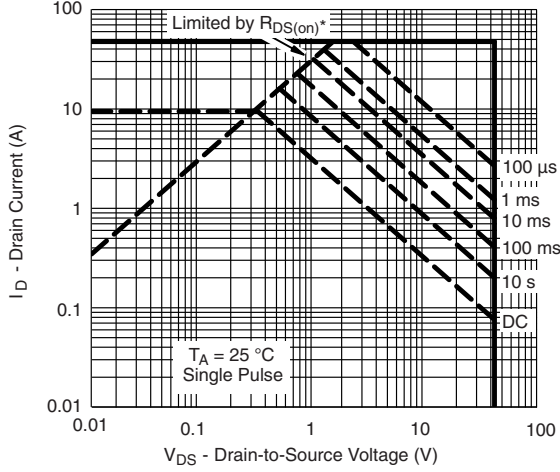
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



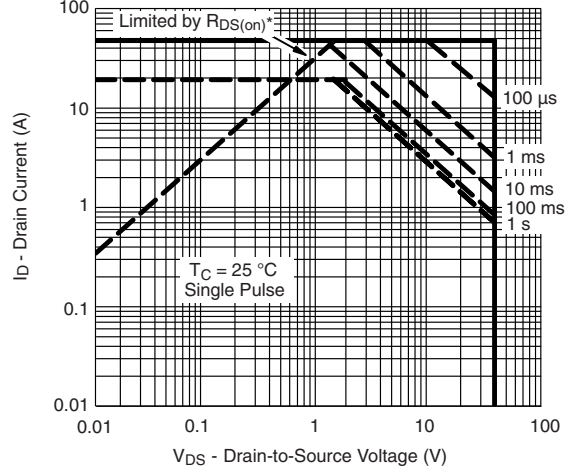


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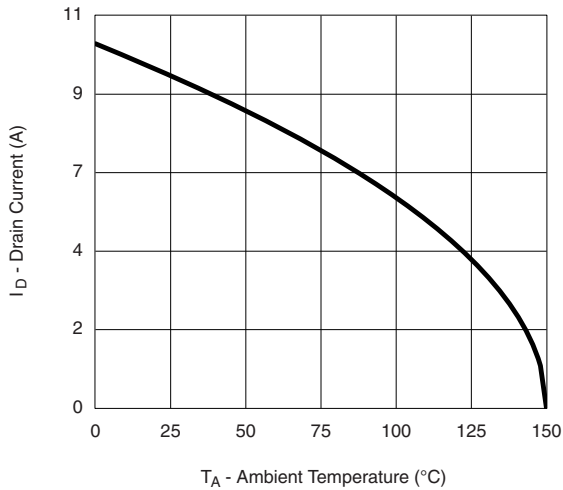
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



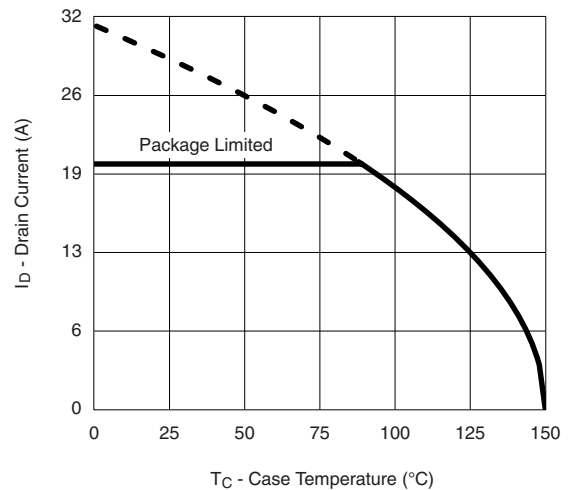
* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified
Safe Operating Area, Junction-to-Ambient



* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified
Safe Operating Area, Junction-to-Case



Current Derating, Junction-to-Ambient**



Current Derating, Junction-to-Case**

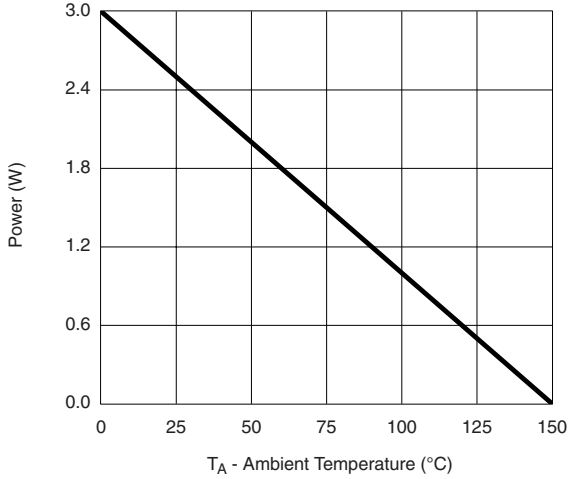
** The power dissipation P_D is based on $T_{J(max)} = 175$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

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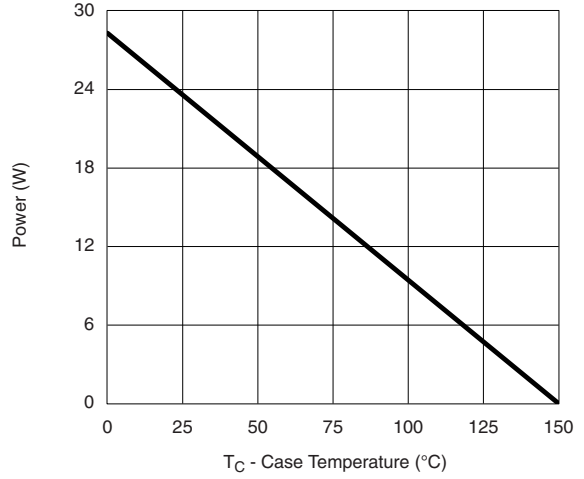
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TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Power Derating*, Junction-to-Ambient



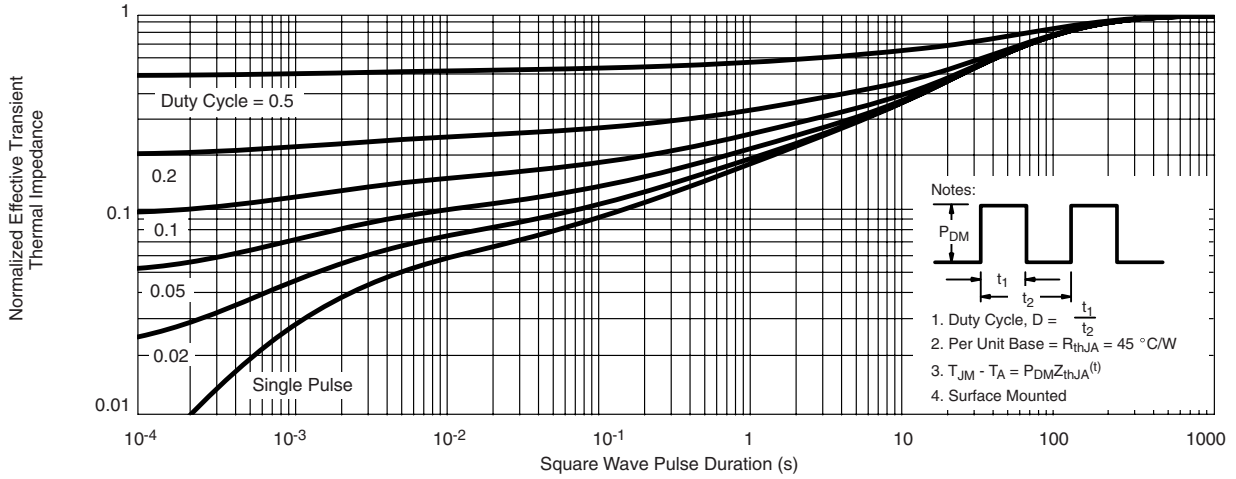
Power Derating*, Junction-to-Case

* The power dissipation P_D is based on $T_{J(max)} = 175\text{ °C}$, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

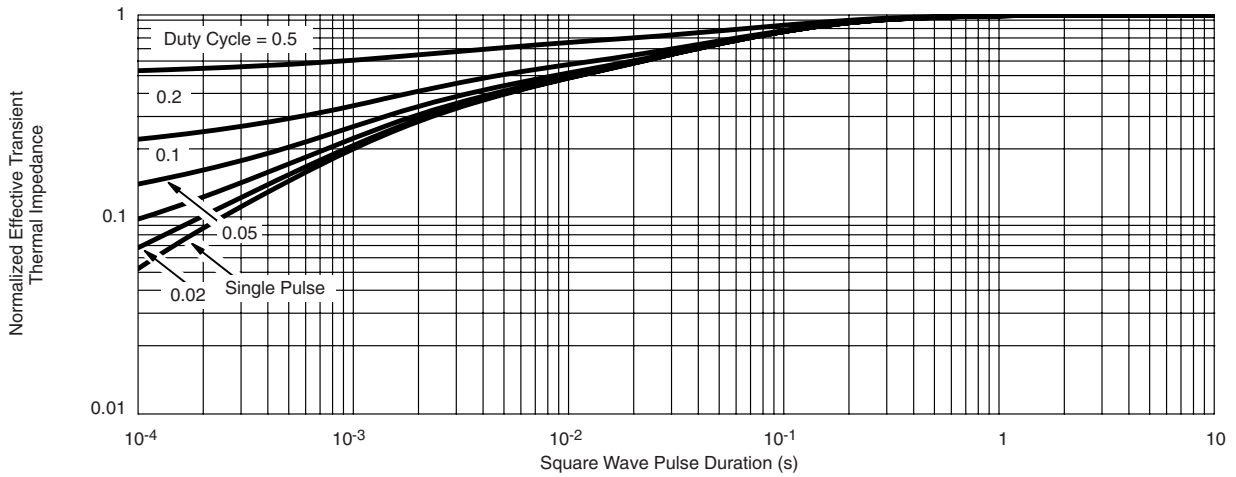


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TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <http://www.vishay.com/ppg?74477>.



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