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SUM60N02-3m9P

Vishay Siliconix

N-Channel 20-V (D-S) 175 °C MOSFET

PRODUCT SUMMARY

$V_{(BR)DSS}$ (V)	$r_{DS(on)}$ (Ω)	I_D (A) ^a
20	0.0039 at $V_{GS} = 10$ V	60
	0.0052 at $V_{GS} = 4.5$ V	60

FEATURES

- TrenchFET® Power MOSFET
- 175 °C Junction Temperature
- 100 % R_g Tested
- 100 % UIS Tested

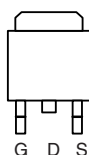


RoHS
COMPLIANT

APPLICATIONS

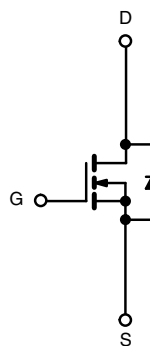
- OR-ing

TO-263



Top View

DRAIN connected to TAB



Ordering Information: SUM60N02-3m9P-E3 (Lead (Pb)-free)

N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS $T_A = 25$ °C, unless otherwise noted

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	20	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current ($T_J = 175$ °C)	I_D	$T_C = 25$ °C	A
		$T_C = 100$ °C	
Pulsed Drain Current	I_{DM}	120	
Single Pulse Avalanche Current	I_{AS}	50	
Single Pulse Avalanche Energy	E_{AS}	125	mJ
Maximum Power Dissipation ^b	P_D	$T_C = 25$ °C	W
		$T_A = 25$ °C ^d	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to 175	°C

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Limit	Unit
Junction-to-Ambient (PCB Mount) ^d	R_{thJA}	40	°C/W
Junction-to-Case	R_{thJC}	1.25	

Notes:

- Package limited.
- Duty cycle ≤ 1 %.
- See SOA curve for voltage derating.
- When mounted on 1" square PCB (FR-4 material).

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SPECIFICATIONS T _J = 25 °C, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{DS} = 0 V, I _D = 250 μA	20			V
Gate-Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	1.0		3	
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 20 V, V _{GS} = 0 V			1	μA
		V _{DS} = 20 V, V _{GS} = 0 V, T _J = 125 °C			50	
		V _{DS} = 20 V, V _{GS} = 0 V, T _J = 175 °C			250	
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 10 V	100			A
Drain-Source On-State Resistance ^a	r _{DS(on)}	V _{GS} = 10 V, I _D = 20 A		0.0031	0.0039	Ω
		V _{GS} = 10 V, I _D = 20 A, T _J = 125 °C			0.0059	
		V _{GS} = 10 V, I _D = 20 A, T _J = 175 °C			0.007	
		V _{GS} = 4.5 V, I _D = 20 A		0.0042	0.0052	
Forward Transconductance ^a	g _{fs}	V _{DS} = 10 V, I _D = 20 A		95		S
Dynamic ^b						
Input Capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = 10 V, f = 1 MHz		5950		pF
Output Capacitance	C _{oss}			985		
Reverse Transfer Capacitance	C _{rss}			365		
Total Gate Charge ^b	Q _g	V _{DS} = 10 V, V _{GS} = 4.5 V, I _D = 50 A		33	50	nC
Gate-Source Charge ^b	Q _{gs}			18		
Gate-Drain Charge ^b	Q _{gd}			7		
Gate Resistance	R _g		0.75	1.5	2.3	Ω
Turn-On Delay Time ^b	t _{d(on)}	V _{DD} = 10 V, R _L = 0.2 Ω I _D ≅ 50 A, V _{GEN} = 10 V, R _g = 1.0 Ω		15	25	ns
Rise Time ^b	t _r			7	11	
Turn-Off Delay Time ^b	t _{d(off)}			35	55	
Fall Time ^b	t _f			8	12	
Source-Drain Diode Ratings and Characteristics T _C = 25 °C ^c						
Continuous Current	I _S				60	A
Pulsed Current	I _{SM}				100	
Forward Voltage ^a	V _{SD}	I _F = 20 A, V _{GS} = 0 V		0.85	1.5	V
Reverse Recovery Time	t _{rr}	I _F = 20 A, di/dt = 100 A/μs		45	90	ns
Peak Reverse Recovery Current	I _{RM}			1.7	3.4	A
Reverse Recovery Charge	Q _{rr}			0.039	0.155	μC

Notes:

a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$

b. Independent of operating temperature.

c. Guaranteed by design, not subject to production testing.

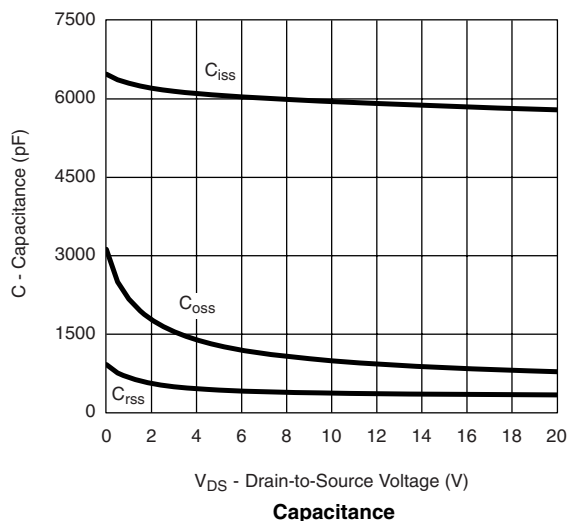
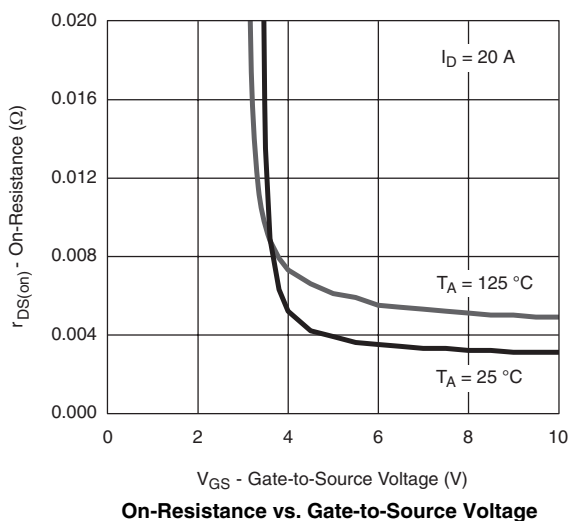
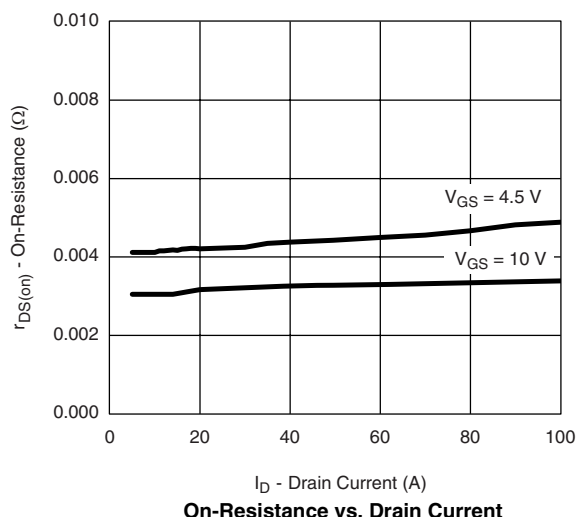
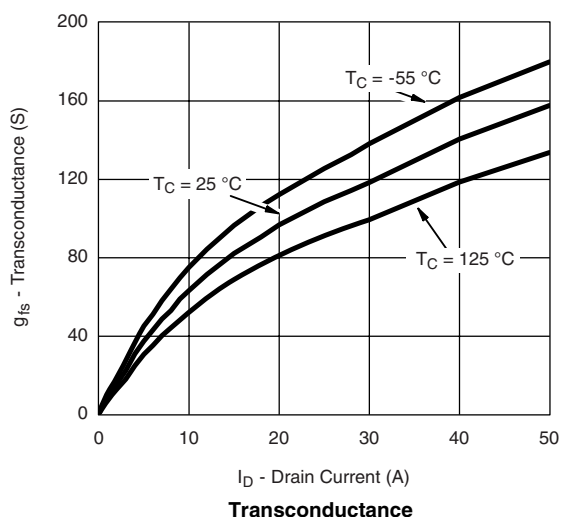
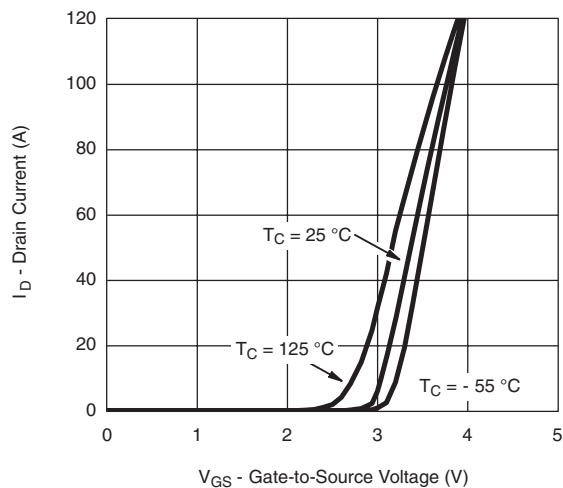
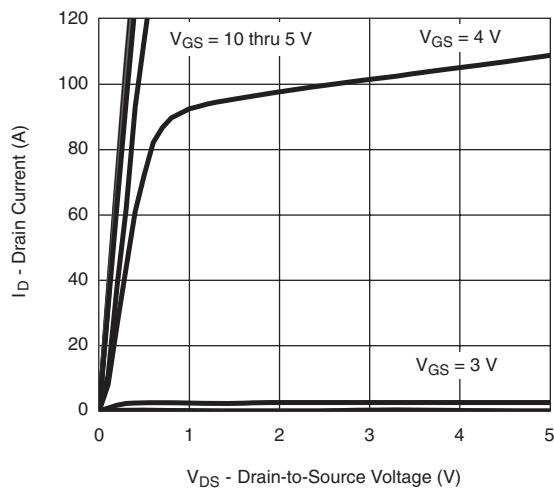
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



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TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

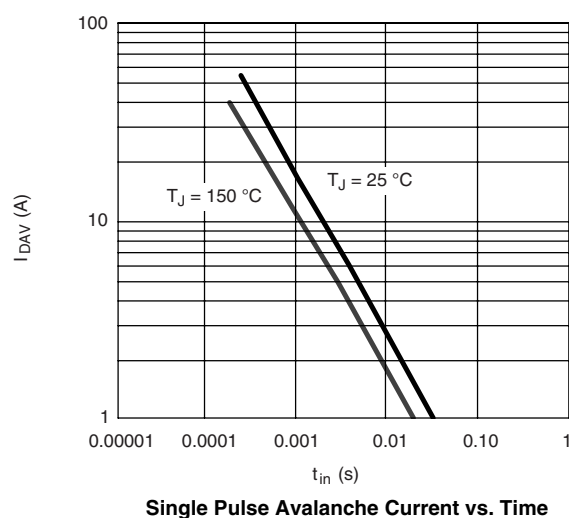
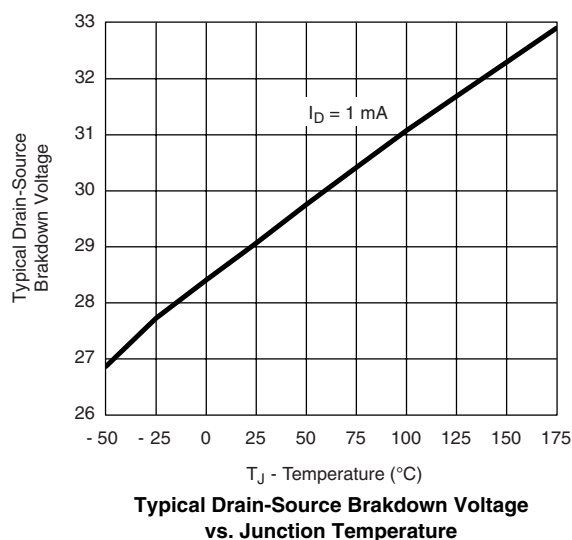
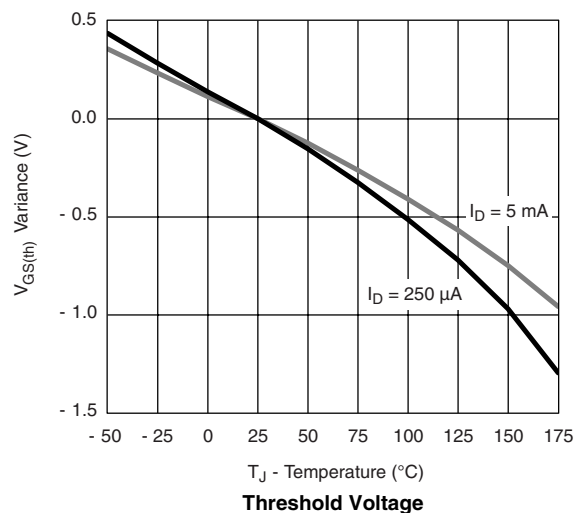
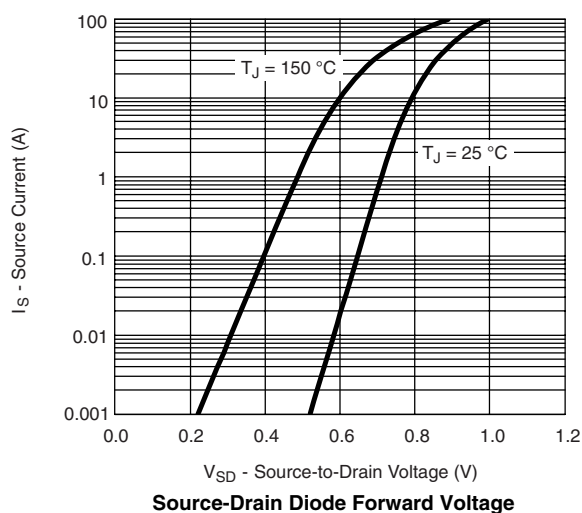
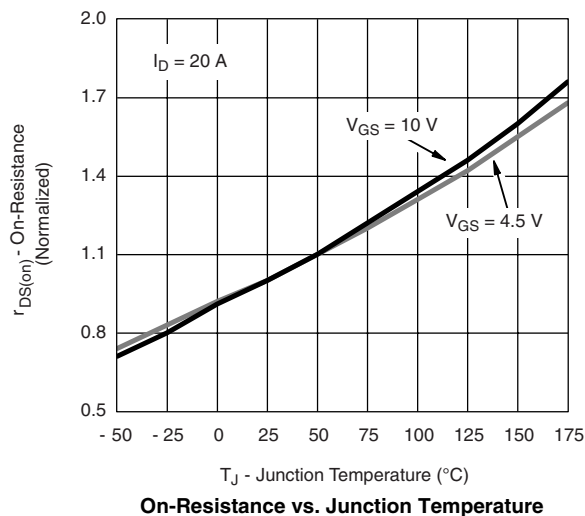
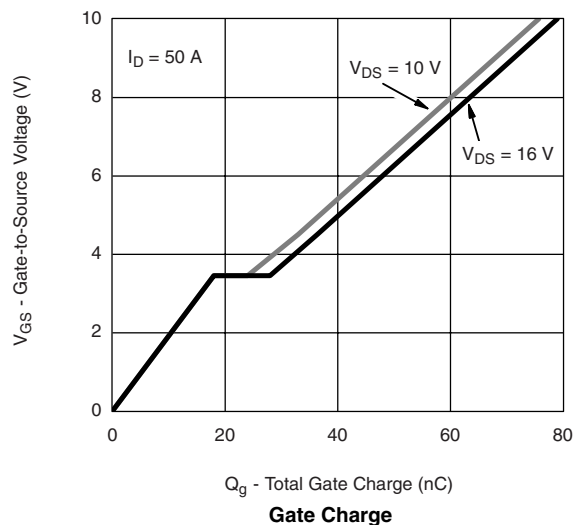


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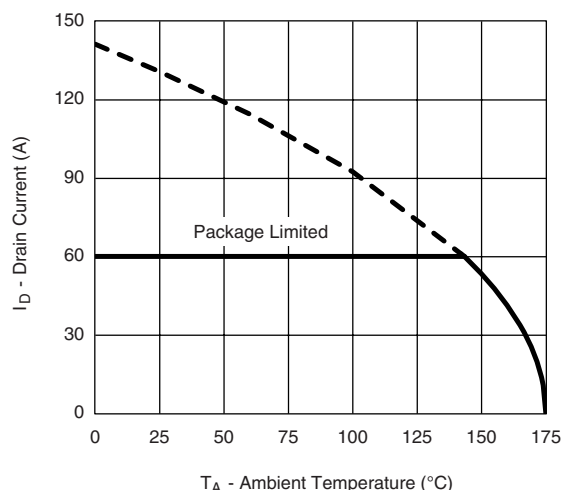




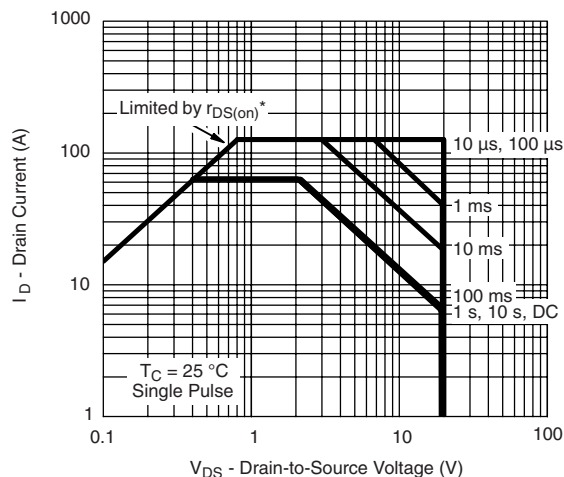
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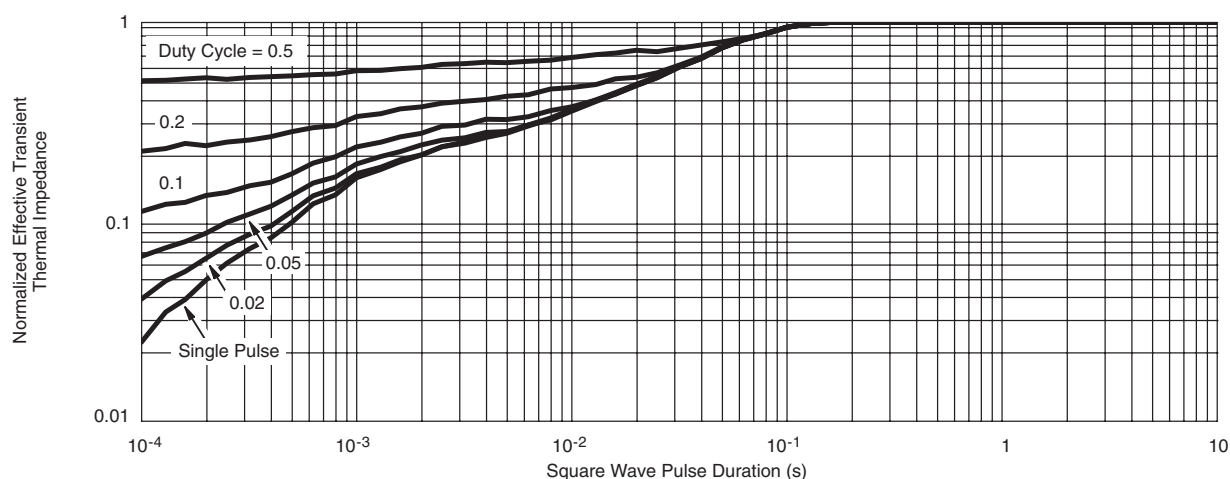


Drain Current vs. Ambient Temperature



* V_{GS} > minimum V_{GS} at which $r_{DS(on)}$ is specified

Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <http://www.vishay.com/ppg?69820>.

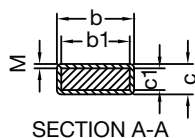
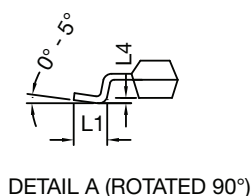
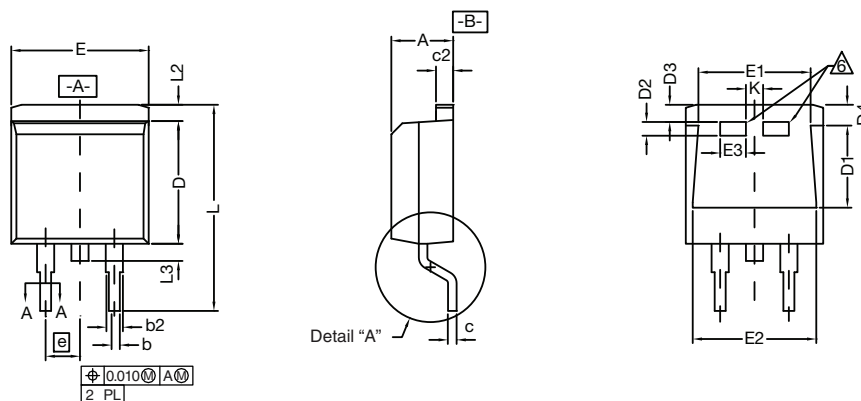


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Package Information

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TO-263 (D²PAK): 3-LEAD



DIM.		INCHES		MILLIMETERS	
		MIN.	MAX.	MIN.	MAX.
A		0.160	0.190	4.064	4.826
b		0.020	0.039	0.508	0.990
b1		0.020	0.035	0.508	0.889
b2		0.045	0.055	1.143	1.397
c*	Thin lead	0.013	0.018	0.330	0.457
	Thick lead	0.023	0.028	0.584	0.711
c1	Thin lead	0.013	0.017	0.330	0.431
	Thick lead	0.023	0.027	0.584	0.685
c2		0.045	0.055	1.143	1.397
D		0.340	0.380	8.636	9.652
D1		0.220	0.240	5.588	6.096
D2		0.038	0.042	0.965	1.067
D3		0.045	0.055	1.143	1.397
D4		0.044	0.052	1.118	1.321
E		0.380	0.410	9.652	10.414
E1		0.245	-	6.223	-
E2		0.355	0.375	9.017	9.525
E3		0.072	0.078	1.829	1.981
e		0.100 BSC		2.54 BSC	
K		0.045	0.055	1.143	1.397
L		0.575	0.625	14.605	15.875
L1		0.090	0.110	2.286	2.794
L2		0.040	0.055	1.016	1.397
L3		0.050	0.070	1.270	1.778
L4		0.010 BSC		0.254 BSC	
M		-	0.002	-	0.050

ECN: T13-0707-Rev. K, 30-Sep-13
DWG: 5843

Notes

- Plane B includes maximum features of heat sink tab and plastic.
- No more than 25 % of L1 can fall above seating plane by max. 8 mils.
- Pin-to-pin coplanarity max. 4 mils.
- *: Thin lead is for SUB, SYB.
Thick lead is for SUM, SYM, SQM.
- Use inches as the primary measurement.
- This feature is for thick lead.

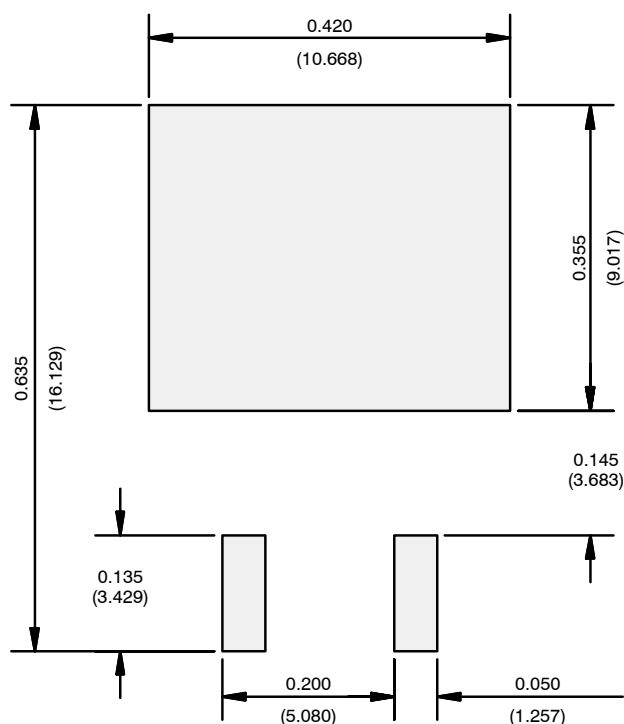
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DWG: 5843



AN826

Vishay Siliconix

RECOMMENDED MINIMUM PADS FOR D²PAK: 3-Lead



Recommended Minimum Pads
Dimensions in Inches/(mm)

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