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Vishay/Siliconix SUM90N06-5M5P-E3

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Vishay Siliconix

N-Channel 60-V (D-S) MOSFET

PRODUCT SUMMARY			
V _{(BR)DSS} (V)	$r_{DS(on)}(\Omega)$	I _D (A)	Q _g (Typ)
60	$0.0055 \text{ at V}_{GS} = 10 \text{ V}$	90 ^d	78.5

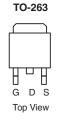
FEATURES

- TrenchFET[®] Power MOSFETS
- 175 °C Junction Temperature
- 100 % R_q and UIS Tested

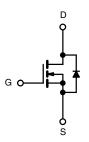


APPLICATIONS

- · Power Supply
 - Secondary Synchronous Rectification
- Industrial







N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS	S T _C = 25 °C, unless other	erwise noted			
Parameter	Symbol	Limit	Unit		
Drain-Source Voltage	V _{DS}	60	M		
Gate-Source Voltage		V _{GS} ± 20			
Continuous Drain Current (T _J = 175 °C)	T _C = 25 °C	I-	90 ^d	Α	
Communication Current (1) = 173 C)	T _C = 70 °C	- I _D	90 ^d		
Pulsed Drain Current		I _{DM}	240	A	
Avalanche Current		I _{AS}	50		
Single Avalanche Energy ^a	L = 0.1 mH	E _{AS}	125	mJ	
Maximum Power Dissipation ^a	T _C = 25 °C	В	272 ^b	W	
	T _A = 25 °C ^c	$ P_{D}$	3.75		
Operating Junction and Storage Temperature Range		T _J , T _{stg}	- 55 to 175	°C	

THERMAL RESISTANCE RATINGS				
Parameter	Symbol	Limit	Unit	
Junction-to-Ambient (PCB Mount) ^c	R _{thJA}	40	°C/W	
Junction-to-Case (Drain)	R _{thJC}	0.55		

Notes:

- a. Duty cycle \leq 1 %.
- b. See SOA curve for voltage derating.
- c. When Mounted on 1" square PCB (FR-4 material).
- d. Package limited.

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Datasheet of SUM90N06-5M5P-E3 - MOSFET N-CH 60V 90A D2PAK

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SUM90N06-5m5P

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Parameter	Symbol	Test Conditions	Min	Тур	Max	Unit
Static	•			•	L	
Drain-Source Breakdown Voltage	V _{(BR)DSS}	$V_{DS} = 0 \text{ V}, I_{D} = 250 \mu\text{A}$	60			V
Gate Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_D = 250 \mu A$	2.5		4.5	
Gate-Body Leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			± 250	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 60 V, V _{GS} = 0 V			1	μΑ
		V _{DS} = 60 V, V _{GS} = 0 V, T _J = 125 °C			50	
		$V_{DS} = 60 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 150 \text{ °C}$			250	
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \ge 10 \text{ V}, V_{GS} = 10 \text{ V}$	70			Α
Drain-Source On-State Resistance ^a	_	$V_{GS} = 10 \text{ V}, I_D = 20 \text{ A}$		0.0045	0.0055	Ω
	r _{DS(on)}	$V_{GS} = 10 \text{ V}, I_D = 20 \text{ A}, T_J = 125 ^{\circ}\text{C}$		0.0072	0.009	
Forward Transconductance ^a	9 _{fs}	$V_{DS} = 15 \text{ V}, I_{D} = 20 \text{ A}$		58		S
Dynamic ^b	<u>.</u>				<u> </u>	
Input Capacitance	C _{iss}			4700		pF
Output Capacitance	C _{oss}	V _{GS} = 0 V, V _{DS} = 30 V, f = 1 MHz		620		
Reverse Transfer Capacitance	C _{rss}			250		
Total Gate Charge ^c	Qg			78.5	120	nC
Gate-Source Charge ^c	Q _{gs}	$V_{DS} = 30 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 50 \text{ A}$		28		
Gate-Drain Charge ^c	Q _{gd}			20.6		
Gate Resistance	R_g	f = 1 MHz		1.2	2.4	Ω
Turn-On Delay Time ^c	t _{d(on)}			16	30	
Rise Time ^c	t _r	V_{DD} = 30 V, R_L = 0.6 Ω		10	20	ns
Turn-Off Delay Time ^c	t _{d(off)}	$I_D \cong 50 \text{ A}, V_{GEN} = 10 \text{ V}, R_g = 1 \Omega$		25	40	
Fall Time ^c	t _f			8	15	
Source-Drain Diode Ratings and Cha	racteristics T ₀	_C = 25 °C ^b		•		
Continuous Current	I _S				85	
Pulsed Current	I _{SM}				240	Α
Forward Voltage ^a	V _{SD}	I _F = 20 A, V _{GS} = 0 V		0.83	1.5	V
Reverse Recovery Time	t _{rr}			62	100	ns
Peak Reverse Recovery Current	I _{RM(REC)}	I _F = 75 A, di/dt = 100 A/μs		3.8	5.7	Α
Reverse Recovery Charge	Q _{rr}	·		118	180	nC

Notes:

- a. Pulse test; pulse width \leq 300 μ s, duty cycle \leq 2 %.
- b. Guaranteed by design, not subject to production testing.
- $\ \ \, \text{c. Independent of operating temperature.}$

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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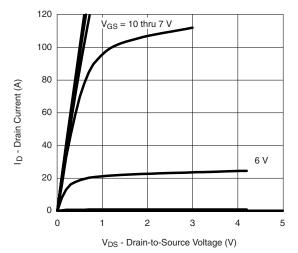
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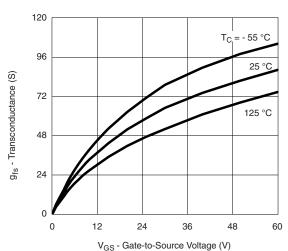


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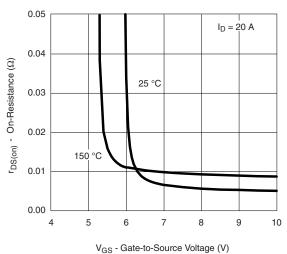
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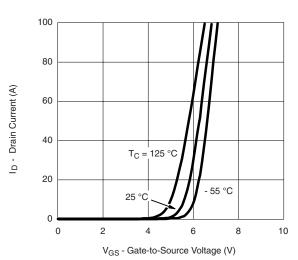




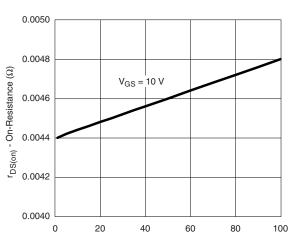
Transfer Characteristics



On-Resistance vs. Drain Current

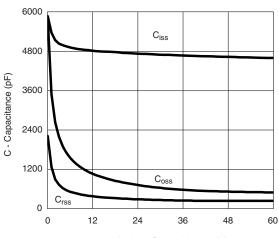


Transconductance



I_D - Drain Current (A)

On-resistance vs. Gate-to-Source Voltage



V_{DS} - Drain-to-Source Voltage (V)

Capacitance

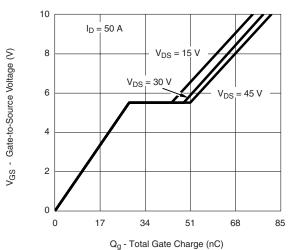
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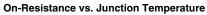


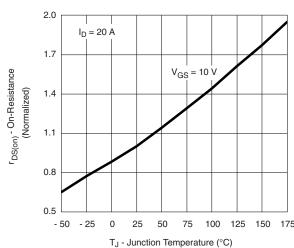
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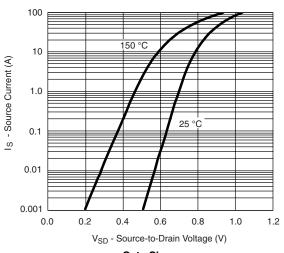




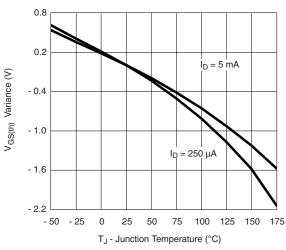




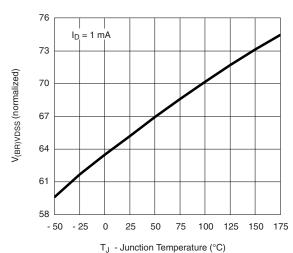
Threshold Voltage



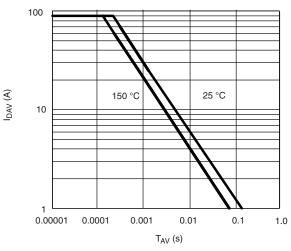
Gate Charge



On-Resistance vs. Junction Temperature



Source-Drain Diode Forward Voltage



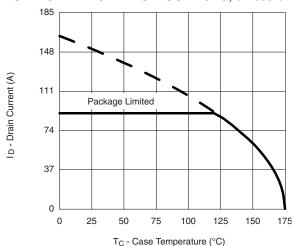
Maximum Drain Current vs. Case Temperature



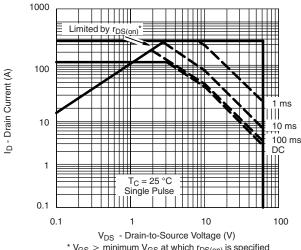


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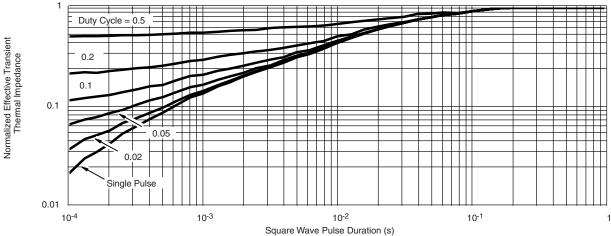
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Single Pulse Avalanche Current Capability vs. Time



* V_{GS} > minimum V_{GS} at which $r_{DS(on)}$ is specified Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see http://www.vishay.com/ppg?69537.

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Datasheet of SUM90N06-5M5P-E3 - MOSFET N-CH 60V 90A D2PAK

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