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**SUP90N15-18P**

Vishay Siliconix

## N-Channel 150-V (D-S) MOSFET

### PRODUCT SUMMARY

$V_{(BR)DSS}$ (V)	$r_{DS(on)}$ ( $\Omega$ )	$I_D$ (A)	$Q_g$ (Typ)
150	0.018 at $V_{GS} = 10$ V	90 <sup>d</sup>	64

### FEATURES

- TrenchFET® Power MOSFET
- 175 °C Junction Temperature
- 100 %  $R_g$  and UIS Tested

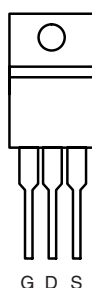


**RoHS**  
COMPLIANT

### APPLICATIONS

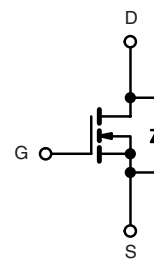
- Primary Side Switch
- Industrial

TO-220AB



Top View

Ordering Information: SUP90N15-18P-E3 (Lead (Pb)-free)



N-Channel MOSFET

### ABSOLUTE MAXIMUM RATINGS $T_C = 25$ °C, unless otherwise noted

ABSOLUTE MAXIMUM RATINGS T <sub>C</sub> = 25 °C, unless otherwise noted				
Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V <sub>DS</sub>	150	V
Gate-Source Voltage		V <sub>GS</sub>	± 20	
Continuous Drain Current (T <sub>J</sub> = 175 °C)	T <sub>C</sub> = 25 °C	I <sub>D</sub>	90 <sup>d</sup>	A
	T <sub>C</sub> = 70 °C		75	
Pulsed Drain Current		I <sub>DM</sub>	180	
Avalanche Current		I <sub>AS</sub>	50	
Single Avalanche Energy <sup>a</sup>	L = 0.1 mH	E <sub>AS</sub>	125	mJ
Maximum Power Dissipation <sup>a</sup>	T <sub>C</sub> = 25 °C	P <sub>D</sub>	375 <sup>b</sup>	W
	T <sub>A</sub> = 25 °C <sup>c</sup>		3.75	
Operating Junction and Storage Temperature Range		T <sub>J</sub> , T <sub>stg</sub>	- 55 to 175	°C

### THERMAL RESISTANCE RATINGS

Parameter	Symbol	Limit	Unit
Junction-to-Ambient (PCB Mount) <sup>c</sup>	$R_{thJA}$	40	°C/W
Junction-to-Case (Drain)	$R_{thJC}$	0.4	

Notes:

- Duty cycle  $\leq 1$  %.
- See SOA curve for voltage derating.
- When Mounted on 1" square PCB (FR-4 material).
- Package limited.

# SUP90N15-18P

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SPECIFICATIONS T <sub>J</sub> = 25 °C, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	V <sub>DS</sub> = 0 V, I <sub>D</sub> = 250 μA	150			V
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	2.5		4.5	
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ± 20 V			± 250	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 150 V, V <sub>GS</sub> = 0 V			1	μA
		V <sub>DS</sub> = 150 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 125 °C			50	
		V <sub>DS</sub> = 150 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 150 °C			250	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> ≥ 10 V, V <sub>GS</sub> = 10 V	120			A
Drain-Source On-State Resistance <sup>a</sup>	r <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 20 A		0.0145	0.018	Ω
		V <sub>GS</sub> = 10 V, I <sub>D</sub> = 20 A, T <sub>J</sub> = 125 °C		0.029	0.036	
Forward Transconductance <sup>a</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 20 A		55		S
Dynamic <sup>b</sup>						
Input Capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 75 V, f = 1 MHz		4180		pF
Output Capacitance	C <sub>oss</sub>			235		
Reverse Transfer Capacitance	C <sub>rss</sub>			83		
Total Gate Charge <sup>c</sup>	Q <sub>g</sub>	V <sub>DS</sub> = 75 V, V <sub>GS</sub> = 10 V, I <sub>D</sub> = 85 A		64	100	nC
Gate-Source Charge <sup>c</sup>	Q <sub>gs</sub>			23		
Gate-Drain Charge <sup>c</sup>	Q <sub>gd</sub>			16		
Gate Resistance	R <sub>g</sub>	f = 1 MHz		2.1	4.2	Ω
Turn-On Delay Time <sup>c</sup>	t <sub>d(on)</sub>	V <sub>DD</sub> = 75 V, R <sub>L</sub> = 0.88 Ω I <sub>D</sub> ≅ 85 A, V <sub>GEN</sub> = 10 V, R <sub>g</sub> = 1 Ω		15	25	ns
Rise Time <sup>c</sup>	t <sub>r</sub>			10	15	
Turn-Off Delay Time <sup>c</sup>	t <sub>d(off)</sub>			25	40	
Fall Time <sup>c</sup>	t <sub>f</sub>			8	15	
Source-Drain Diode Ratings and Characteristics T <sub>C</sub> = 25 °C <sup>b</sup>						
Continuous Current	I <sub>S</sub>				90	A
Pulsed Current	I <sub>SM</sub>				180	
Forward Voltage <sup>a</sup>	V <sub>SD</sub>	I <sub>F</sub> = 30 A, V <sub>GS</sub> = 0 V		1.0	1.5	V
Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = 50 A, di/dt = 100 A/μs		130	200	ns
Peak Reverse Recovery Current	I <sub>RM(REC)</sub>			8	12	A
Reverse Recovery Charge	Q <sub>rr</sub>			0.52	1.2	μC

Notes:

- a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .
- b. Guaranteed by design, not subject to production testing.
- c. Independent of operating temperature.

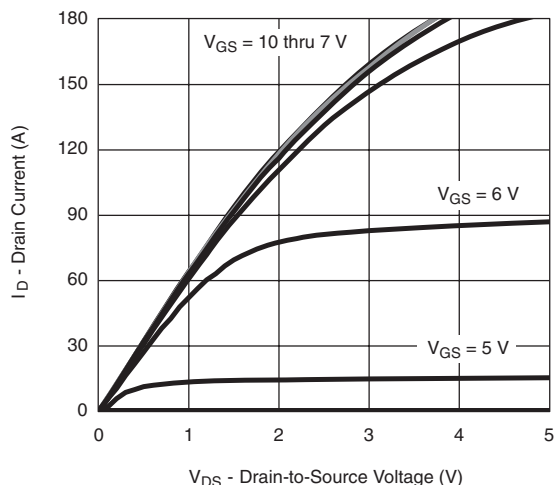
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



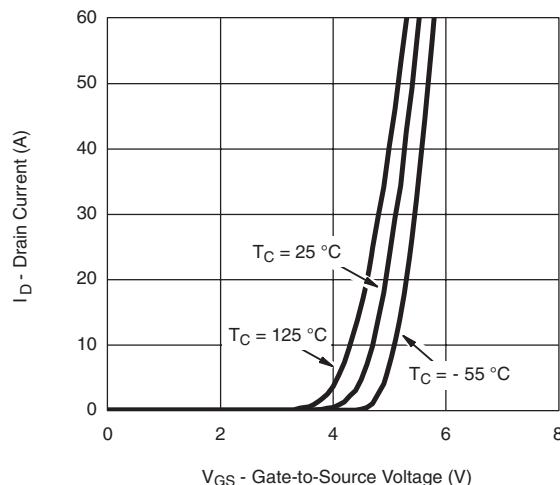
# SUP90N15-18P

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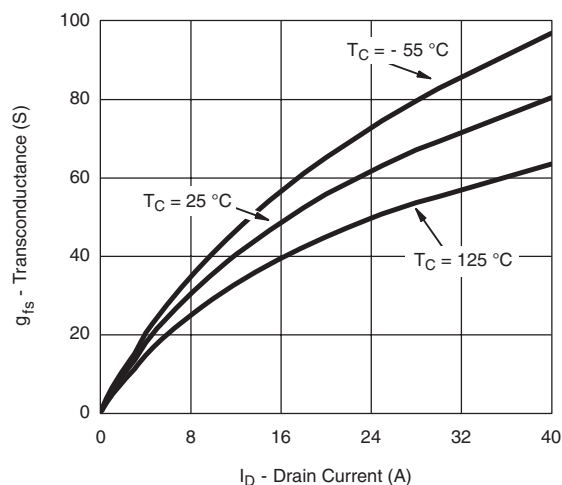
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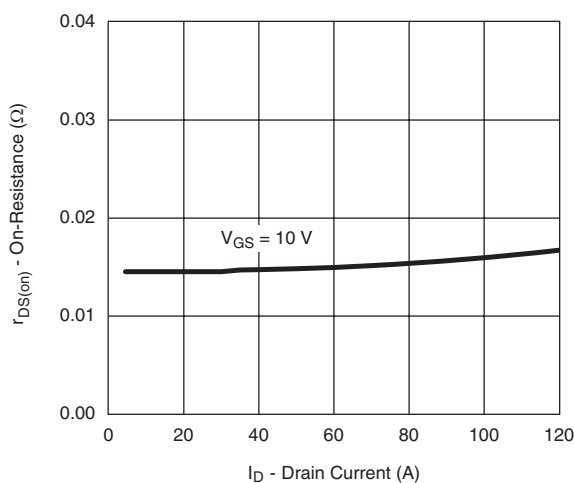
**Output Characteristics**



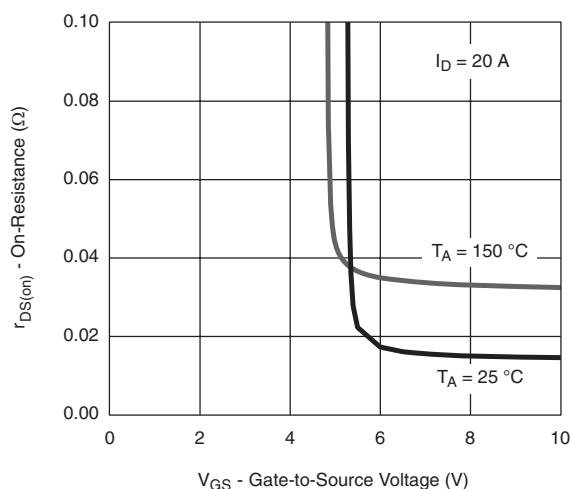
**Transfer Characteristics**



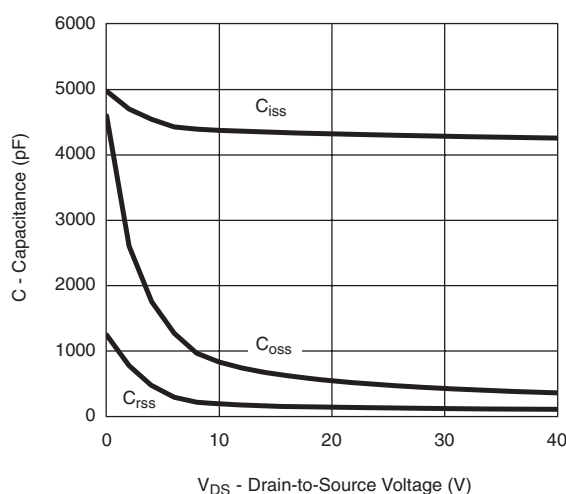
**Transconductance**



**On-Resistance vs. Drain Current**



**On-Resistance vs. Gate-to-Source Voltage**



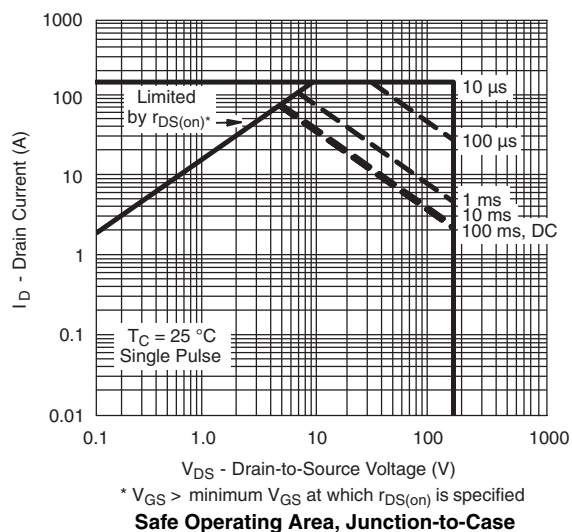
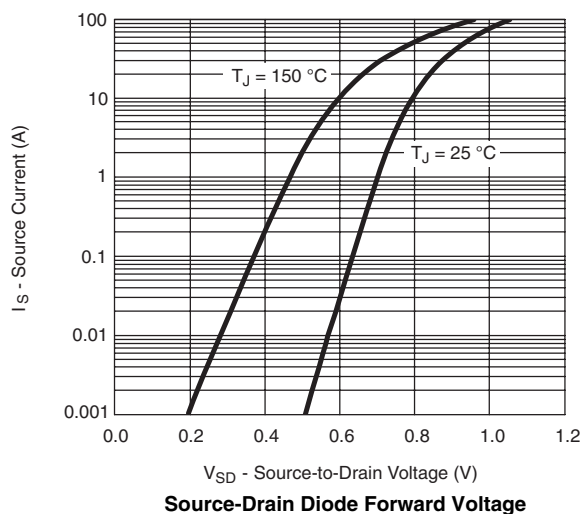
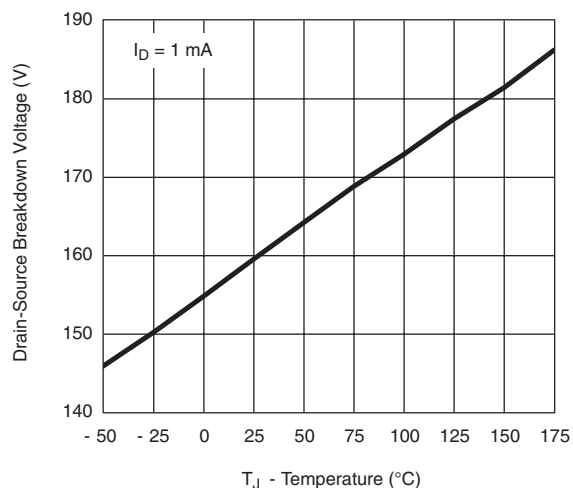
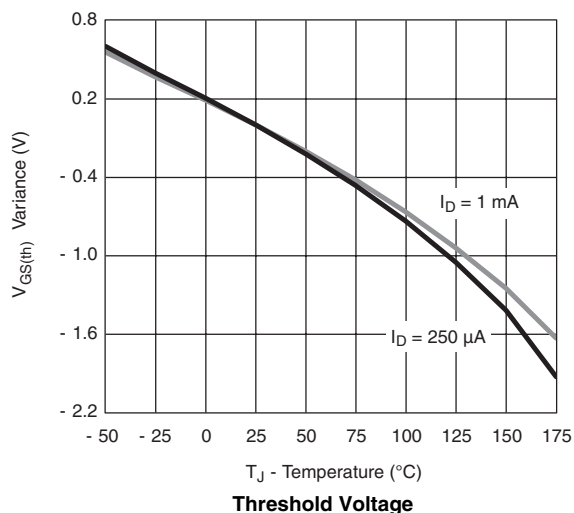
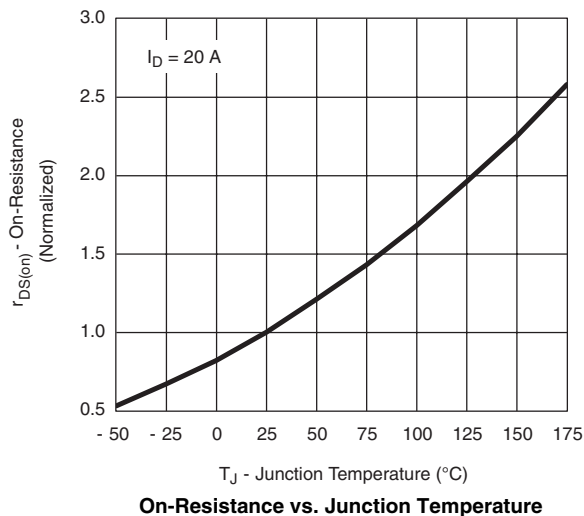
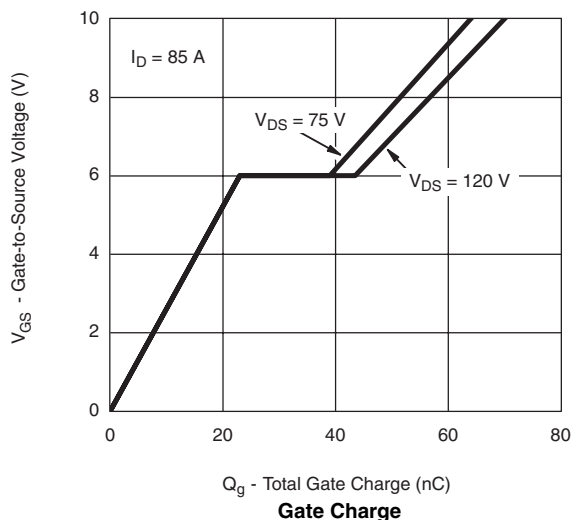
**Capacitance**

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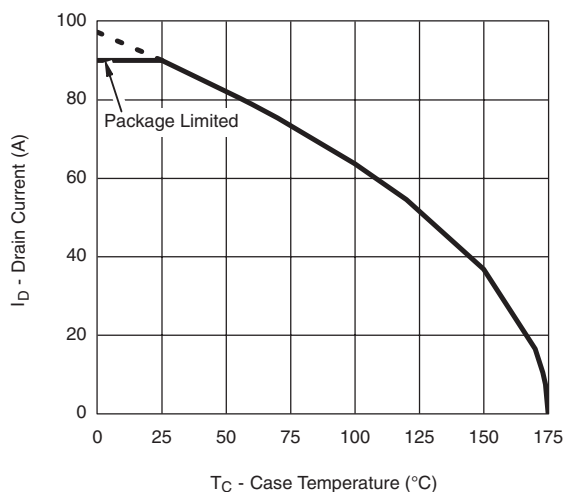




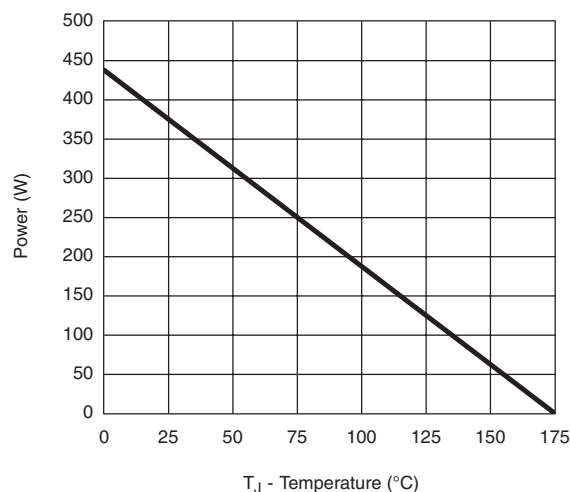
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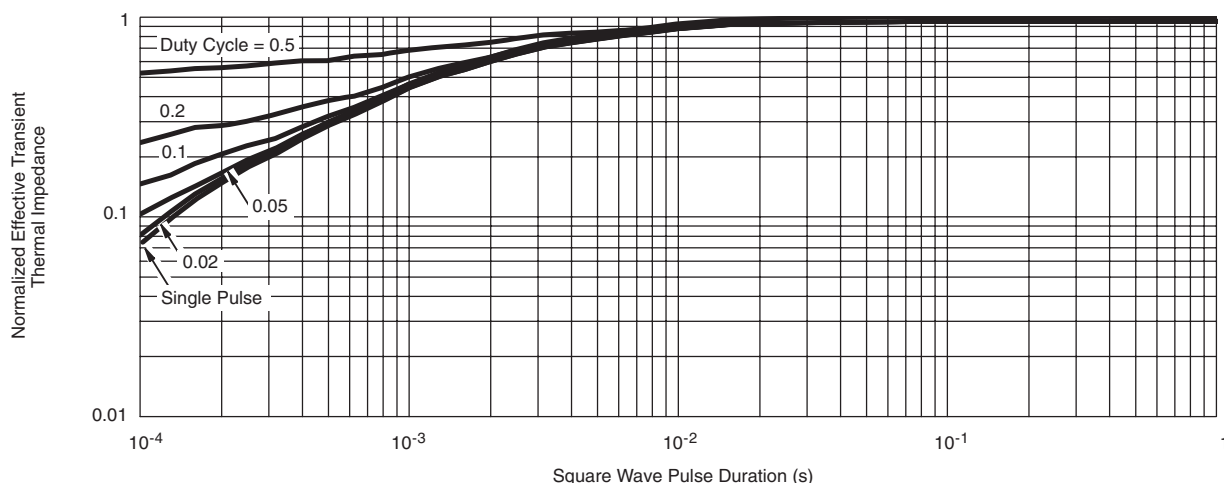
## TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



**Current Derating\*, Junction-to-Case**



**Power Derating\*, Junction-to-Case**



**Normalized Thermal Transient Impedance, Junction-to-Case**

\* The power dissipation  $P_D$  is based on  $T_{J(max)} = 150\text{ °C}$ , using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

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