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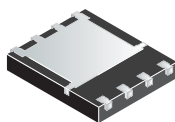
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[Texas Instruments](#)

[CSD17506Q5A](#)

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CSD17506Q5A

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SLPS304B – DECEMBER 2010 – REVISED JUNE 2012

30V, N-Channel NexFET™ Power MOSFETs

Check for Samples: [CSD17506Q5A](#)

FEATURES

- Ultralow Q_g and Q_{gd}
- Low Thermal Resistance
- Avalanche Rated
- Pb Free Terminal Plating
- RoHS Compliant
- Halogen Free
- SON 5-mm × 6-mm Plastic Package

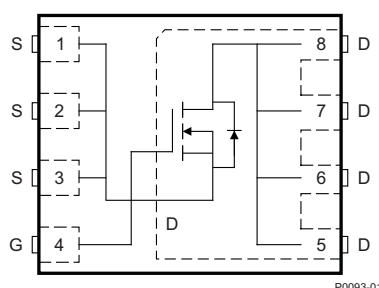
APPLICATIONS

- Point-of-Load Synchronous Buck in Networking, Telecom, and Computing Systems
- Synchronous or Control FET Applications

DESCRIPTION

The NexFET™ power MOSFET has been designed to minimize losses in power conversion applications.

Top View



P0093-01

PRODUCT SUMMARY

$T_A = 25^\circ\text{C}$ unless otherwise stated		TYPICAL VALUE	UNIT
V_{DS}	Drain to Source Voltage	30	V
Q_g	Gate Charge Total (4.5V)	8.3	nC
Q_{gd}	Gate Charge Gate to Drain	2.3	nC
$R_{DS(on)}$	Drain to Source On Resistance	$V_{GS} = 4.5\text{V}$	4.2 mΩ
		$V_{GS} = 10\text{V}$	3.2 mΩ
$V_{GS(th)}$	Threshold Voltage	1.3	V

ORDERING INFORMATION

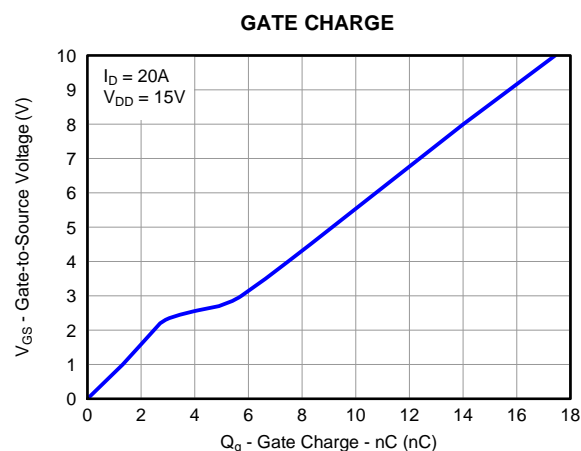
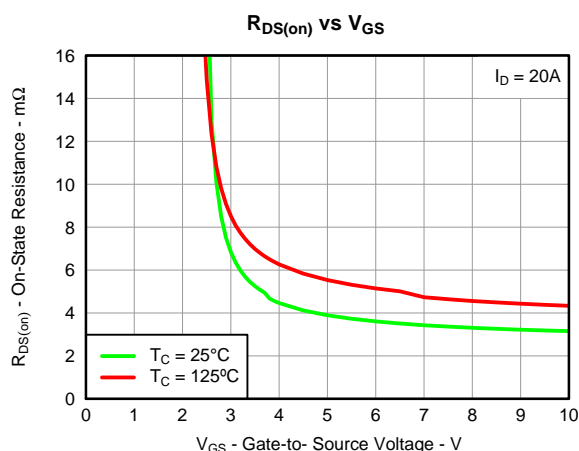
Device	Package	Media	Qty	Ship
CSD17506Q5A	SON 5-mm × 6-mm Plastic Package	13-Inch Reel	2500	Tape and Reel

ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$ unless otherwise stated		VALUE	UNIT
V_{DS}	Drain to Source Voltage	30	V
V_{GS}	Gate to Source Voltage	±20	V
I_D	Continuous Drain Current, $T_C = 25^\circ\text{C}$	100	A
	Continuous Drain Current ⁽¹⁾	23	A
I_{DM}	Pulsed Drain Current, $T_A = 25^\circ\text{C}$ ⁽²⁾	150	A
P_D	Power Dissipation ⁽¹⁾	3.2	W
T_J, T_{STG}	Operating Junction and Storage Temperature Range	–55 to 150	°C
E_{AS}	Avalanche Energy, single pulse $I_D = 72\text{A}$, $L = 0.1\text{mH}$, $R_G = 25\Omega$	259	mJ

(1) Typical $R_{\theta JA} = 39^\circ\text{C/W}$ on a 1-inch² (6.45-cm²), 2-oz. (0.071-mm thick) Cu pad on a 0.06-inch (1.52-mm) thick FR4 PCB.

(2) Pulse duration ≤300μs, duty cycle ≤2%



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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ELECTRICAL CHARACTERISTICS

(T_A = 25°C unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Static Characteristics						
BV _{DSS}	Drain to Source Voltage	V _{GS} = 0V, I _{DS} = 250μA	30			V
I _{DSS}	Drain to Source Leakage Current	V _{GS} = 0V, V _{DS} = 24V			1	μA
I _{GSS}	Gate to Source Leakage Current	V _{DS} = 0V, V _{GS} = 20V			100	nA
V _{GS(th)}	Gate to Source Threshold Voltage	V _{DS} = V _{GS} , I _{DS} = 250μA	1	1.3	1.8	V
R _{DS(on)}	Drain to Source On Resistance	V _{GS} = 4.5V, I _{DS} = 20A		4.2	5.3	mΩ
		V _{GS} = 10V, I _{DS} = 20A		3.2	4	mΩ
g _{fs}	Transconductance	V _{DS} = 15V, I _{DS} = 20A		76		S
Dynamic Characteristics						
C _{iss}	Input Capacitance	V _{GS} = 0V, V _{DS} = 15V, f = 1MHz		1270	1650	pF
C _{oss}	Output Capacitance			860	1120	pF
C _{rss}	Reverse Transfer Capacitance			50	65	pF
R _G	Series Gate Resistance			1.1	2.2	Ω
Q _g	Gate Charge Total (4.5V)	V _{DS} = 15V, I _{DS} = 20A		8.3	11	nC
Q _{gd}	Gate Charge Gate to Drain			2.3		nC
Q _{gs}	Gate Charge Gate to Source			3.1		nC
Q _{g(th)}	Gate Charge at V _{th}			1.6		nC
Q _{oss}	Output Charge	V _{DS} = 14V, V _{GS} = 0V		23		nC
t _{d(on)}	Turn On Delay Time	V _{DS} = 15V, V _{GS} = 4.5V, I _{DS} = 20A, R _G = 2Ω		7.5		ns
t _r	Rise Time			13		ns
t _{d(off)}	Turn Off Delay Time			13		ns
t _f	Fall Time			5.3		ns
Diode Characteristics						
V _{SD}	Diode Forward Voltage	I _{SD} = 20A, V _{GS} = 0V		0.8	1	V
Q _{rr}	Reverse Recovery Charge	V _{DD} = 14V, I _F = 20A, di/dt = 300A/μs		33		nC
t _{rr}	Reverse Recovery Time			27		ns

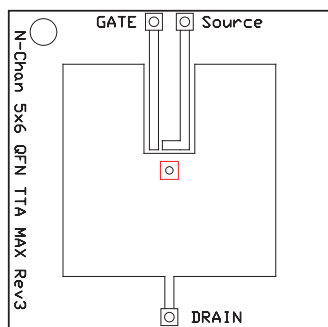
THERMAL CHARACTERISTICS

(T_A = 25°C unless otherwise stated)

PARAMETER	MIN	TYP	MAX	UNIT
R _{θJC} Thermal Resistance Junction to Case ⁽¹⁾			1	°C/W
R _{θJA} Thermal Resistance Junction to Ambient ⁽¹⁾⁽²⁾			50	°C/W

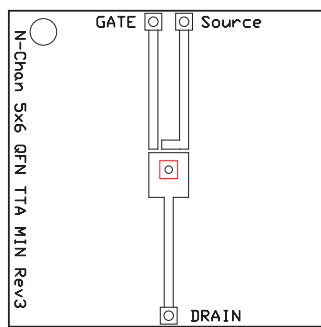
(1) R_{θJC} is determined with the device mounted on a 1-inch² (6.45-cm²), 2-oz. (0.071-mm thick) Cu pad on a 1.5-inch × 1.5-inch (3.81-cm × 3.81-cm), 0.06-inch (1.52-mm) thick FR4 PCB. R_{θJC} is specified by design, whereas R_{θJA} is determined by the user's board design.

(2) Device mounted on FR4 material with 1-inch² (6.45-cm²), 2-oz. (0.071-mm thick) Cu.



M0137-01

Max $R_{\theta JA} = 50^{\circ}\text{C/W}$
when mounted on
1 inch² (6.45 cm²) of 2-
oz. (0.071-mm thick)
Cu.



M0137-02

Max $R_{\theta JA} = 120^{\circ}\text{C/W}$
when mounted on a
minimum pad area of
2-oz. (0.071-mm thick)
Cu.

TYPICAL MOSFET CHARACTERISTICS

($T_A = 25^{\circ}\text{C}$ unless otherwise stated)

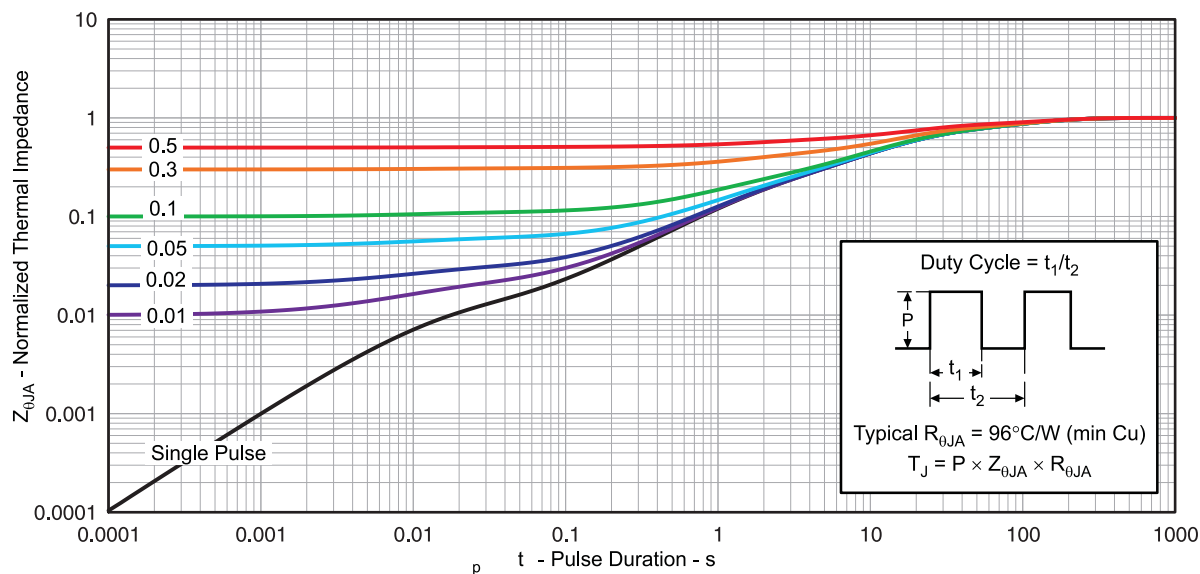


Figure 1. Transient Thermal Impedance

CSD17506Q5A



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TYPICAL MOSFET CHARACTERISTICS (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)

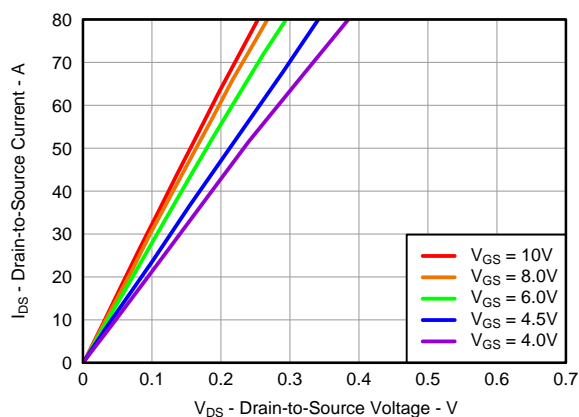


Figure 2. Saturation Characteristics

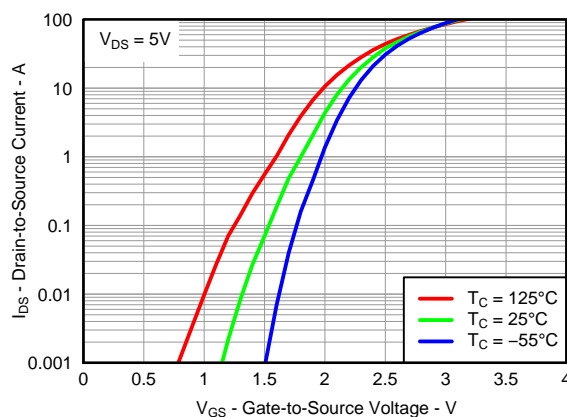


Figure 3. Transfer Characteristics

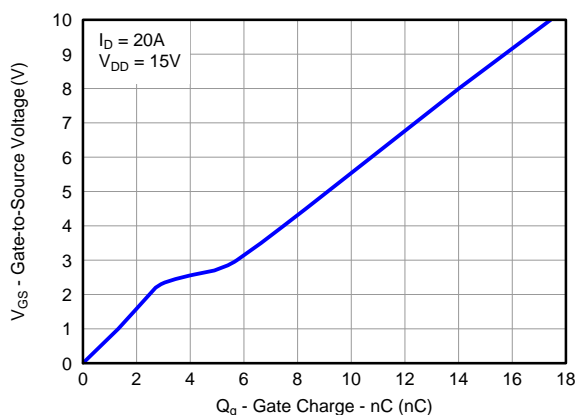


Figure 4. Gate Charge

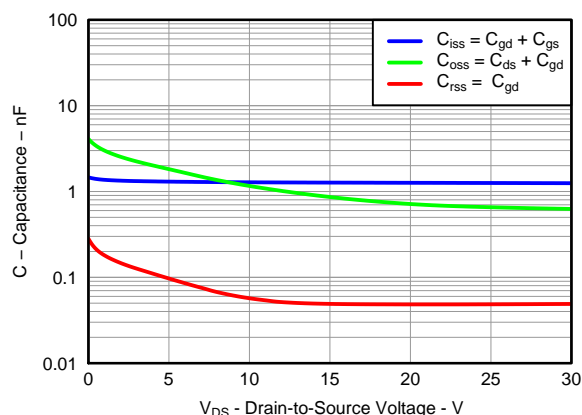


Figure 5. Capacitance

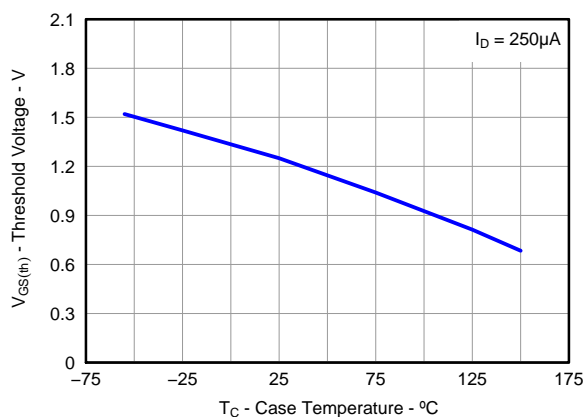


Figure 6. Threshold Voltage vs. Temperature

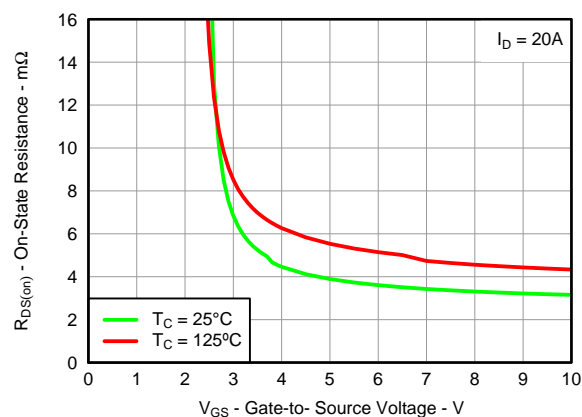


Figure 7. On-State Resistance vs. Gate-to-Source Voltage

TYPICAL MOSFET CHARACTERISTICS (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)

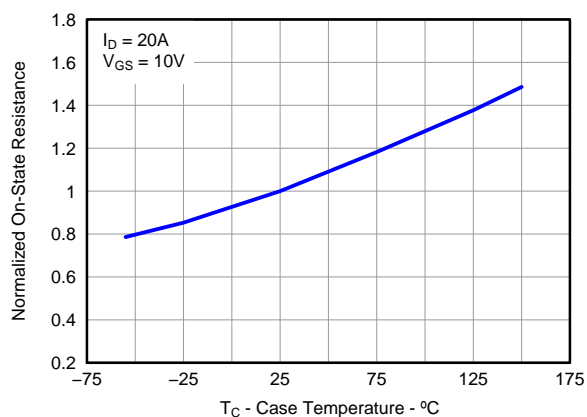


Figure 8. Normalized On-State Resistance vs. Temperature

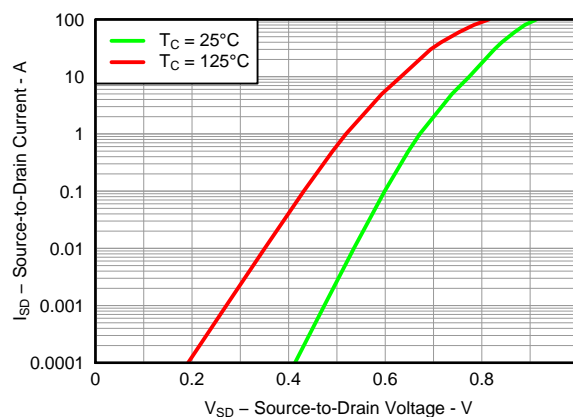


Figure 9. Typical Diode Forward Voltage

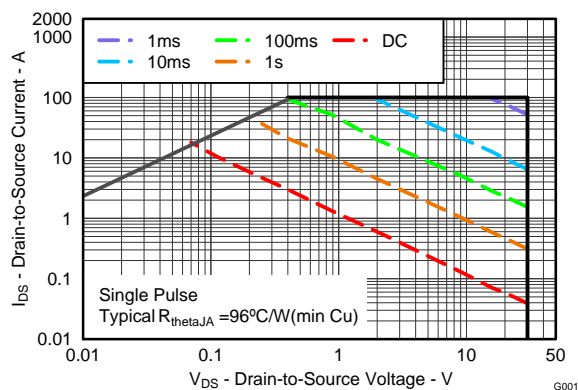


Figure 10. Maximum Safe Operating Area

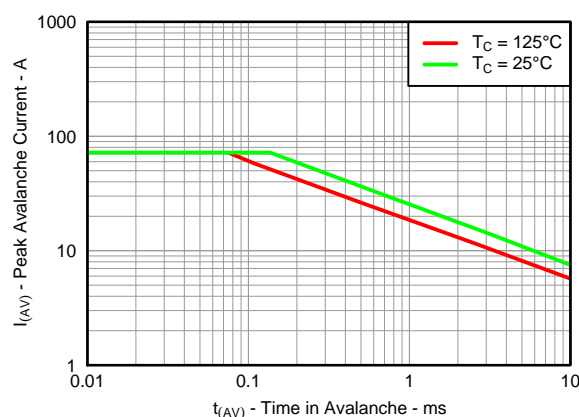


Figure 11. Single Pulse Unclamped Inductive Switching

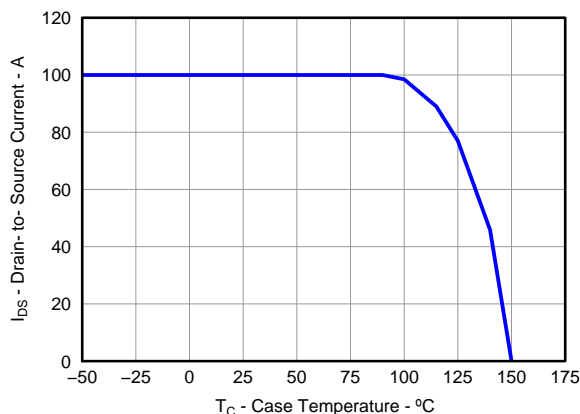


Figure 12. Maximum Drain Current vs. Temperature

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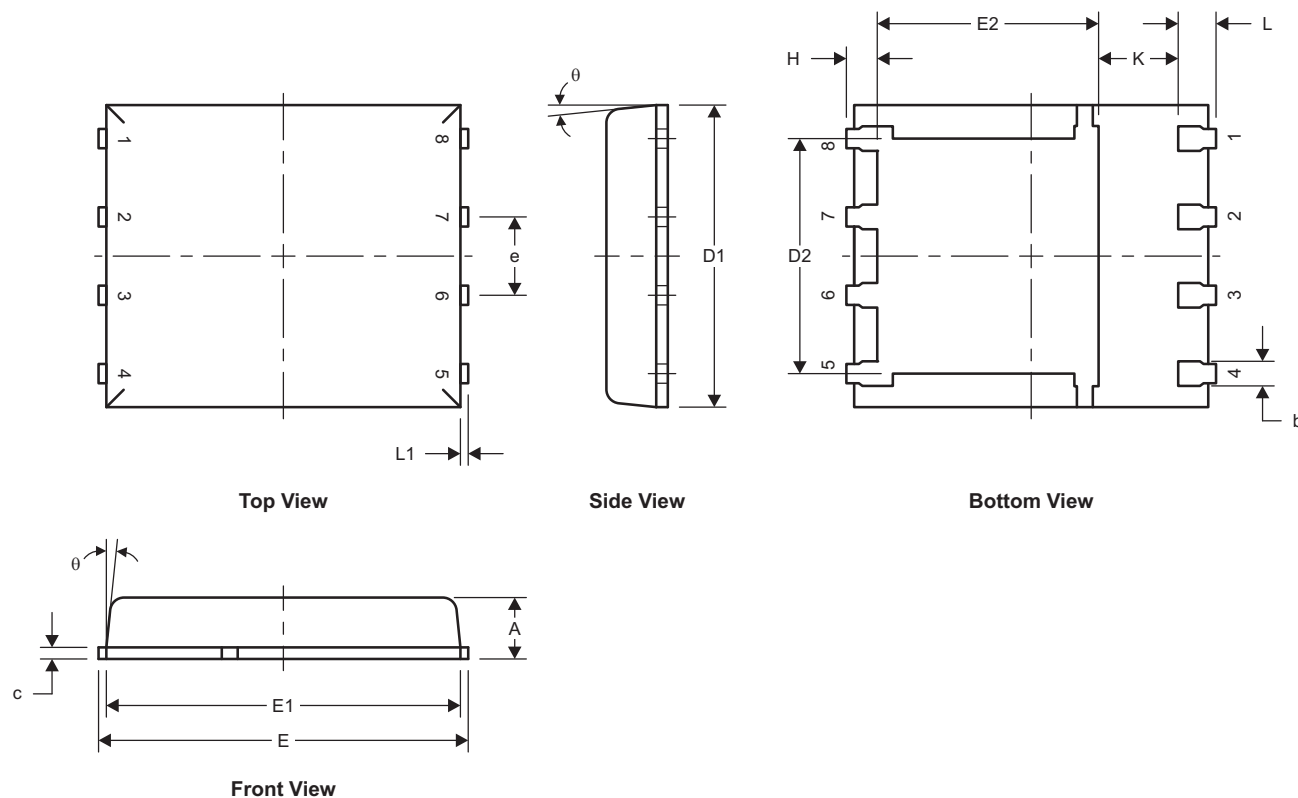


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MECHANICAL DATA

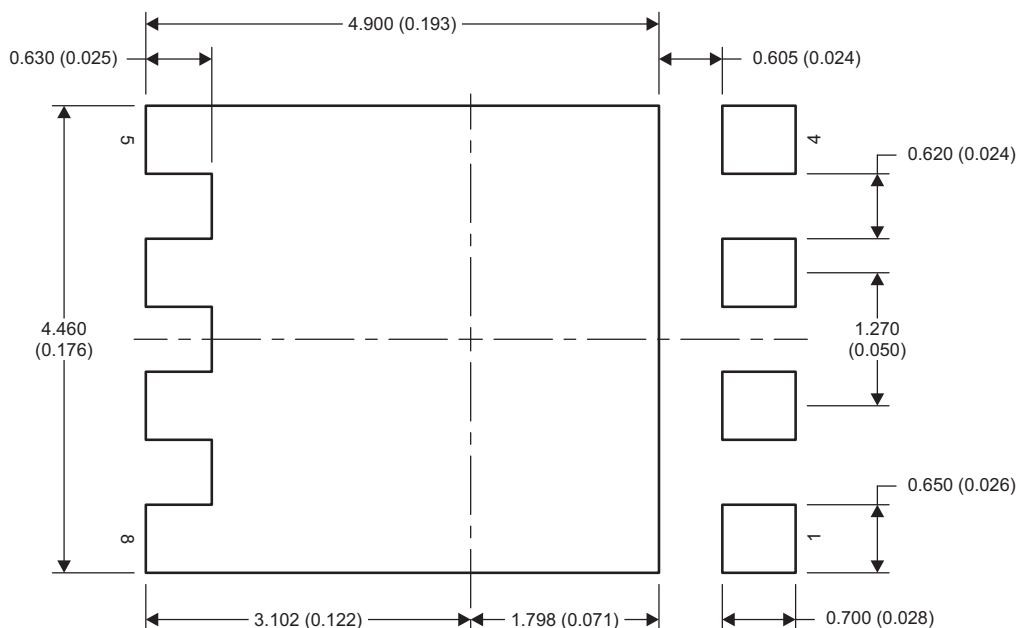
Q5A Package Dimensions



M0135-01

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.90	1.00	1.10
b	0.33	0.41	0.51
c	0.20	0.25	0.34
D1	4.80	4.90	5.00
D2	3.61	3.81	4.02
E	5.90	6.00	6.10
E1	5.70	5.75	5.80
E2	3.38	3.58	3.78
e	1.17	1.27	1.37
H	0.41	0.56	0.71
K	1.10		
L	0.51	0.61	0.71
L1	0.06	0.13	0.20
θ	0°		12°

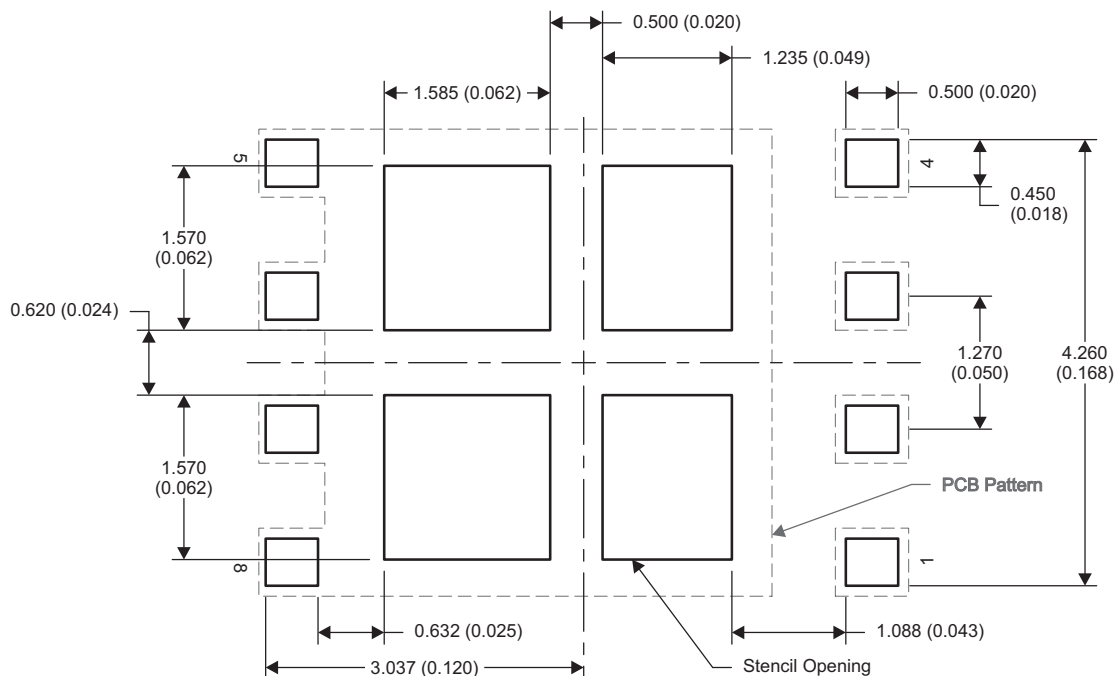
Recommended PCB Pattern



M0139-01

NOTE: Dimensions are in mm (inches).

Stencil Recommendation



M0209-01

NOTE: Dimensions are in mm (inches).

For recommended circuit layout for PCB designs, see application note [SLPA005](#) – *Reducing Ringing Through PCB Layout Techniques*.

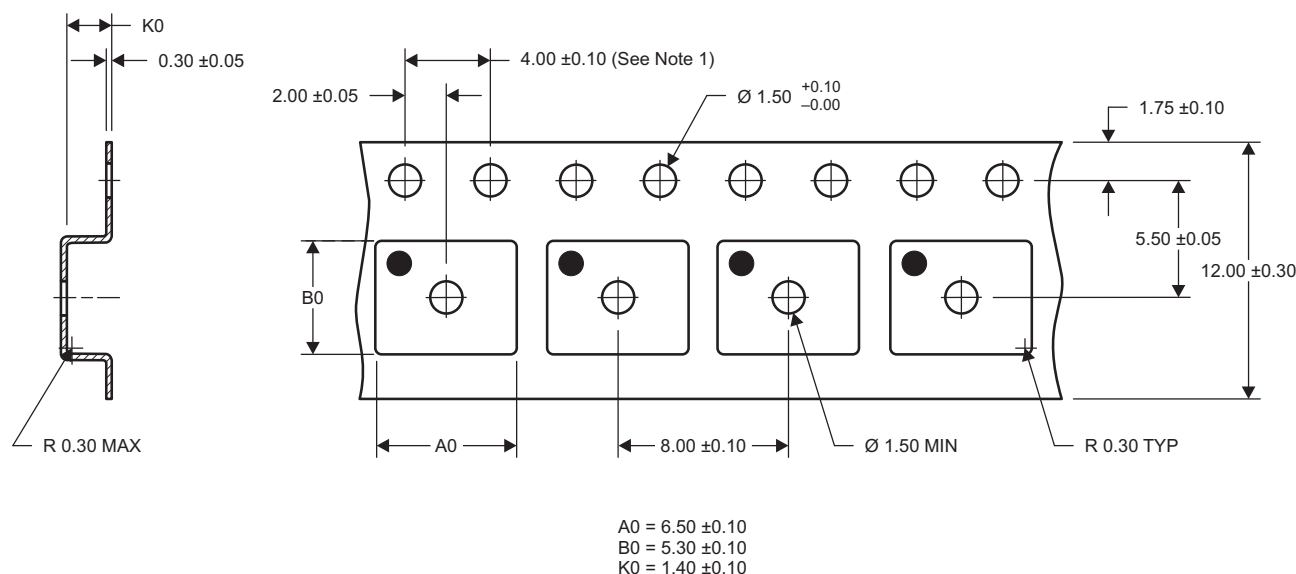
CSD17506Q5A



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Q5A Tape and Reel Information



M0138-01

- NOTES: 1. 10-sprocket hole-pitch cumulative tolerance ± 0.2
2. Camber not to exceed 1mm in 100mm, noncumulative over 250mm
3. Material: black static-dissipative polystyrene
4. All dimensions are in mm (unless otherwise specified)
5. A0 and B0 measured on a plane 0.3mm above the bottom of the pocket

REVISION HISTORY

Changes from Original (December 2010) to Revision A	Page
• Changed V_{GS} in the Abs Max Ratings table From: +20/-12V To: $\pm 20V$	1
• Changed from +20/-12V to 20V	2
Changes from Revision A (July 2011) to Revision B	Page
• Changed Figure 10, Maximum Safe Operating Area	5



PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD17506Q5A	ACTIVE	VSONP	DQJ	8	2500	Pb-Free (RoHS Exempt)	CU SN	Level-1-260C-UNLIM	-55 to 150	CSD17506	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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PACKAGE OPTION ADDENDUM

7-Jan-2016

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