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Data sheet acquired from Harris Semiconductor
 SCHS048C – Revised October 2003

CMOS Liquid-Crystal Display Drivers

High-Voltage Types (20-Volt Rating)

CD4054B – 4-Segment Display Driver

CD4055B – BCD to 7-Segment Decoder/Driver with “Display-Frequency” Output

CD4056B – BCD to 7-Segment Decoder/Driver with Strobed-Latch Function

■ **CD4055B** and **CD4056B** types are single-digit BCD-to-7-segment decoder/driver circuits that provide level-shifting functions on the chip. This feature permits the BCD input-signal swings (V_{DD} to V_{SS}) to be the same as or different from the 7-segment output-signal swings (V_{DD} to V_{EE}). For example, the BCD input-signal swings (V_{DD} to V_{SS}) may be as small as 0 to -3 V, whereas the output-display drive-signal swing (V_{DD} to V_{EE}) may be as large as from 0 to -15 V. If V_{DD} to V_{EE} exceeds 15 V, V_{DD} to V_{SS} should be at least 4 V (0 to -4 V).

The 7-segment outputs are controlled by the DISPLAY-FREQUENCY (DF) input which causes the selected segment outputs to be low, high, or a square-wave output (for liquid-crystal displays). When the DF input is low the output segments will be high when selected by the BCD inputs. When the DF input is high, the output segments will be low when selected by the BCD inputs. When a square-wave is present at the DF input, the selected segments will have a square-wave output that is 180° out of phase with the DF input. Those segments which are not selected will have a square-wave output that is in phase with the input. DF square-wave repetition rates for liquid-crystal displays usually range from 30 Hz (well above flicker rate) to 200 Hz (well below the upper limit of the liquid-crystal frequency response). The **CD4055B** provides a level-shifted high-amplitude DF output which is required for driving the common electrode in liquid-crystal displays. The **CD4056B** provides a strobed-latch function at the BCD inputs. Decoding of all input combinations on the **CD4055B** and **CD4056B** provides displays of 0 to 9 as well as L, P, H, A, –, and a blank position.

The **CD4054B** provides level shifting similar to the **CD4055B** and **CD4056B** independently strobed latches, and common DF control on 4 signal lines. The **CD4054B** is intended to provide drive-signal compatibility with the **CD4055B** and **CD4056B** 7-segment decoder types for the decimal point, colon, polarity, and similar display lines. A level-shifted high-amplitude DF output can be obtained from any **CD4054B** output line by connect-

CD4054B, CD4055B, CD4056B Types

Features:

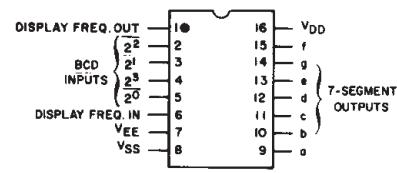
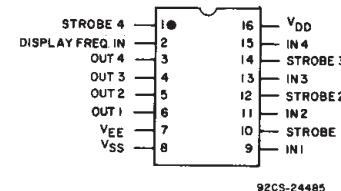
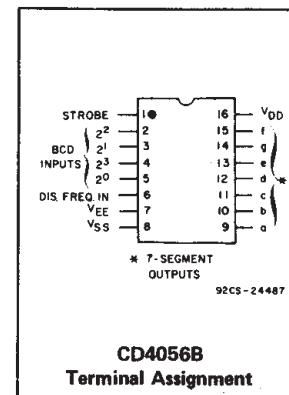
- Operation of liquid crystals with CMOS circuits provides ultra-low-power displays
- Equivalent ac output drive for liquid-crystal displays – no external capacitor required
- Voltage doubling across display, e.g. $V_{DD} - V_{EE} = 18$ V results in effective 36 V p-p drive across selected display segments
- Low- or high-output level dc drive for other types of displays
- On-chip logic-level conversion for different input- and output-level swings
- Full decoding of all input combinations: 0-9, L, H, P, A, –, and blank positions
- Strobed-latch function—**CD4054B** Series and **CD4056B** Series
- DISPLAY-FREQUENCY (DF) output for liquid-crystal common-line drive signal—**CD4055B** Series (**CD4054B** Series also: see introductory text)
- 100% tested for quiescent current at 20 V
- Maximum input current of 1 μ A at 18 V over full package temperature range; 100 nA at 18 V and 25°C
- Noise margin (over full package temperature range):
 1 V at $V_{DD} = 5$ V
 2 V at $V_{DD} = 10$ V
 2.5 V at $V_{DD} = 15$ V
- 5-V, 10-V, and 15-V parametric ratings

Applications

- General-purpose displays
- Calculators and meters
- Wall and table clocks
- Industrial control panels
- Portable lab instruments
- Panel meters
- Auto dashboard displays
- Appliance control panels

ing the corresponding input and strobe lines to a low and high level, respectively and applying a square wave to DF_{IN}. The **CD4054B** may also be utilized for logic-level “up conversion” or “down conversion”. For example, input-signal swings (V_{DD} to V_{SS}) from +5 to 0 V can be converted to output-signal swings (V_{DD} to V_{EE}) of +5 to -5 V. The level-shifted function on all three types permits the use of different input- and output-signal swings. The input swings from a low level of V_{SS} to a high level of V_{DD} while the output swings from a low level of V_{EE} to the same high level of V_{DD} . Thus, the input and output swings can be selected independently of each other over a 3-to-18 V range. V_{SS} may be connected to V_{EE} when no level-shift function is required.

For the **CD4054B** and **CD4056B**, data are



transferred from input to output by placing a high voltage level at the strobe input. A low voltage level at the strobe input latches the data input and the corresponding output segments remain selected (or non-selected) while the strobe is low.

Whenever the level-shifting function is required, the **CD4055B** can be used by itself to drive a liquid-crystal display (Fig.16 and Fig.20). The **CD4056B**, however, must be used together with a **CD4054B** to provide the common DF output (Fig.19). The capability of extending the voltage swing on the negative end (this voltage cannot be extended on the positive end) can be used to advantage in the setup of Fig.18. Fig.17 is common to all three types.

The **CD4054B**, **CD4055B**, and **CD4056B**-series types are supplied in 16-lead dual-in-line plastic packages (E suffix), 16-lead small-outline packages (M, M96, MT, and NSR suffixes), and 16-lead thin shrink small-outline packages (PW and PWR suffixes). The **CD4054B**- and **CD4056B**-series types also are supplied in 16-lead hermetic dual-in-line ceramic packages (F3A suffix).

CD4054B, CD4055B, CD4056B Types

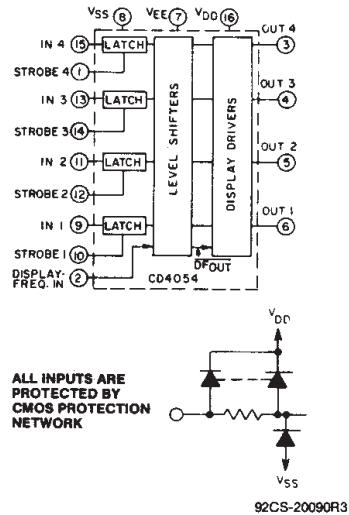


Fig.1 – CD4054B functional diagram.

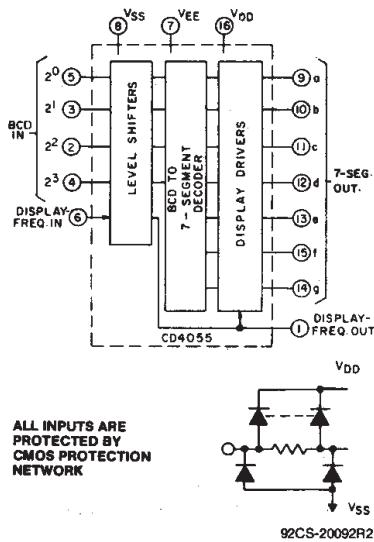


Fig.2 – CD4055B functional diagram.

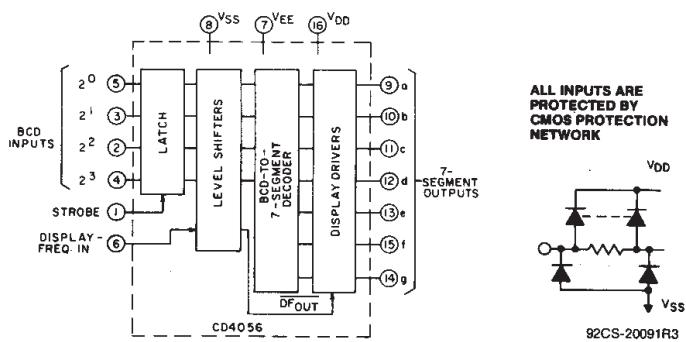


Fig.3 – CD4056B functional diagram.

CD4054B TRUTH TABLE

DF	IN	ST	OUT
0	0	1	0
1	0	1	1
0	1	1	1
1	1	1	0
X	X	0	*

X = Don't Care.

*Depends upon the input mode previously applied when ST = 1.

TRUTH TABLE FOR CD4055B and CD4056B

INPUT CODE	OUTPUT STATE							DISPLAY CHARACTER
	a	b	c	d	e	f	g	
2 ³ 2 ² 2 ¹ 2 ⁰	1	1	1	1	1	1	0	1
0 0 0 0	0	1	1	0	0	0	0	1
0 0 0 1	1	1	0	1	1	0	1	1
0 0 1 0	1	1	1	1	0	0	1	1
0 0 1 1	1	1	1	1	1	0	1	1
0 1 0 0	0	1	1	0	0	1	1	1
0 1 0 1	1	0	1	1	0	1	1	1
0 1 1 0	1	0	1	1	1	1	1	1
0 1 1 1	1	1	1	0	0	0	0	1
1 0 0 0	1	1	1	1	1	1	1	1
1 0 0 1	1	1	1	1	1	0	1	1
1 0 1 0	0	0	0	1	1	1	0	1
1 0 1 1	0	1	1	0	1	1	1	1
1 1 0 0	1	1	0	0	1	1	1	1
1 1 0 1	1	1	1	0	1	1	1	1
1 1 1 0	0	0	0	0	0	0	1	—
1 1 1 1	0	0	0	0	0	0	0	BLANK

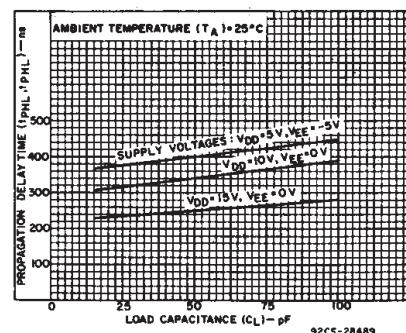


Fig.4 – Typical propagation delay time vs. load capacitance for CD4054B.

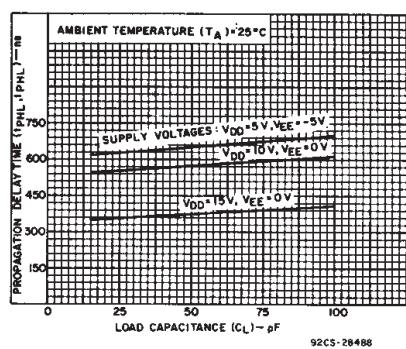


Fig.5 – Typical propagation delay time vs. load capacitance for CD4055 and CD4056B.

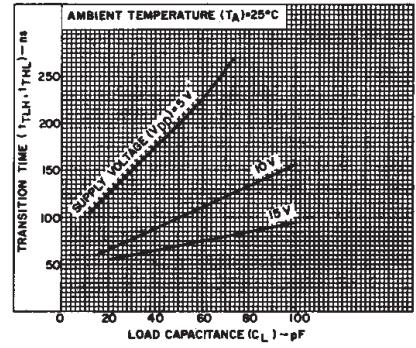


Fig.6 – Typical transition time vs. load capacitance.

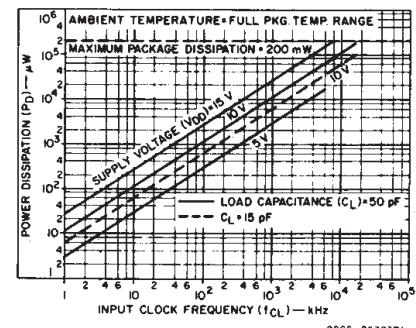


Fig.7 – Typical input clock frequency vs. power dissipation.

CD4054B, CD4055B, CD4056B Types

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V_{DD})

Voltages referenced to V_{SS} Terminal) -0.5V to +20V

INPUT VOLTAGE RANGE, ALL INPUTS

-0.5V to V_{DD} +0.5V

DC INPUT CURRENT, ANY ONE INPUT

±10mA

POWER DISSIPATION PER PACKAGE (P_D):

For $T_A = -55^\circ C$ to $+100^\circ C$ 500mW

For $T_A = +100^\circ C$ to $+125^\circ C$ Derate Linearity at 12mW/ $^\circ C$ to 200mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR $T_A =$ FULL PACKAGE-TEMPERATURE RANGE (All Package Types) 100mW

OPERATING-TEMPERATURE RANGE (T_A)

-55 $^\circ C$ to +125 $^\circ C$

STORAGE TEMPERATURE RANGE (T_{STG})

-65 $^\circ C$ to +150 $^\circ C$

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 \pm 1/32 inch (1.59 \pm 0.79mm) from case for 10s max +265 $^\circ C$

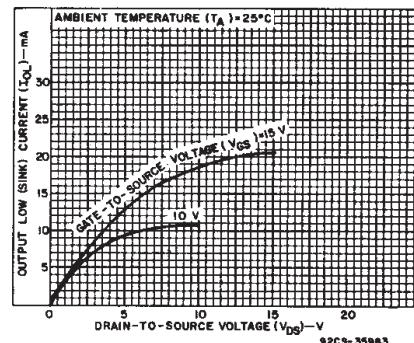


Fig.8 – Typical n-channel output low (sink) current characteristics.

STATIC ELECTRICAL CHARACTERISTICS

Characteristic	CONDITIONS					LIMITS AT INDICATED TEMPERATURES (°C)						Units
	V_{EE} (V)	V_{SS} (V)	V_O (V)	V_{IN} (V)	V_{DD} (V)	-55 $^\circ C$	-40 $^\circ C$	+85 $^\circ C$	+125 $^\circ C$	+25 $^\circ C$		
Quiescent Device Current, I_{DD} MAX.	-5	0		5		5	150	150	-	0.04	5	μA
	0	0		10		10	300	300	-	0.04	10	
	0	0		15		20	600	600	-	0.04	20	
	0	0		20		100	3000	3000	-	0.08	100	
Output Voltage:	0	0	0.5	5		0.05				-	0	0.05
	0	0	0.10	10		0.05				-	0	0.05
	0	0	0.15	15		0.05				-	0	0.05
	0	0	0.5	5		4.95				-	4.95	
	0	0	0.10	10		9.95				-	9.95	
	0	0	0.15	15		14.95				-	14.95	
	0	0	0.5	5						-	14.95	
	0	0	0.10	10						-	14.95	
Input Low Voltage, V_{IL} MAX.	0	0	0.5	4.5		5	1.5			-	-	1.5
	0	0	1.9			10	3			-	-	3
	0	0	1.5,13.5			15	4			-	-	4
	-5	0	0.5,4.5			5	3.5			-	-	
Input High Voltage, V_{IH} MIN.	0	0	1.9			10	7			-	-	
	0	0	1.5,13.5			15	11			-	-	
	-5	0	4.5			5	-0.6	-0.55	-0.35	0.3	-0.45	-0.9
	0	0	9.5			10	-0.6	-0.55	-0.35	-0.3	-0.45	-0.9
Output Low (Sink) Current, I_{OL}	-5	0	-4.5			5	0.98	0.92	0.67	0.55	0.8	1.6
	0	0	0.5			10	0.98	0.92	0.67	0.55	0.8	1.6
	0	0	1.5			15	3.6	3.4	2.4	2	2.9	5.8
	-5	0	4.5			5	-0.6	-0.55	-0.35	0.3	-0.45	-0.9
Output High (Source) Current, I_{OH}	-5	0	9.5			10	-0.6	-0.55	-0.35	-0.3	-0.45	-0.9
	0	0	13.5			15	-1.9	-1.8	-1.2	-1.1	-1.5	-3
	0	0	-	0.18	18	± 0.1	± 0.1	± 1	± 1	-	$\pm 10^{-5}$	± 0.1
	0	0	-	0.18	18	± 0.1	± 0.1	± 1	± 1	-	$\pm 10^{-5}$	± 0.1
Input Current, I_{IN}	0	0	-	0.18	18	± 0.1	± 0.1	± 1	± 1	-	$\pm 10^{-5}$	± 0.1
	0	0	-	0.18	18	± 0.1	± 0.1	± 1	± 1	-	$\pm 10^{-5}$	± 0.1
	0	0	-	0.18	18	± 0.1	± 0.1	± 1	± 1	-	$\pm 10^{-5}$	± 0.1
	0	0	-	0.18	18	± 0.1	± 0.1	± 1	± 1	-	$\pm 10^{-5}$	± 0.1

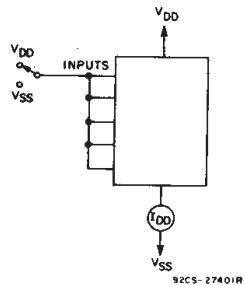


Fig. 11 – Quiescent-device-current test circuit.

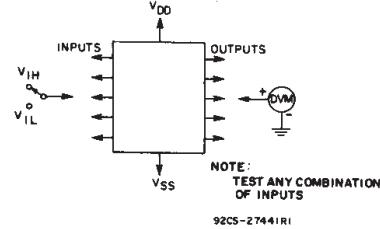


Fig. 12 – Input-voltage test circuit.

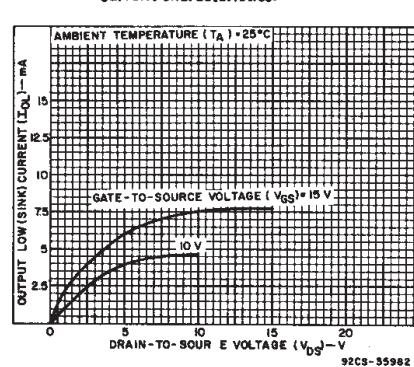


Fig. 9 – Minimum n-channel output low (sink) current characteristics.

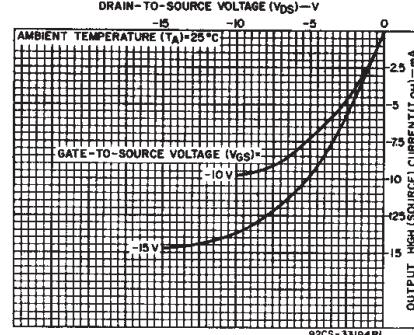


Fig. 10 – Typical p-channel output high (source) current characteristics.

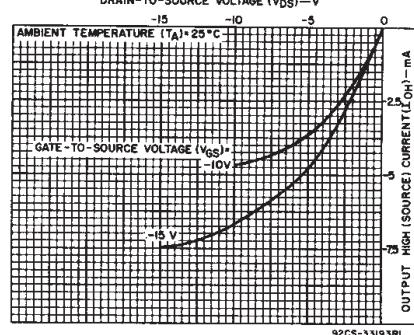


Fig. 13 – Minimum p-channel output high (source) current characteristics.

CD4054B, CD4055B, CD4056B Types

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25^\circ\text{C}$, $C_L = 50 \text{ pF}$, Input $t_f, t_r = 20 \text{ ns}$, $R_L = 200 \text{ k}\Omega$

CHARACTERISTIC	CONDITIONS			LIMITS				UNITS	
				ALL PACKAGE TYPES					
	V_{EE} (V)	V_{SS} (V)	V_{DD} (V)	CD4054	CD4055, CD4056	Typ.	Max.		
Propagation Delay Time, t_{PHL}, t_{PLH} (Any Input to Any Output)	-5	0	5	400	800	650	1300	ns	
	0	0	10	340	680	575	1150		
	0	0	15	250	500	375	750		
Transition Time, t_{THL}, t_{TLH} (Any Output)	-5	0	5	100	200	100	200	ns	
	0	0	10	100	200	100	200		
	0	0	15	75	150	75	150		
Minimum Data Setup Time, t_S^*	-5	0	5	110	220	110	220	ns	
	0	0	10	50	100	50	100		
			15	35	70	35	70		
Minimum Strobe Pulse Width, t_W^*	-5	0	5	110	220	110	220	ns	
	0	0	10	50	100	50	100		
	0	0	15	35	70	35	70		
Input Capacitance, C_{IN} (Any Input)	-	-	-	5	7.5	5	7.5	pF	

* CD4054 and CD4056 only.

RECOMMENDED OPERATING CONDITIONS at $T_A = 25^\circ\text{C}$ (Unless otherwise specified)

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

CHARACTERISTIC	V_{EE} (V)	V_{SS} (V)	V_{DD} (V)	LIMITS		UNITS
				Min.	Max.	
Supply Voltage Range: (At $T_A =$ Full Package Temperature Range)				3	18	V
Setup Time (t_S^*)	-5	0	5	220	—	ns
	0	0	10	100	—	
	0	0	15	70	—	
Strobe Pulse Width (t_W^*)	-5	0	5	220	—	ns
	0	0	10	100	—	
	0	0	15	70	—	

* For CD4054 and CD4056 only.

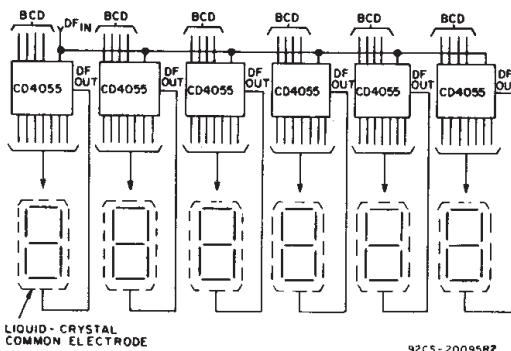


Fig. 16 – Clock display: $V_{DD} = 0 \text{ V}$, $V_{SS} = -5 \text{ V}$, $V_{EE} = -15 \text{ V}$, $DF_{IN} = 30 \text{ Hz}$ square wave.

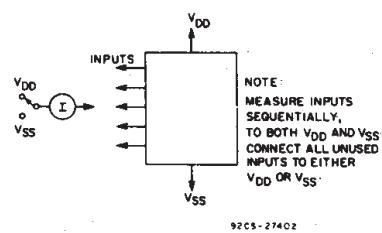


Fig. 14 – Input-current test circuit.

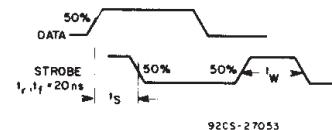


Fig. 15 – Data setup time and strobe pulse duration.

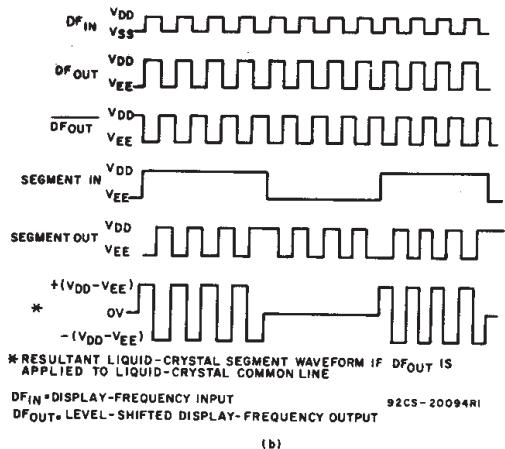
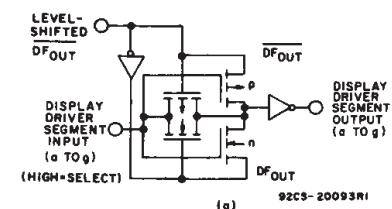


Fig. 17 – Display-driver circuit for one segment line and waveforms.

CD4054B, CD4055B, CD4056B Types

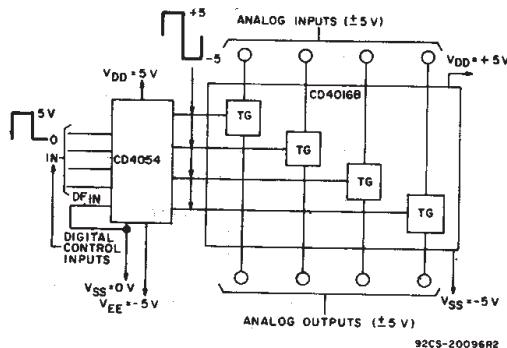


Fig.18 – Digital (0 to +5 V) to bidirectional analog control (+5 to -5 V) level shifter.

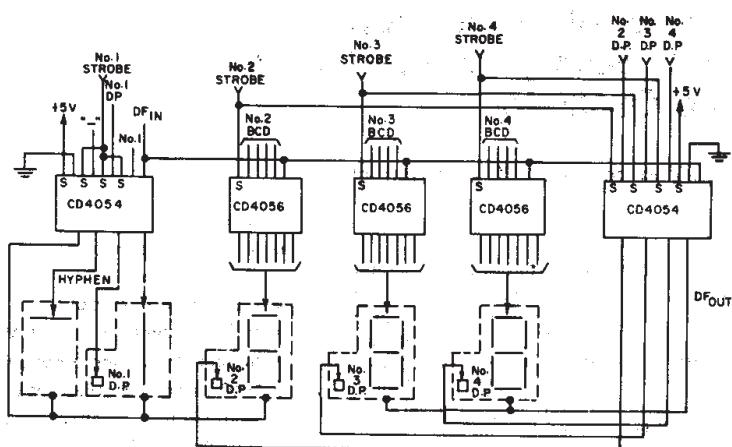


Fig.19 – Typical 3½-digit liquid-crystal display:
V_{DD} = +5 V, V_{SS} = 0 V, V_{EE} = -10 V,
DFIN = 30 Hz square wave.

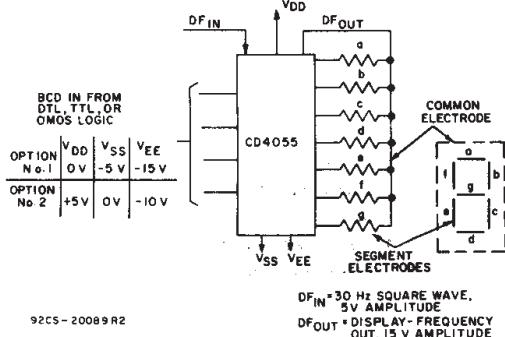


Fig.20 – Single-digit liquid-crystal display.

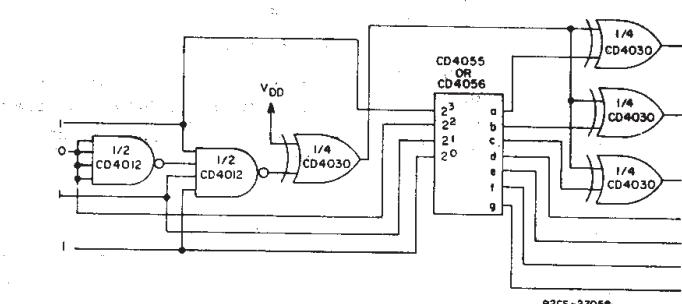


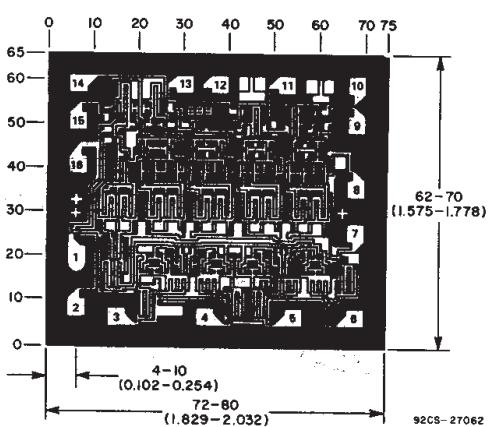
Fig.21 – Conversion of "H" display to "F" display.

In addition to the letters L, H, P, and A (See the truth table), five other letters can be displayed through the use of simple logic circuits preceding and following the CD4055B or CD4056B devices. Fig.21 is an example of a circuit that converts an "H" display (code 1011) to an "F" display. One condition that must be met is that VEE=VSS. If VEE≠VSS, the CD4054B must be used to level shift in the appropriate places.

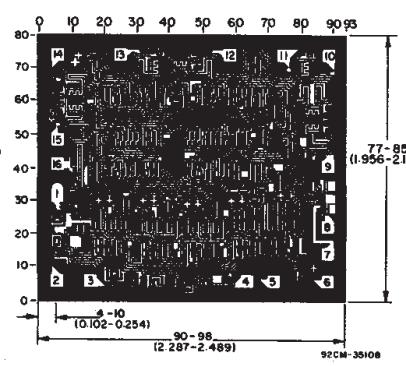
In a similar manner the letters C, E, J, and U can be displayed. These circuits can also be used to drive LED displays provided the exclusive-OR gates have sufficient output-current drive.

The letters B, D, G, I, O, and S may be represented by the codes for numbers 8, 0, 6, 1, 0, and 5, respectively, when there is pre-knowledge that only letters are to be displayed.

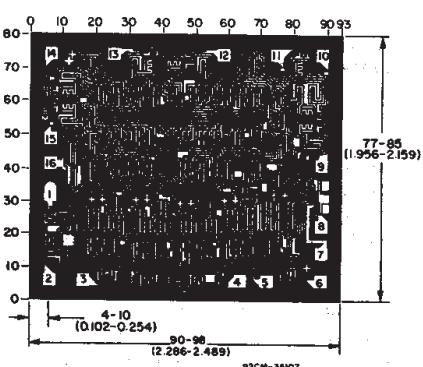
Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid gradations are in mils (10⁻³ inch).



Dimensions and pad layout for CD4054BH.



Dimensions and pad layout for CD4055BH



Dimensions and pad layout for CD4056BH

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD4054BE	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD4054BE	Samples
CD4054BF3A	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	CD4054BF3A	Samples
CD4054BM	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4054BM	Samples
CD4054BM96	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4054BM	Samples
CD4054BPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM054B	Samples
CD4055BE	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD4055BE	Samples
CD4055BEE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD4055BE	Samples
CD4055BM	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4055BM	Samples
CD4055BPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM055B	Samples
CD4056BE	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD4056BE	Samples
CD4056BEE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD4056BE	Samples
CD4056BF3A	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	CD4056BF3A	Samples
CD4056BM	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4056BM	Samples
CD4056BM96	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4056BM	Samples
CD4056BM96E4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4056BM	Samples
CD4056BM96G4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4056BM	Samples
CD4056BME4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4056BM	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD4056BMG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4056BM	Samples
CD4056BMT	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4056BM	Samples
CD4056BPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM056B	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF CD4054B, CD4054B-MIL, CD4056B, CD4056B-MIL :

• Catalog: [CD4054B](#), [CD4056B](#)

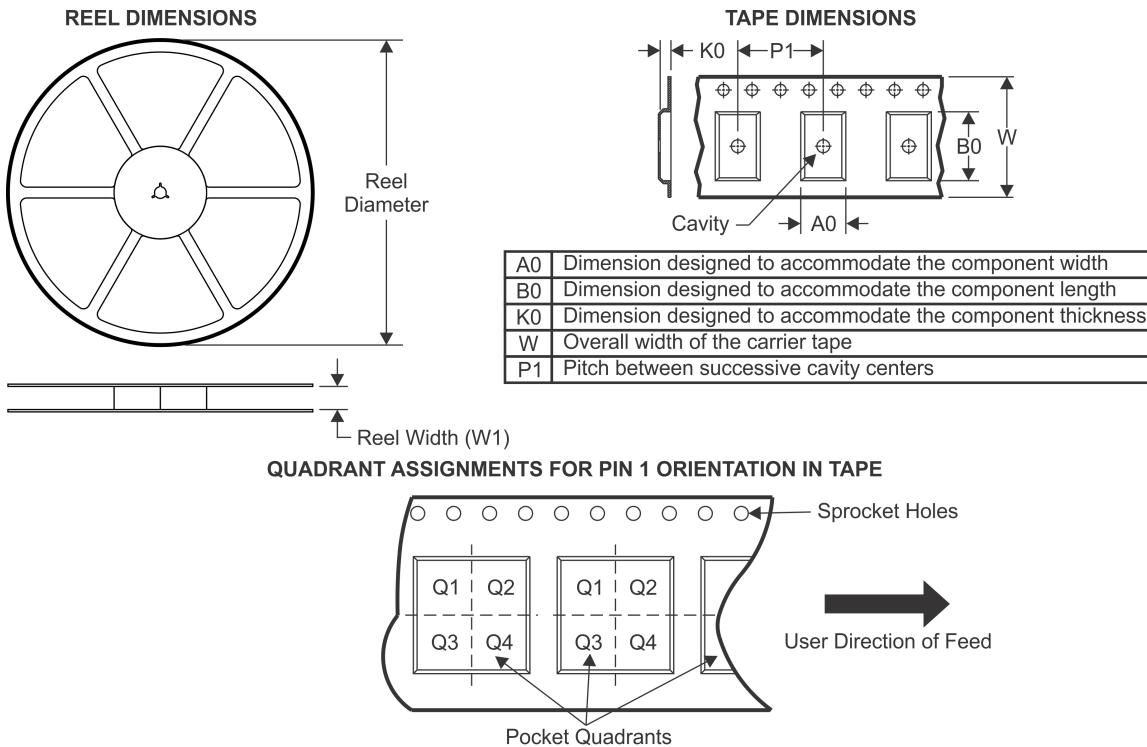
• Military: [CD4054B-MIL](#), [CD4056B-MIL](#)

NOTE: Qualified Version Definitions:

• Catalog - TI's standard catalog product

• Military - QML certified for Military and Defense Applications

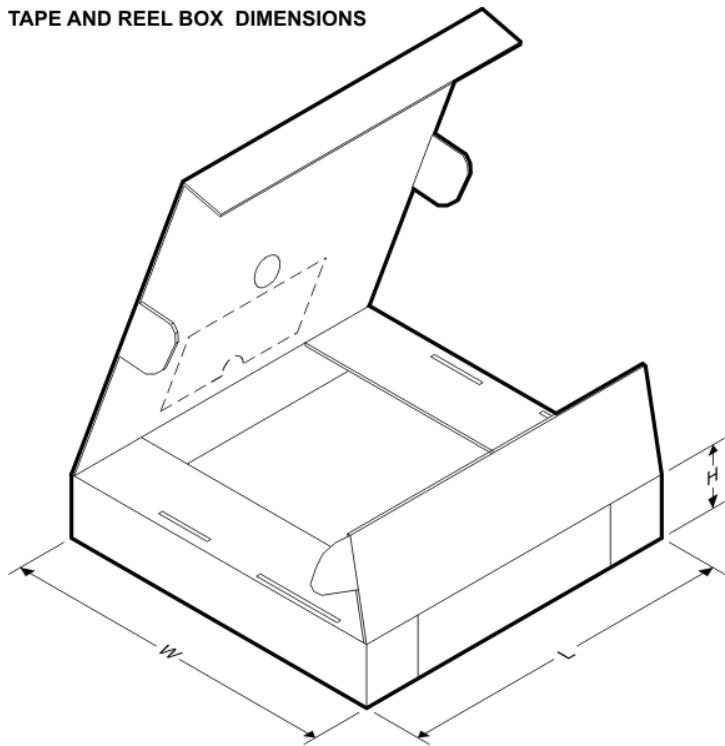
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD4054BM96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD4056BM96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



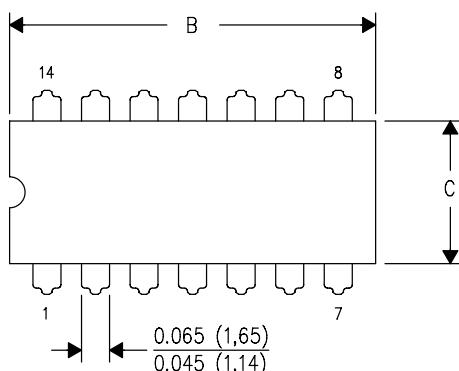
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD4054BM96	SOIC	D	16	2500	333.2	345.9	28.6
CD4056BM96	SOIC	D	16	2500	333.2	345.9	28.6

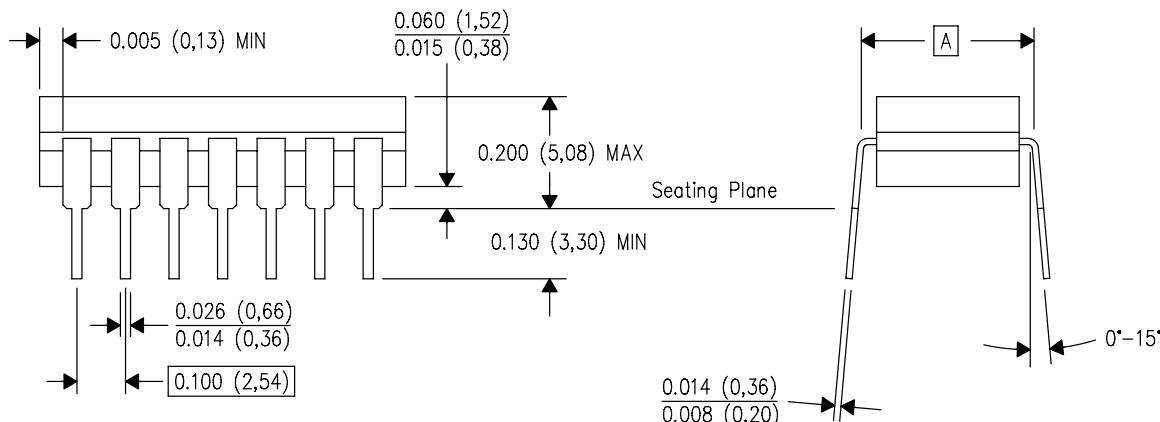
J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM	PINS **	14	16	18	20
		A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX		0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN		—	—	—	—
C MAX		0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN		0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

NOTES:

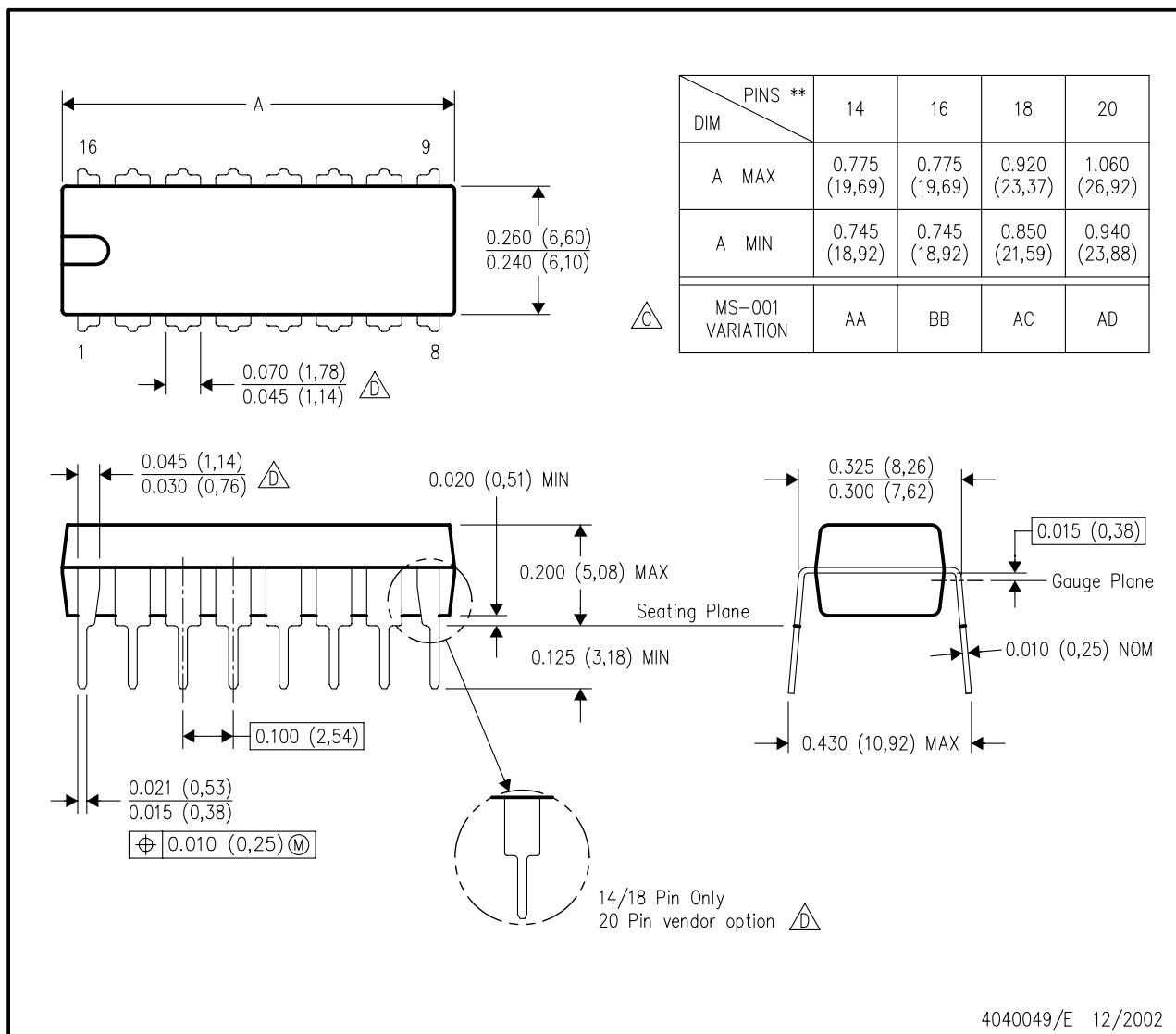
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

MECHANICAL DATA

N (R-PDIP-T**)

16 PINS SHOWN

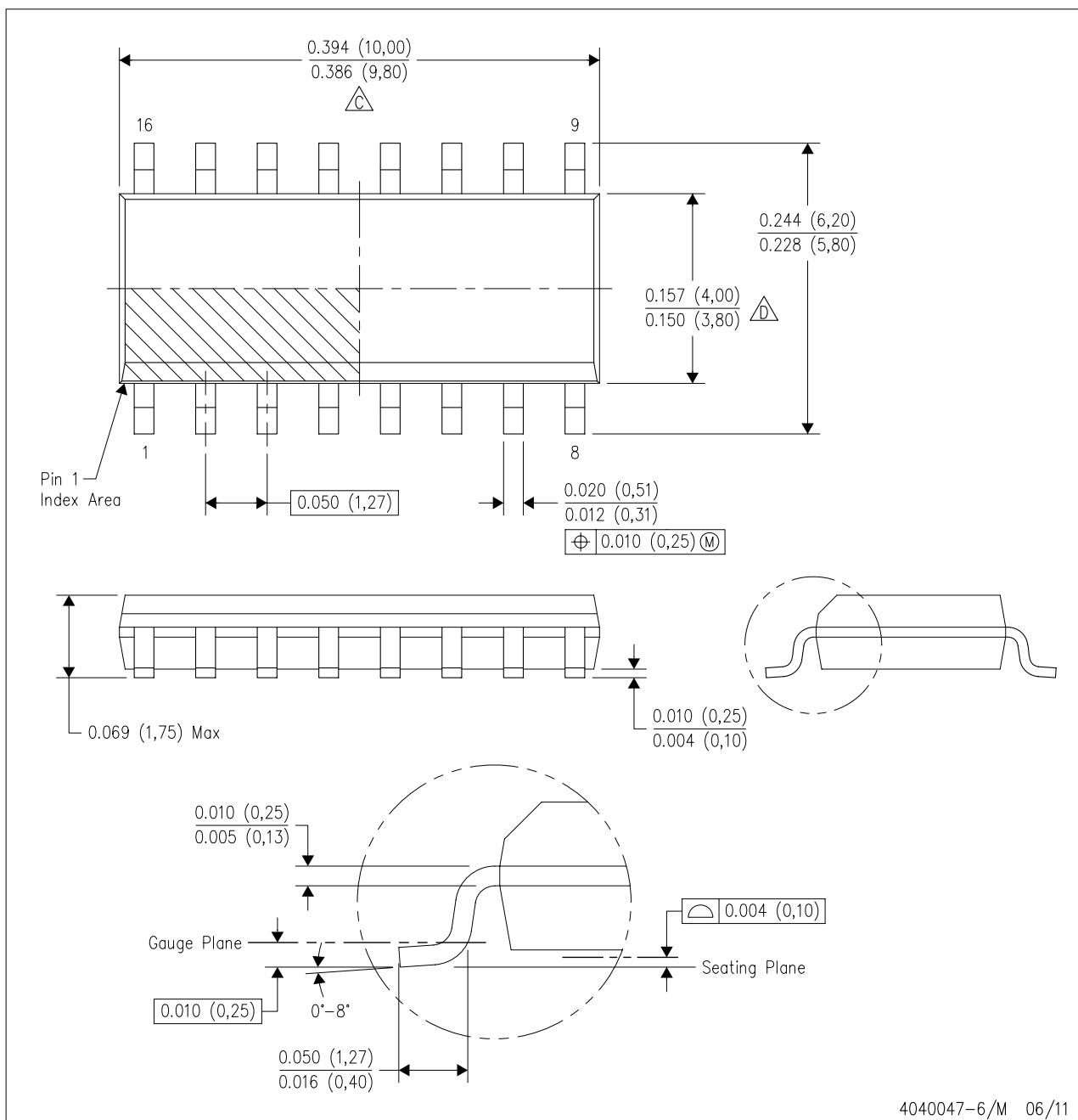
PLASTIC DUAL-IN-LINE PACKAGE



MECHANICAL DATA

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.

Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall

 Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.

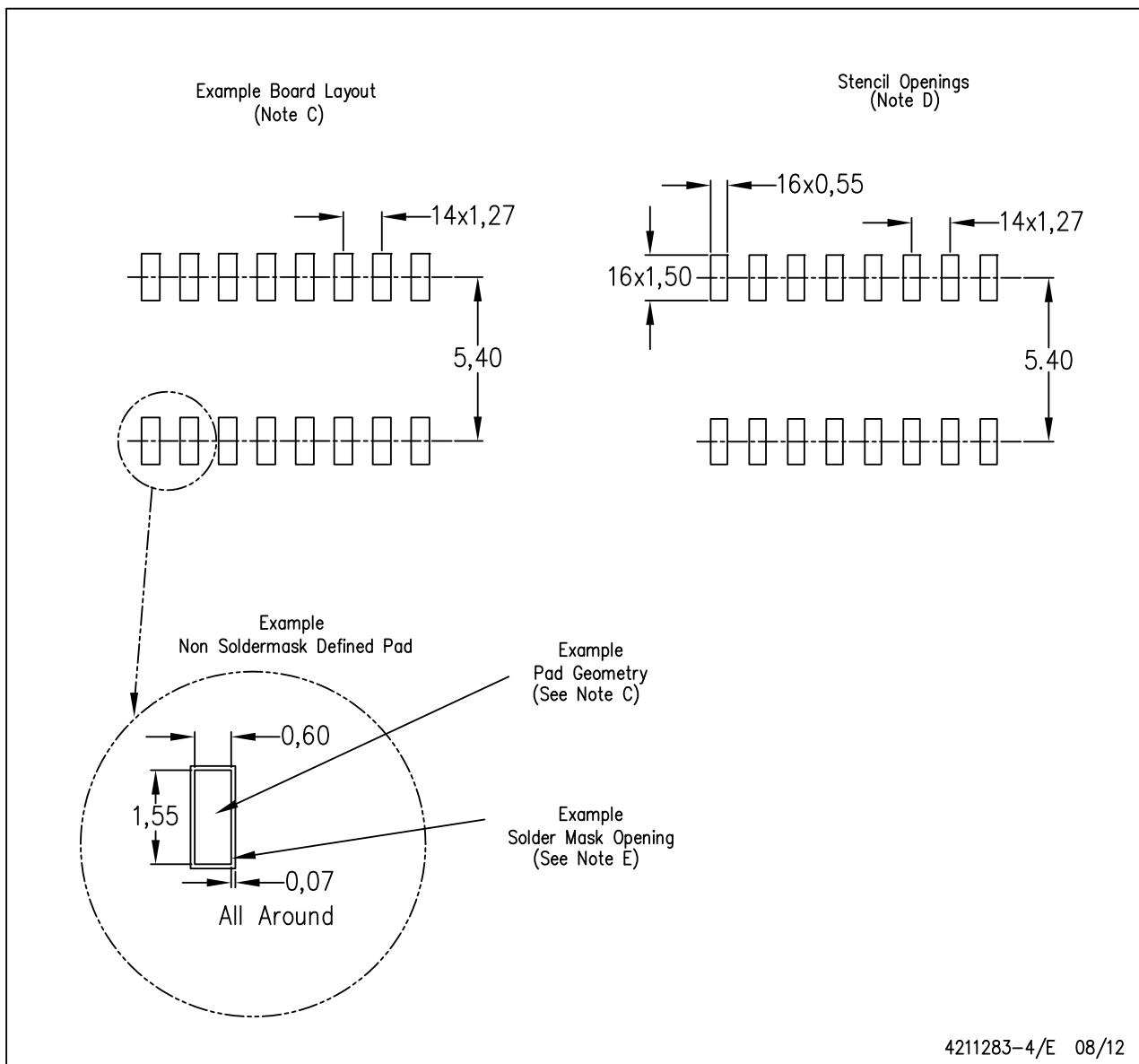
D Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0.43) each side.
E Reference JEDEC MS-012 variation AC.

E. Reference GEDEC MS 012 Variation Ac.

LAND PATTERN DATA

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



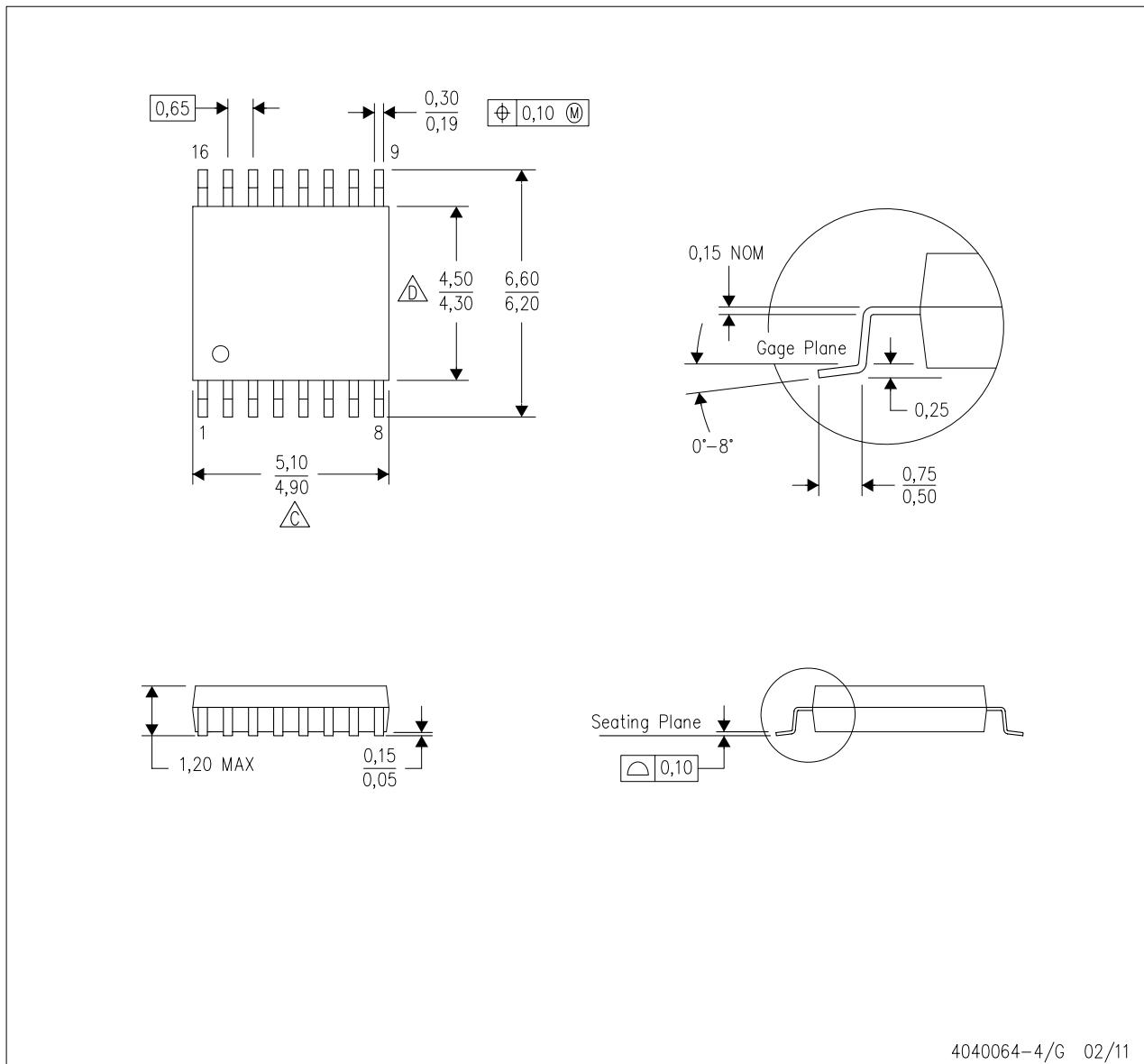
NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4040064-4/G 02/11

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

B. This drawing is subject to change without notice.

 This drawing is subject to change without notice.
 Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 each side.

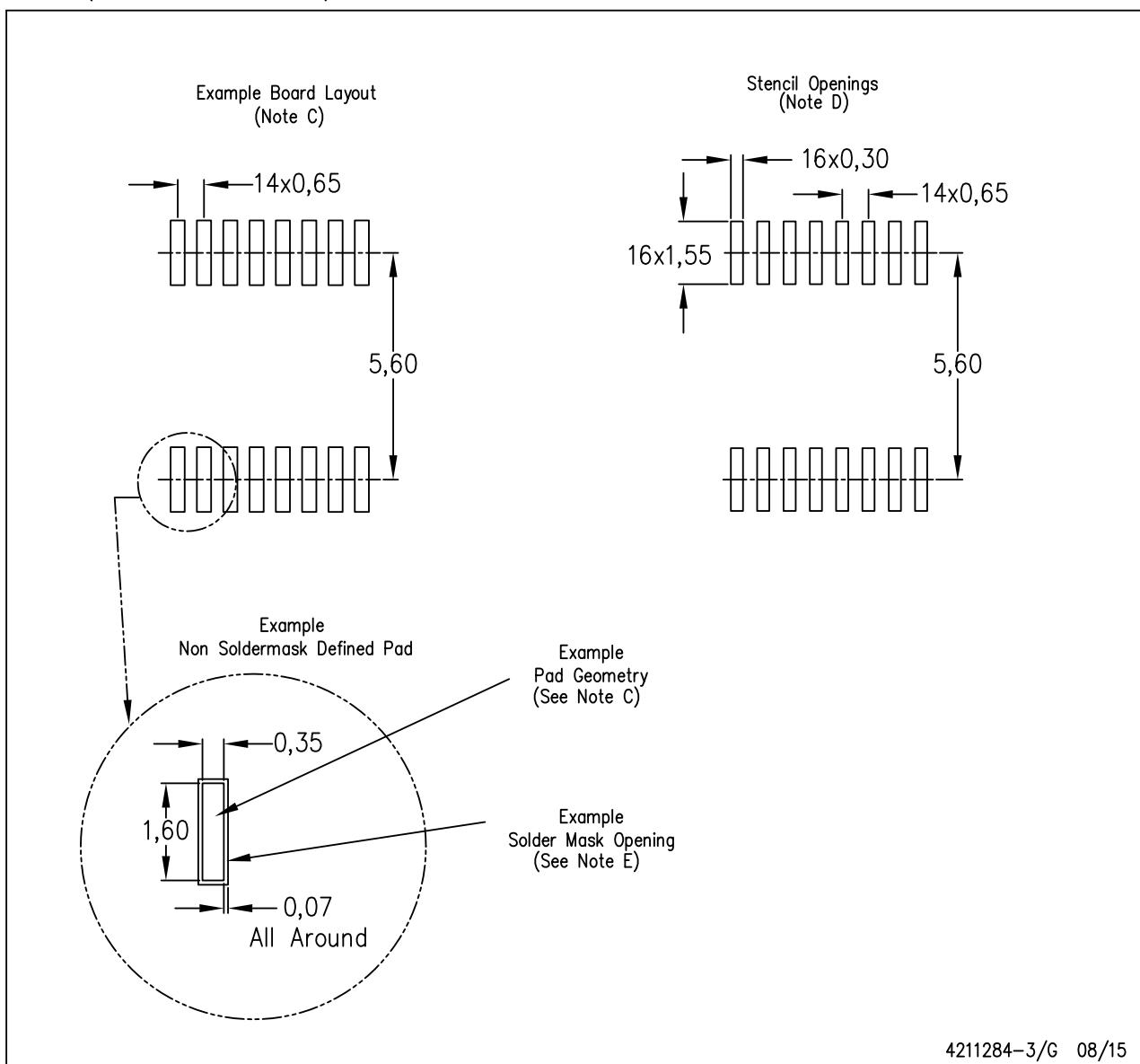
 Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.

E. Falls within JEDDEC MO-153

LAND PATTERN DATA

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4211284-3/G 08/15

NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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