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FEDD51V65165E-02
Issue Date: Aug. 28, 2002

MD51V65165E

4,194,304-Word × 16-Bit DYNAMIC RAM : FAST PAGE MODE TYPE WITH EDO

DESCRIPTION

The MD51V65165E is a 4,194,304-word × 16-bit dynamic RAM fabricated in Oki's silicon-gate CMOS technology. The MD51V65165E achieves high integration, high-speed operation, and low-power consumption because Oki manufactures the device in a quadruple-layer polysilicon/double-layer metal CMOS process. The MD51V65165E is available in a 50-pin plastic TSOP.

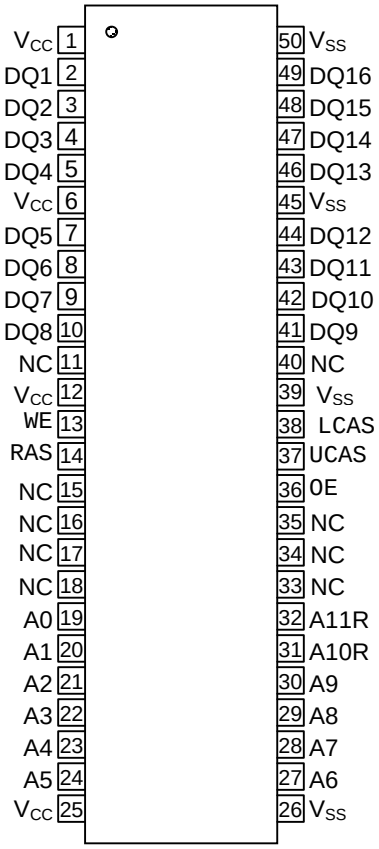
FEATURES

· 4,194,304-word × 16-bit configuration
· Single 3.3V power supply, ±0.3V tolerance
· Input : LVTTL compatible, low input capacitance
· Output : LVTTL compatible, 3-state
· Refresh :
  RAS only refresh : 4096 cycles/64ms
  CAS before RAS refresh, hidden refresh : 4096 cycles/64ms
· Fast page mode with EDO, read modify write capability
· CAS before RAS refresh, hidden refresh, RAS-only refresh capability
· Packages
  50-pin 400mil plastic TSOP (TSOPII50-P-400-0.80-K) (Product : MD51V65165E-xxTA)
  xx indicates speed rank.

PRODUCT FAMILY

Family	Access Time (Max.)				Cycle Time (Min.)	Power Dissipation	
	t_{RAC}	t_{AA}	t_{CAC}	t_{OEA}		Operating (Max.)	Standby (Max.)
MD51V65165E	50ns	25ns	13ns	13ns	84ns	504mW	1.8mW
	60ns	30ns	15ns	15ns	104ns	432mW	

PIN CONFIGURATION (TOP VIEW)

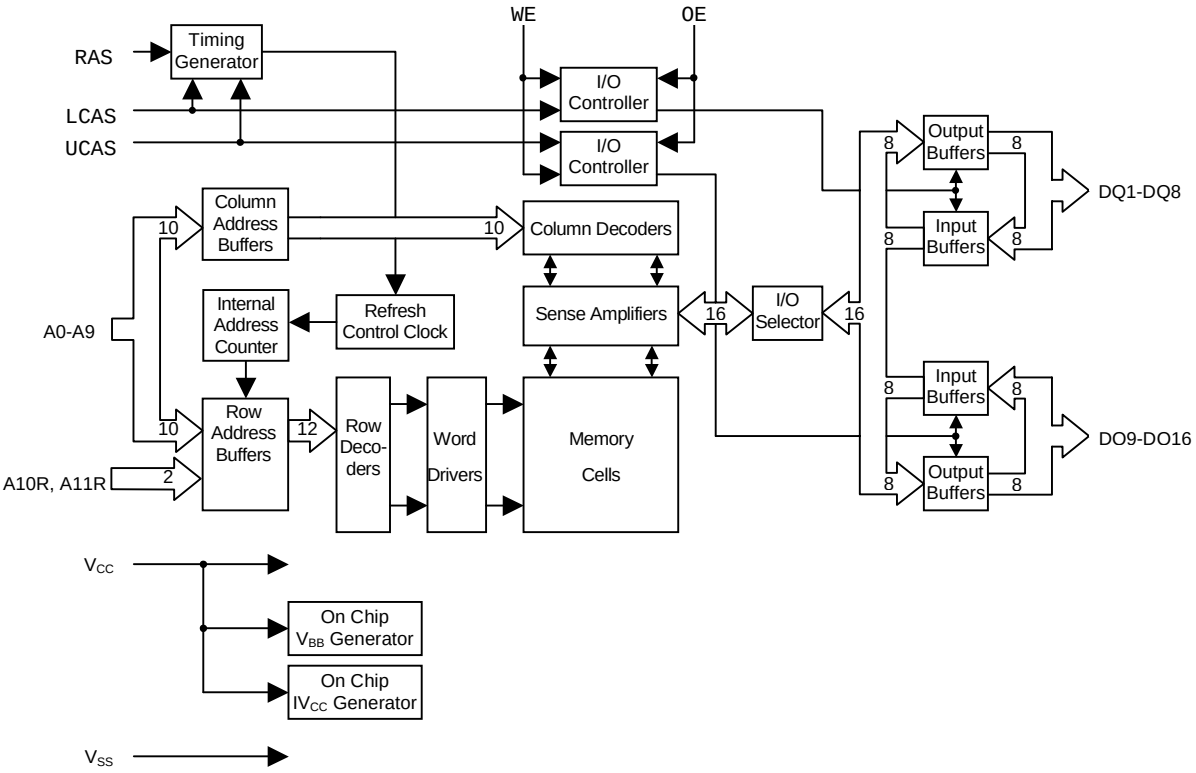


50-Pin Plastic TSOP
(K Type)

Pin Name	Function
A0–A9, A10R, A11R	Address Input
RAS	Row Address Strobe
LCAS	Lower Byte Column Address Strobe
UCAS	Upper Byte Column Address Strobe
DQ1–DQ16	Data Input/Data Output
OE	Output Enable
WE	Write Enable
V_{CC}	Power Supply (3.3V)
V_{SS}	Ground (0V)
NC	No Connection

Note : The same power supply voltage must be provided to every V_{CC} pin, and the same GND voltage level must be provided to every V_{SS} pin.

BLOCK DIAGRAM



FUNCTION TABLE

Input Pin					DQ Pin		Function Mode
RAS	LCAS	UCAS	WE	OE	DQ1-DQ8	DQ9-DQ16	
H	*	*	*	*	High-Z	High-Z	Standby
L	H	H	*	*	High-Z	High-Z	Refresh
L	L	H	H	L	D_{OUT}	High-Z	Lower Byte Read
L	H	L	H	L	High-Z	D_{OUT}	Upper Byte Read
L	L	L	H	L	D_{OUT}	D_{OUT}	Word Read
L	L	H	L	H	D_{IN}	Don't Care	Lower Byte Write
L	H	L	L	H	Don't Care	D_{IN}	Upper Byte Write
L	L	L	L	H	D_{IN}	D_{IN}	Word Write
L	L	L	H	H	High-Z	High-Z	—

* : "H" or "L"

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	–0.5 to V_{CC}+0.5	V
Voltage V_{CC} Supply relative to V_{SS}	V_{CC}	–0.5 to 4.6	V
Short Circuit Output Current	I_{OS}	50	mA
Power Dissipation	P_{D*}	1	W
Operating Temperature	T_{opr}	0 to 70	°C
Storage Temperature	T_{stg}	–55 to 150	°C

*: Ta = 25°C

RECOMMENDED OPERATING CONDITIONS

(Ta = 0 to 70°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{CC}	3.0	3.3	3.6	V
	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.0	—	V_{CC} + 0.3*1	V
Input Low Voltage	V_{IL}	– 0.3*2	—	0.8	V

Notes: *1. The input voltage is V_{CC} + 1.0V when the pulse width is less than 20ns (the pulse width is with respect to the point at which V_{CC} is applied).

*2. The input voltage is V_{SS} − 1.0V when the pulse width is less than 20ns (the pulse width respect to the point at which V_{SS} is applied).

PIN CAPACITANCE

(Vcc = 3.3V ± 0.3V, Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Min.	Max.	Unit
Input Capacitance (A0 – A9, A10R, A11R)	C_{IN1}	—	5	pF
Input Capacitance (RAS, LCAS, UCAS, WE, OE)	C_{IN2}	—	7	pF
Output Capacitance (DQ1 - DQ16)	$C_{I/O}$	—	7	pF

DC CHARACTERISTICS

(V_{CC} = 3.3V ± 0.3V, Ta = 0 to 70°C)

Parameter	Symbol	Condition	MD51V65165 E-50		MD51V65165 E-60		Unit	Note
			Min.	Max.	Min.	Max.		
Output High Voltage	V_{OH}	I_{OH} = –2.0mA	2.4	V_{CC}	2.4	V_{CC}	V	
Output Low Voltage	V_{OL}	I_{OL} = 2mA	0	0.4	0	0.4	V	
Input Leakage Current	I_{LI}	0V ≤ V_I ≤ V_{CC}+0.3V; All other pins not under test = 0V	– 10	10	– 10	10	µA	
Output Leakage Current	I_{LO}	DQ disable 0V ≤ V_O ≤ V_{CC}	– 10	10	– 10	10	µA	
Average Power Supply Current (Operating)	I_{CC1}	RAS, CAS cycling, t_{RC} = Min.	—	140	—	120	mA	1,2
Power Supply Current (Standby)	I_{CC2}	RAS, CAS = V_{IH}	—	2	—	2	mA	1
		RAS, CAS ≥ V_{CC} – 0.2V	—	0.5	—	0.5		
Average Power Supply Current (RAS-only Refresh)	I_{CC3}	RAS cycling, CAS = V_{IH}, t_{RC} = Min.	—	140	—	120	mA	1,2
Power Supply Current (Standby)	I_{CC5}	RAS = V_{IH}, CAS = V_{IL}, DQ = enable	—	5	—	5	mA	1
Average Power Supply Current (CAS before RAS Refresh)	I_{CC6}	RAS = cycling, CAS before RAS	—	140	—	120	mA	1,2
Average Power Supply Current (Fast Page Mode)	I_{CC7}	RAS = V_{IL}, CAS cycling, t_{HPC} = Min.	—	140	—	120	mA	1,3

Notes: 1. I_{CC} Max. is specified as I_{CC} for output open condition.
2. The address can be changed once or less while RAS = V_{IL}.
3. The address can be changed once or less while CAS = V_{IH}.

AC CHARACTERISTICS (1/2)

(V_{CC} = 3.3V ± 0.3V, Ta = 0 to 70°C) Note1,2,3

Parameter	Symbol	MD51V65165 E-50		MD51V65165 E-60		Unit	Note
		Min.	Max.	Min.	Max.		
Random Read or Write Cycle Time	t_{RC}	84	—	104	—	ns	
Read Modify Write Cycle Time	t_{RWC}	110	—	135	—	ns	
Fast Page Mode Cycle Time	t_{HPC}	20	—	25	—	ns	
Fast Page Mode Read Modify Write Cycle Time	t_{HPRWC}	58	—	68	—	ns	
Access Time from RAS	t_{RAC}	—	50	—	60	ns	4, 5, 6
Access Time from CAS	t_{CAC}	—	13	—	15	ns	4,5
Access Time from Column Address	t_{AA}	—	25	—	30	ns	4,6
Access Time from CAS Precharge	t_{CPA}	—	30	—	35	ns	4,13
Access Time from OE	t_{OEA}	—	13	—	15	ns	4
Output Low Impedance Time from CAS	t_{CLZ}	0	—	0	—	ns	4
Data Output Hold After CAS Low	t_{DOH}	5	—	5	—	ns	
CAS to Data Output Buffer Turn-off Delay Time	t_{CEZ}	0	13	0	15	ns	7,8
RAS to Data Output Buffer Turn-off Delay Time	t_{REZ}	0	13	0	15	ns	7,8
OE to Data Output Buffer Turn-off Delay Time	t_{OEZ}	0	13	0	15	ns	7
WE to Data Output Buffer Turn-off Delay Time	t_{WEZ}	0	13	0	15	ns	7
Transition Time	t_T	1	50	1	50	ns	3
Refresh Period	t_{REF}	—	64	—	64	ms	
RAS Precharge Time	t_{RP}	30	—	40	—	ns	
RAS Pulse Width	t_{RAS}	50	10,000	60	10,000	ns	
RAS Pulse Width (Fast Page Mode with EDO)	t_{RASP}	50	100,000	60	100,000	ns	
RAS Hold Time	t_{RSH}	7	—	10	—	ns	
RAS Hold Time referenced to OE	t_{ROH}	7	—	10	—	ns	
CAS Precharge Time (Fast Page Mode with EDO)	t_{CP}	7	—	10	—	ns	15
CAS Pulse Width	t_{CAS}	7	10,000	10	10,000	ns	
CAS Hold Time	t_{CSH}	35	—	40	—	ns	
CAS to RAS Precharge Time	t_{CRP}	5	—	5	—	ns	13
RAS Hold Time from CAS Precharge	t_{RHCP}	30	—	35	—	ns	13
OE Hold Time from CAS (DQ Disable)	t_{CHO}	5	—	5	—	ns	

AC CHARACTERISTICS (2/2)

(V_{CC} = 3.3V ± 0.3V, Ta = 0 to 70°C) Note1,2,3

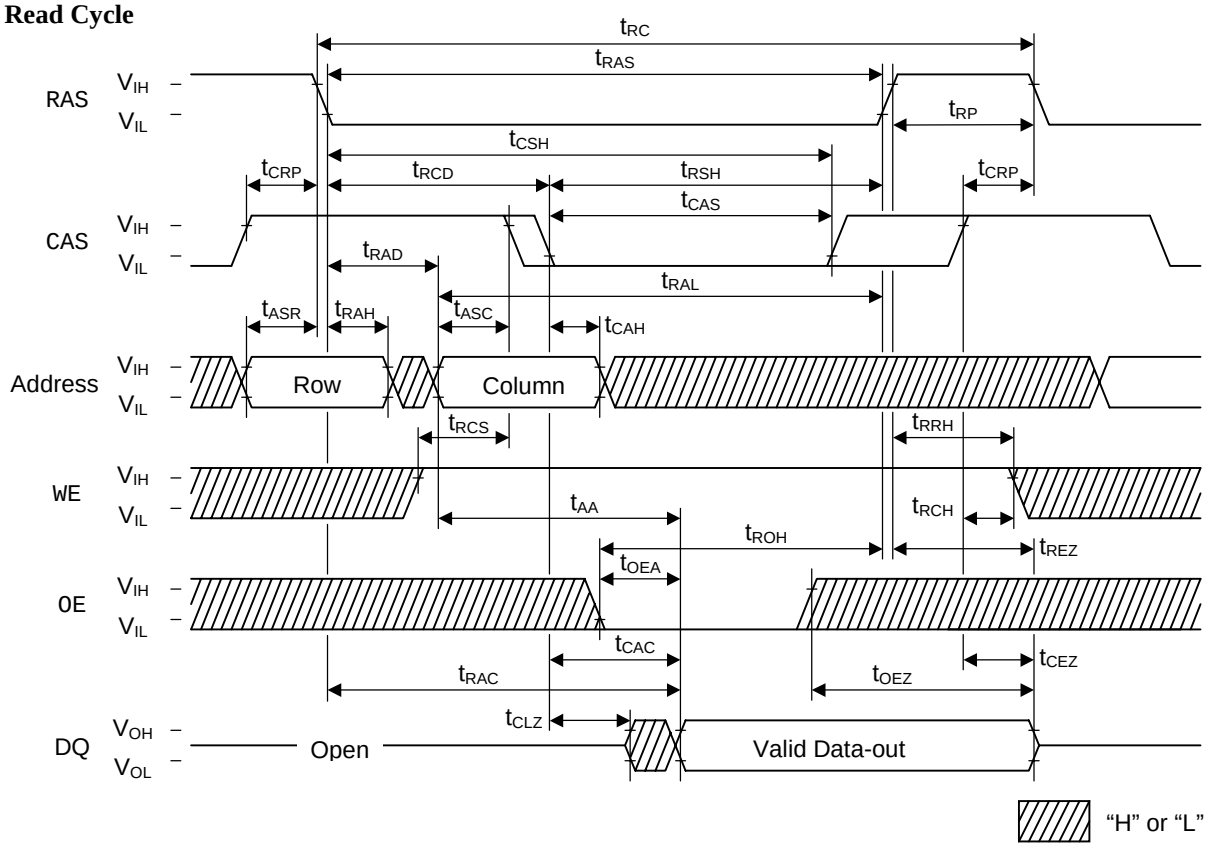
Parameter	Symbol	MD51V65165 E-50		MD51V65165 E-60		Unit	Note
		Min.	Max.	Min.	Max.		
RAS to CAS Delay Time	t_{RCD}	11	37	14	45	ns	5
RAS to Column Address Delay Time	t_{RAD}	9	25	12	30	ns	6
Row Address Set-up Time	t_{ASR}	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	7	—	10	—	ns	
Column Address Set-up Time	t_{ASC}	0	—	0	—	ns	12
Column Address Hold Time	t_{CAH}	7	—	10	—	ns	12
Column Address to RAS Lead Time	t_{RAL}	25	—	30	—	ns	
Read Command Set-up Time	t_{RCS}	0	—	0	—	ns	12
Read Command Hold Time	t_{RCH}	0	—	0	—	ns	9,12
Read Command Hold Time referenced to RAS	t_{RRH}	0	—	0	—	ns	9
Write Command Set-up Time	t_{WCS}	0	—	0	—	ns	10,12
Write Command Hold Time	t_{WCH}	7	—	10	—	ns	12
Write Command Pulse Width	t_{WP}	7	—	10	—	ns	
WE Pulse Width (DQ Disable)	t_{WPE}	7	—	10	—	ns	
OE Command Hold Time	t_{OEH}	7	—	10	—	ns	
OE Precharge Time	t_{OEP}	7	—	10	—	ns	
OE Command Hold Time	t_{OCH}	7	—	10	—	ns	
Write Command to RAS Lead Time	t_{RWL}	7	—	10	—	ns	
Write Command to CAS Lead Time	t_{CWL}	7	—	10	—	ns	14
Data-in Set-up Time	t_{DS}	0	—	0	—	ns	11,12
Data-in Hold Time	t_{DH}	7	—	10	—	ns	11,12
OE to Data-in Delay Time	t_{OED}	13	—	15	—	ns	
CAS to WE Delay Time	t_{CWD}	30	—	34	—	ns	10
Column Address to WE Delay Time	t_{AWD}	42	—	49	—	ns	10
RAS to WE Delay Time	t_{RWD}	67	—	79	—	ns	10
CAS Precharge WE Delay Time	t_{CPWD}	47	—	54	—	ns	10
CAS Active Delay Time from RAS Precharge	t_{RPC}	5	—	5	—	ns	12
RAS to CAS Set-up Time (CAS before RAS)	t_{CSR}	5	—	5	—	ns	12
RAS to CAS Hold Time(CAS before RAS)	t_{CHR}	10	—	10	—	ns	13
WE to RAS Hold Time(CAS before RAS)	t_{WRP}	10	—	10	—	ns	
WE Hold Time(CAS before RAS)	t_{WRH}	10	—	10	—	ns	

Notes:

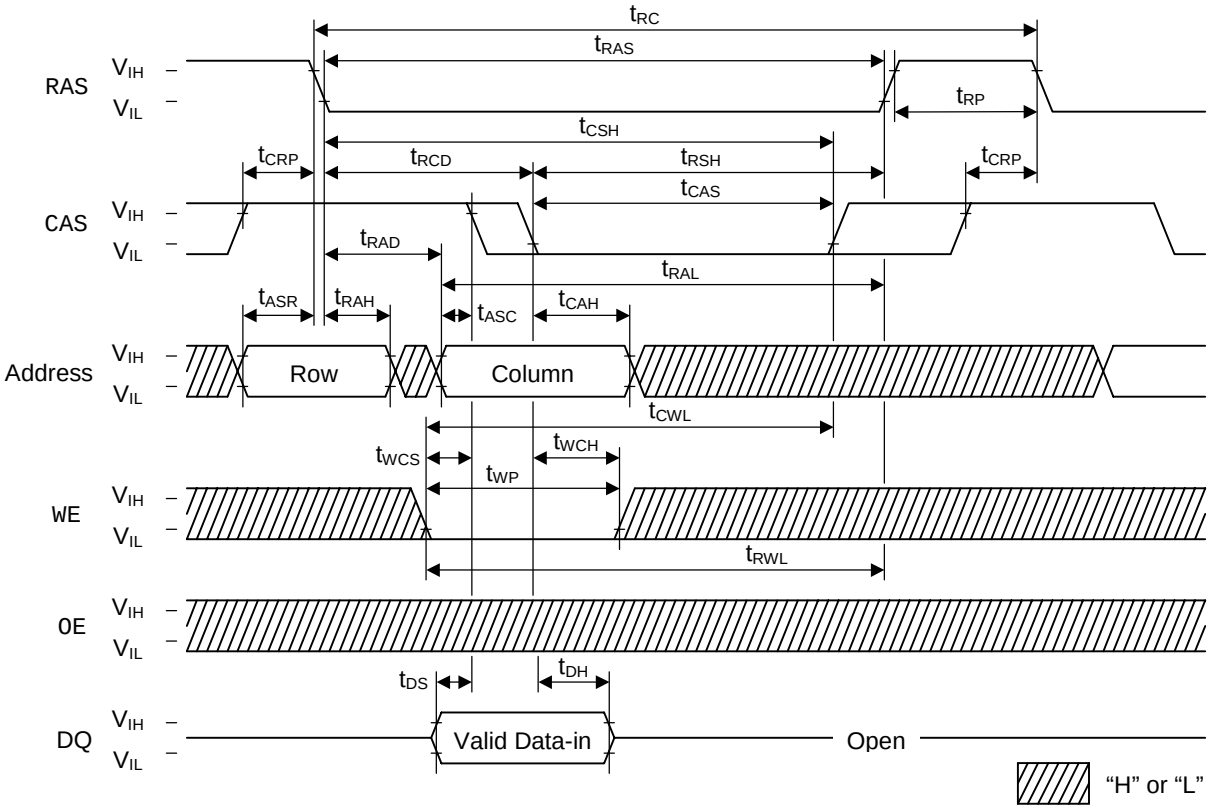
1. A start-up delay of 200μs is required after power-up, followed by a minimum of eight initialization cycles (RAS-only refresh or CAS before RAS refresh) before proper device operation is achieved.
2. The AC characteristics assume t_T = 2ns.
3. V_{IH} (Min.) and V_{IL} (Max.) are reference levels for measuring input timing signals. Transition times (t_T) are measured between V_{IH} and V_{IL}.
4. This parameter is measured with a load circuit equivalent to 1 TTL load and 100pF.
   The output timing reference levels are V_{OH}=2.0 and V_{OL}=0.8V.
5. Operation within the t_{RCD} (Max.) limit ensures that t_{RAC} (Max.) can be met.
   t_{RCD} (Max.) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (Max.) limit, then the access time is controlled by t_{CAC}.
6. Operation within the t_{RAD} (Max.) limit ensures that t_{RAC} (Max.) can be met.
   t_{RAD} (Max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (Max.) limit, then the access time is controlled by t_{AA}.
7. t_{CEZ} (Max.), t_{REZ} (Max.), t_{WEZ} (Max.), and t_{OEZ} (Max.) define the time at which the output achieved the open circuit condition and are not referenced to output voltage levels.
8. t_{CEZ}, and t_{REZ} must be satisfied for open circuit condition.
9. t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. t_{WCS}, t_{CWD}, t_{RWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (Min.), then the cycle is an early write cycle and the data out will remain open circuit (high impedance) throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (Min.), $t_{RWD} \geq t_{RWD}$(Min.), $t_{AWD} \geq t_{AWD}$ (Min.) and $t_{CPWD} \geq t_{CPWD}$ (Min.), then the cycle is a read modify write cycle and data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, then the condition of the data out (at access time) is indeterminate.
11. These parameters are referenced to the UCAS and LCAS, leading edges in an early write cycle, and to the WE leading edge in an OE control write cycle, or a read modify write cycle.
12. These parameters are determined by the falling edge of either UCAS or LCAS, whichever is earlier.
13. These parameters are determined by the rising edge of either UCAS or LCAS, whichever is later.
14. t_{CWL} should be satisfied by both UCAS and LCAS.
15. t_{CP} is determined by the time both UCAS and LCAS are high.

TIMING CHART

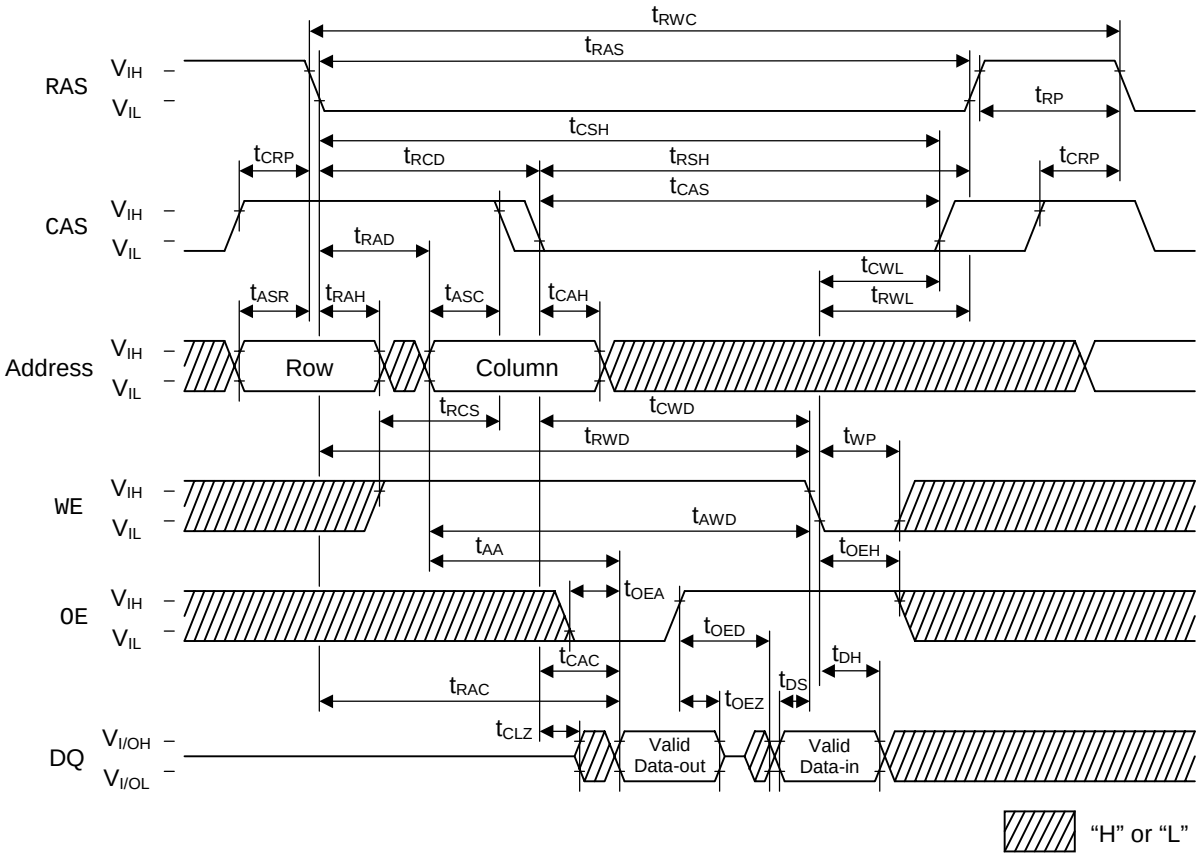
Read Cycle



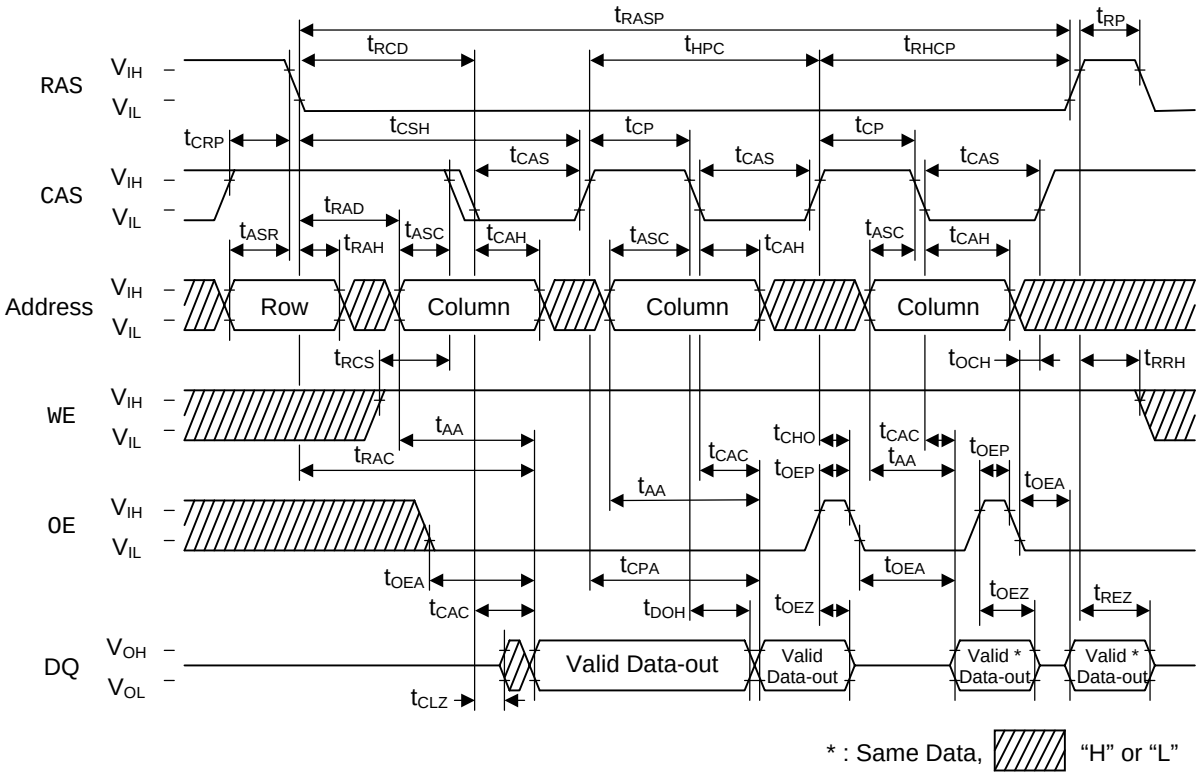
Write Cycle (Early Write)



Read Modify Write Cycle

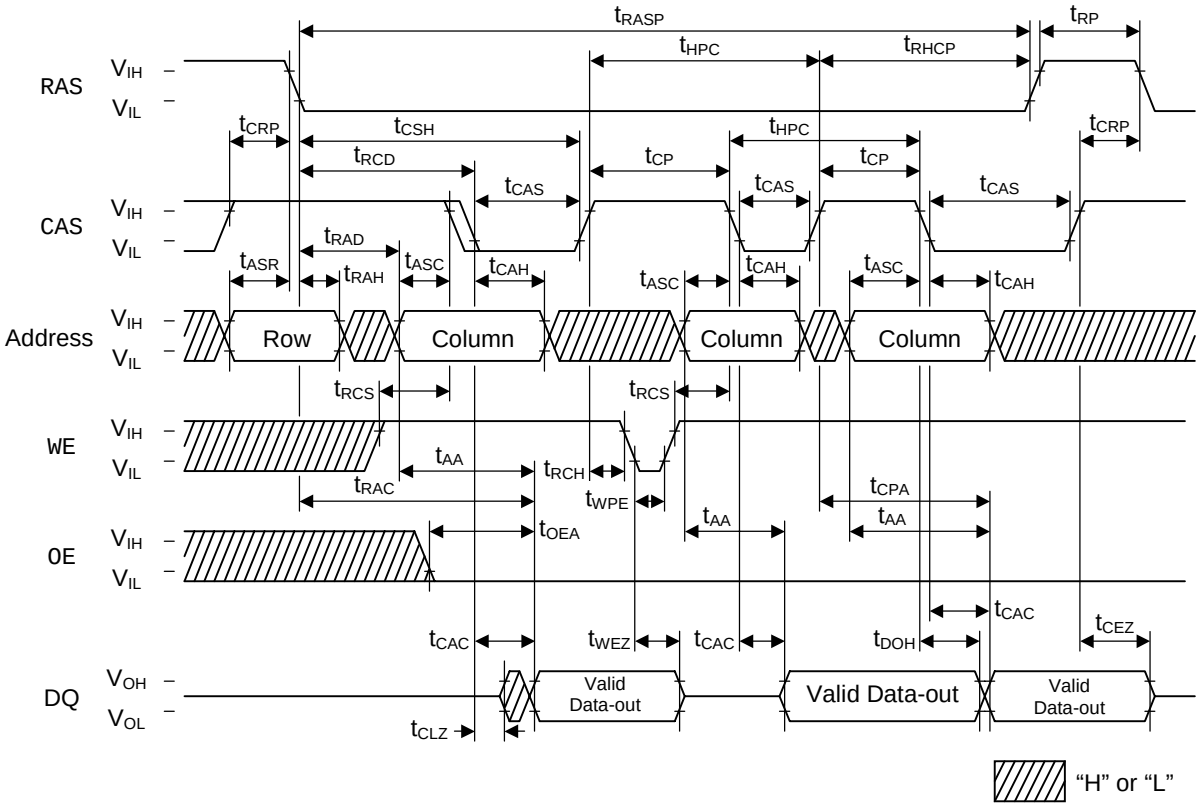


Fast Page Mode Read Cycle (Part-1)



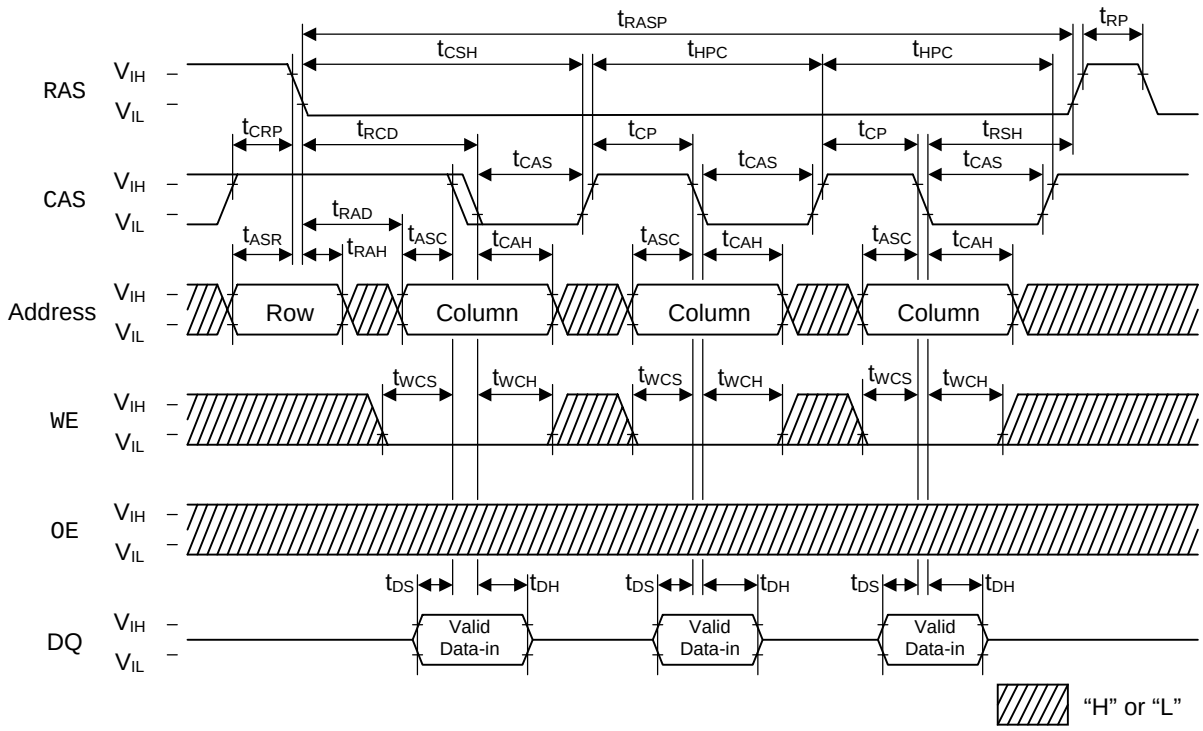
* : Same Data, “H” or “L”

Fast Page Mode Read Cycle (Part-2)

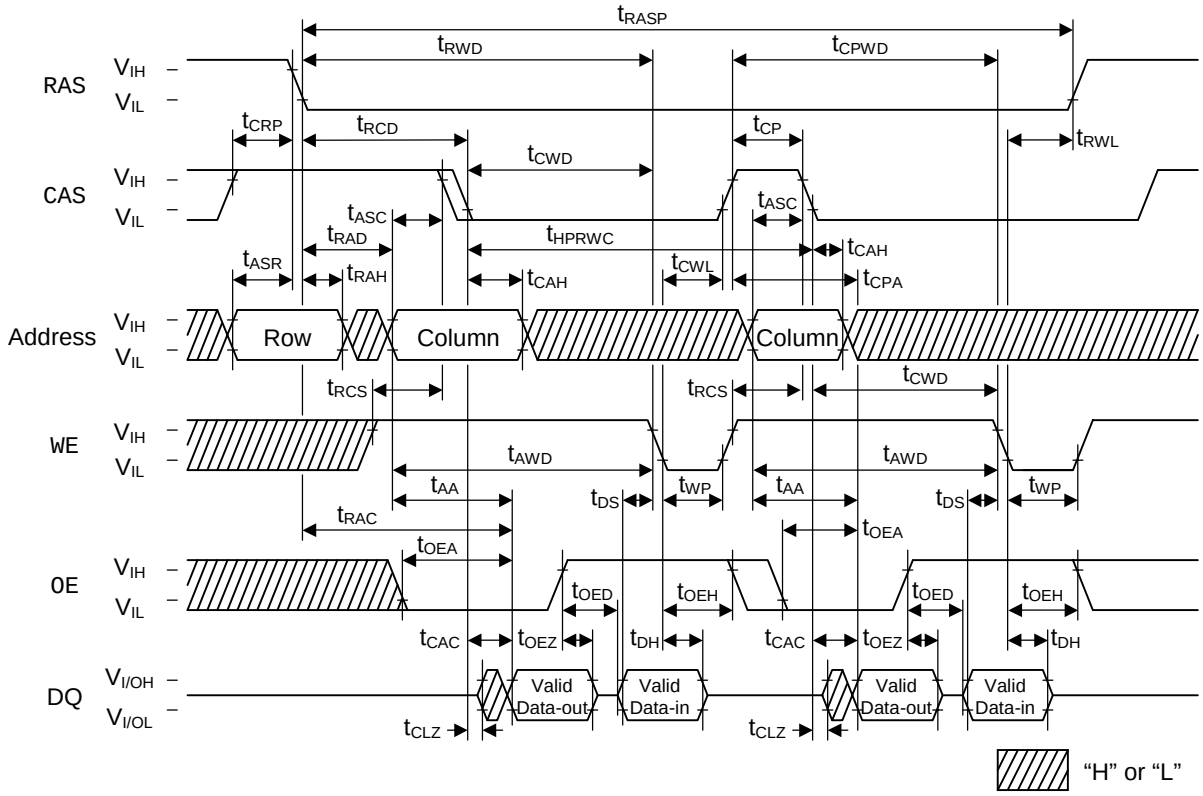


“H” or “L”

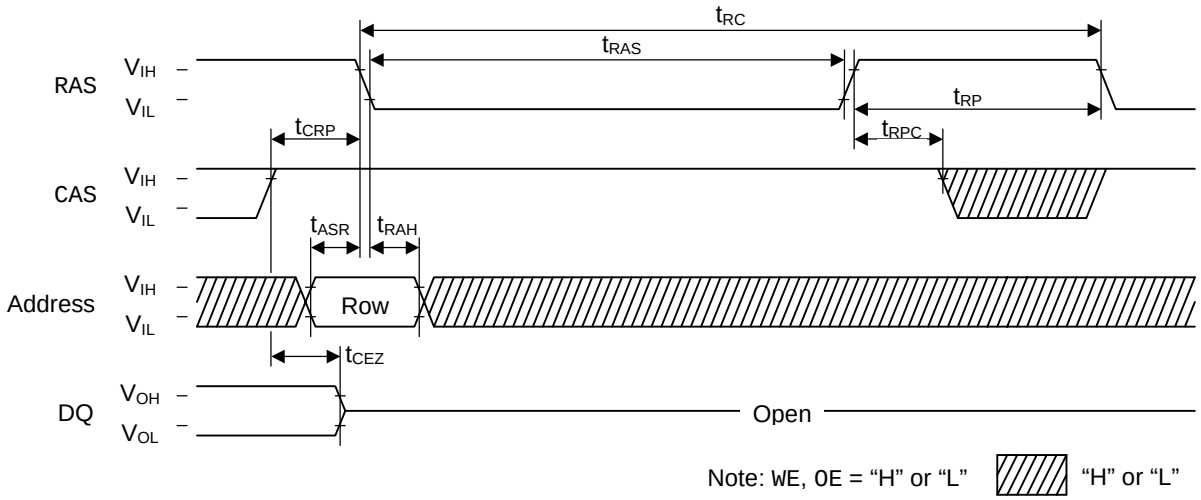
Fast Page Mode Write Cycle (Early Write)



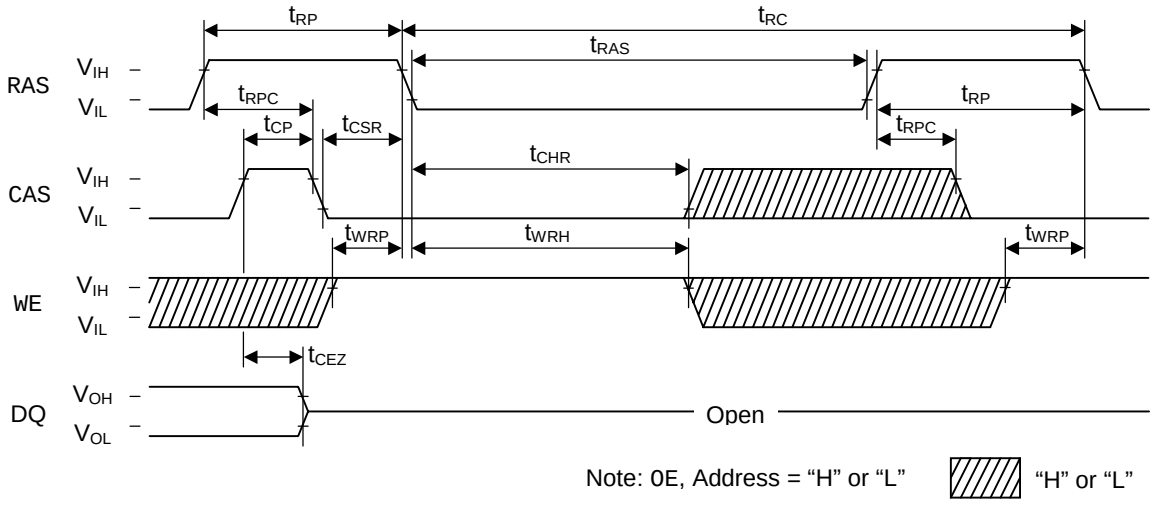
Fast Page Mode Read Modify Write Cycle



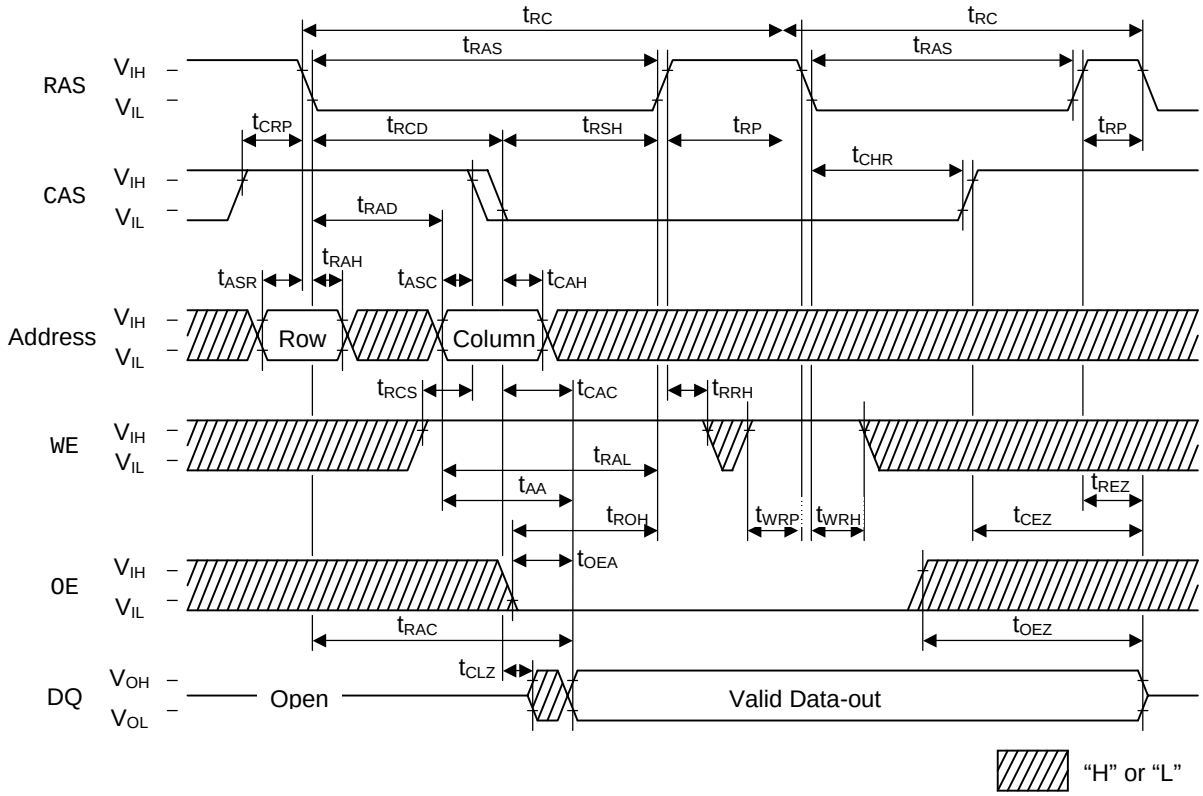
RAS-only Refresh Cycle



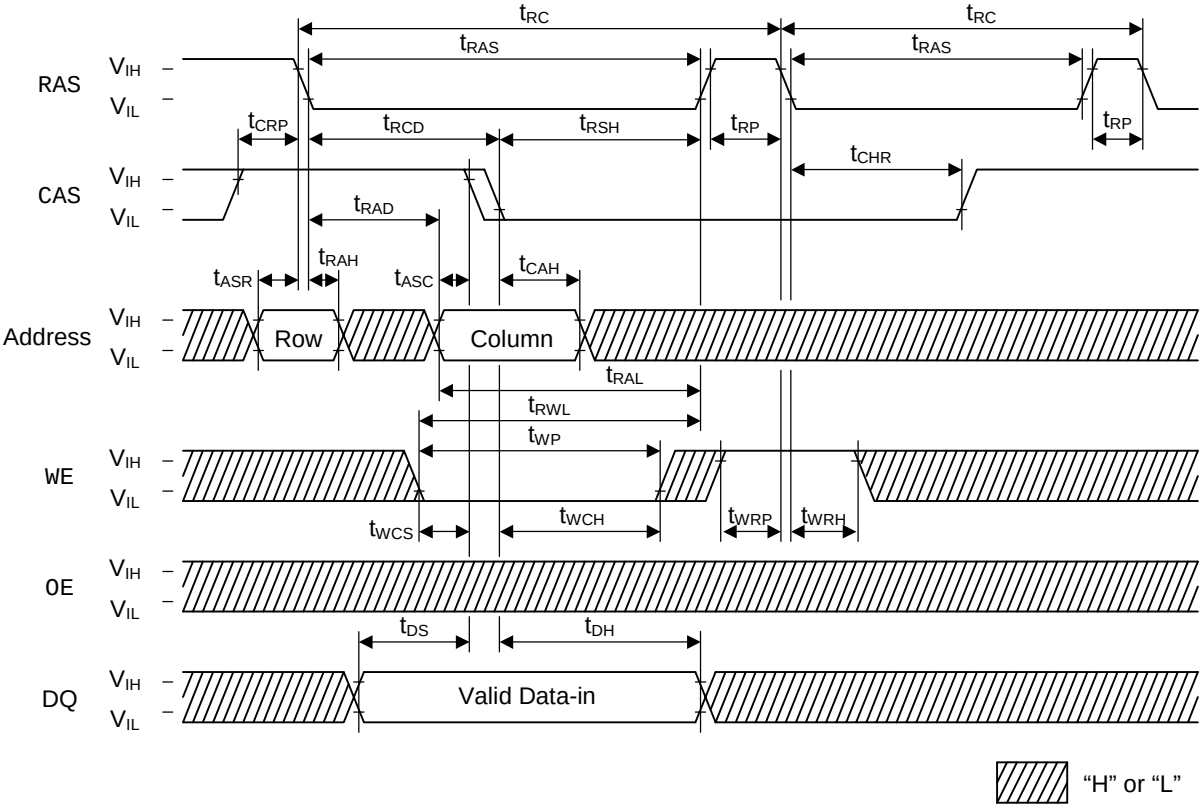
CAS before RAS Refresh Cycle



Hidden Refresh Read Cycle



Hidden Refresh Write Cycle



REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
FEDD51V65165E-01	Jan., 2002	–	–	Final edition 1
FEDD51V65165E-02	Aug., 2002	1, 2	1, 2	Deleted SOJ package

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