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Texas Instruments MSP430F5340IRGZR

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# MSP430F5342, MSP430F5341, MSP430F5340

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# MSP430F534x Mixed Signal Microcontroller

Check for Samples: MSP430F5342, MSP430F5341, MSP430F5340

### FEATURES

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- Low Supply-Voltage Range: 3.6 V Down to 1.8 V
- Ultralow-Power Consumption
  - Active Mode (AM): All System Clocks Active
     290 μA/MHz at 8 MHz, 3 V, Flash Program Execution (Typical)
     150 μA/MHz at 8 MHz, 3 V, RAM Program Execution (Typical)
  - Standby Mode (LPM3): Real-Time Clock With Crystal, Watchdog, and Supply Supervisor Operational, Full RAM Retention, Fast Wake-Up: 1.9 μA at 2.2 V, 2.1 μA at 3 V (Typical) Low-Power Oscillator (VLO), General-Purpose Counter, Watchdog, and Supply Supervisor Operational, Full RAM Retention, Fast Wake-Up: 1.4 μA at 3 V (Typical)
  - Off Mode (LPM4): Full RAM Retention, Supply Supervisor Operational, Fast Wake-Up: 1.1 µA at 3 V (Typical)
  - Shutdown Mode (LPM4.5):
     0.18 µA at 3 V (Typical)
- Wake Up From Standby Mode in 3.5 µs (Typ)
- 16-Bit RISC Architecture, Extended Memory, Up to 25-MHz System Clock
- Flexible Power Management System
  - Fully Integrated LDO With Programmable Regulated Core Supply Voltage
  - Supply Voltage Supervision, Monitoring, and Brownout
- Unified Clock System
  - FLL Control Loop for Frequency Stabilization
  - Low-Power Low-Frequency Internal Clock Source (VLO)
  - Low-Frequency Trimmed Internal Reference Source (REFO)
  - 32-kHz Watch Crystals (XT1)
  - High-Frequency Crystals up to 32 MHz (XT2)

- 16-Bit Timer TA0, Timer\_A With Five Capture/Compare Registers
- 16-Bit Timer TA1, Timer\_A With Three Capture/Compare Registers
- 16-Bit Timer TA2, Timer\_A With Three Capture/Compare Registers
- 16-Bit Timer TB0, Timer\_B With Seven Capture/Compare Shadow Registers
- Two Universal Serial Communication Interfaces (USCI)
  - USCI\_A0 and USCI\_A1 Each Support:
    - Enhanced UART Supports Auto-Baudrate Detection
    - IrDA Encoder and Decoder
    - Synchronous SPI
  - USCI\_B0 and USCI\_B1 Each Support:
    - I<sup>2</sup>C
    - Synchronous SPI
- 12-Bit Analog-to-Digital Converter (ADC) With Internal Reference, Sample-and-Hold, and Autoscan Feature
- Comparator
- Hardware Multiplier Supports 32-Bit Operations
- Serial Onboard Programming, No External Programming Voltage Needed
- Three-Channel Internal DMA
- Basic Timer With Real-Time Clock Feature
- Table 1 Summarizes Family Members
- For Complete Module Descriptions, See the MSP430x5xx and MSP430x6xx Family User's Guide (SLAU208)

### **APPLICATIONS**

- Analog Sensor Systems
- Digital Sensor Systems
- Data Loggers
- General-Purpose Applications

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#### DESCRIPTION

The Texas Instruments MSP430 family of ultralow-power microcontrollers consists of several devices that feature different sets of peripherals targeted for various applications. The architecture, combined with extensive low-power modes, is optimized to achieve extended battery life in portable measurement applications. The device features a powerful 16-bit RISC CPU, 16-bit registers, and constant generators that contribute to maximum code efficiency. The digitally controlled oscillator (DCO) allows the device to wake up from low-power modes to active mode in 3.5  $\mu$ s (typical).

The MSP430F534x are microcontroller configurations with four 16-bit timers, a high-performance 12-bit analogto-digital converter (ADC), two universal serial communication interfaces (USCIs), a hardware multiplier, DMA, a real-time clock module with alarm capabilities, and 38 I/O pins.

Typical applications include analog and digital sensor systems, data loggers, and various general-purpose applications.

Table 1 summarizes the available family members.

					US	SCI				
Device	Flash (KB)	SRAM (KB)	Timer_A <sup>(3)</sup>	Timer_B <sup>(4)</sup>	Channel A: UART, IrDA, SPI	Channel B: SPI, I <sup>2</sup> C	ADC12_A (Ch)	Comp_B (Ch)	I/O	Package Type
MSP430F5342	128	10	5, 3 <sup>(5)</sup> , 3 <sup>(6)</sup>	7	2	2	7 ext, 2 int	5	38	48 RGZ
MSP430F5341	96	8	5, 3 <sup>(5)</sup> , 3 <sup>(6)</sup>	7	2	2	7 ext, 2 int	5	38	48 RGZ
MSP430F5340	64	6	5, 3 <sup>(5)</sup> , 3 <sup>(6)</sup>	7	2	2	7 ext, 2 int	5	38	48 RGZ

#### Table 1. Family Members<sup>(1)(2)</sup>

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

(2) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/packaging.

(3) Each number in the sequence represents an instantiation of Timer\_A with its associated number of capture compare registers and PWM output generators available. For example, a number sequence of 3, 5 would represent two instantiations of Timer\_A, the first instantiation having 3 and the second instantiation having 5 capture compare registers and PWM output generators, respectively.

(4) Each number in the sequence represents an instantiation of Timer\_B with its associated number of capture compare registers and PWM output generators available. For example, a number sequence of 3, 5 would represent two instantiations of Timer\_B, the first instantiation having 3 and the second instantiation having 5 capture compare registers and PWM output generators, respectively.

(5) Only one PWM output and one external capture input available at pin.

(6) No PWM outputs or external capture inputs available at pins.

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#### **Functional Block Diagram**



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#### Pin Designation



NOTE: Exposed thermal pad connection to V<sub>SS</sub> is recommended.

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# INSTRUMENTS

# MSP430F5342, MSP430F5341, MSP430F5340

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#### **Table 2. Terminal Functions**

TERMINAL			DECODIDEION			
NAME	NO.	100	DESCRIPTION			
P6.3/CB3/A3	1	I/O	General-purpose digital I/O Comparator_B input CB3 Analog input A3 – ADC			
P6.4/CB4/A4	2	I/O	General-purpose digital I/O Comparator_B input CB4 Analog input A4 – ADC			
P6.5/CB5/A5	3	I/O	General-purpose digital I/O Comparator_B input CB5 Analog input A5 – ADC			
P5.0/A8/VREF+/VeREF+	4	I/O	General-purpose digital I/O Analog input A8 – ADC Output of reference voltage to the ADC Input for an external reference voltage to the ADC			
P5.1/A9/VREF-/VeREF-	5	I/O	General-purpose digital I/O Analog input A9 – ADC Negative terminal for the ADC's reference voltage for both sources, the internal reference voltage, or an external applied reference voltage			
AVCC1	6		Analog power supply			
P5.4/XIN	7	I/O	General-purpose digital I/O Input terminal for crystal oscillator XT1			
P5.5/XOUT	8	I/O	O General-purpose digital I/O Output terminal of crystal oscillator XT1			
AVSS1	9		Analog ground supply			
DVCC1	10		Digital power supply			
DVSS1	11		Digital ground supply			
VCORE <sup>(2)</sup>	12		Regulated core power supply output (internal usage only, no external current loading)			
P1.0/TA0CLK/ACLK	13	I/O	General-purpose digital I/O with port interrupt TA0 clock signal TA0CLK input ; ACLK output (divided by 1, 2, 4, 8, 16, or 32)			
P1.1/TA0.0	14	I/O	General-purpose digital I/O with port interrupt TA0 CCR0 capture: CCI0A input, compare: Out0 output BSL transmit output			
P1.2/TA0.1	15	I/O	General-purpose digital I/O with port interrupt TA0 CCR1 capture: CCI1A input, compare: Out1 output BSL receive input			
P1.3/TA0.2	16	I/O	General-purpose digital I/O with port interrupt TA0 CCR2 capture: CCI2A input, compare: Out2 output			
P1.4/TA0.3	17	I/O	General-purpose digital I/O with port interrupt TA0 CCR3 capture: CCI3A input compare: Out3 output			
P1.5/TA0.4	18	I/O	General-purpose digital I/O with port interrupt TA0 CCR4 capture: CCI4A input, compare: Out4 output			
P1.6/TA1CLK/CBOUT	19	I/O	General-purpose digital I/O with port interrupt TA1 clock signal TA1CLK input Comparator_B output			

(1) I = input, O = output, N/A = not available

<sup>(2)</sup> VCORE is for internal usage only. No external current loading is possible. VCORE should only be connected to the recommended capacitor value, C<sub>VCORE</sub>.





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#### Table 2. Terminal Functions (continued)

TERMINAL			DESCRIPTION			
NAME	NO.	10.0				
P1.7/TA1.0	20	I/O	General-purpose digital I/O with port interrupt TA1 CCR0 capture: CCI0A input, compare: Out0 output			
P2.7/UCB0STE/UCA0CLK	21	I/O	General-purpose digital I/O with port interrupt Slave transmit enable – USCI_B0 SPI mode Clock signal input – USCI_A0 SPI slave mode Clock signal output – USCI_A0 SPI master mode			
P3.0/UCB0SIMO/UCB0SDA	22	I/O	General-purpose digital I/O Slave in, master out – USCI_B0 SPI mode I2C data – USCI_B0 I2C mode			
P3.1/UCB0SOMI/UCB0SCL	23	I/O	General-purpose digital I/O Slave out, master in – USCI_B0 SPI mode I2C clock – USCI_B0 I2C mode			
P3.2/UCB0CLK/UCA0STE	24	I/O	General-purpose digital I/O Clock signal input – USCI_B0 SPI slave mode Clock signal output – USCI_B0 SPI master mode Slave transmit enable – USCI_A0 SPI mode			
P3.3/UCA0TXD/UCA0SIMO	25	I/O	General-purpose digital I/O Transmit data – USCI_A0 UART mode Slave in, master out – USCI_A0 SPI mode			
P3.4/UCA0RXD/UCA0SOMI	26	I/O	General-purpose digital I/O Receive data – USCI_A0 UART mode Slave out, master in – USCI_A0 SPI mode			
P4.0/PM_UCB1STE/ PM_UCA1CLK	27	I/O	General-purpose digital I/O with reconfigurable port mapping secondary function Default mapping: Slave transmit enable – USCI_B1 SPI mode Default mapping: Clock signal input – USCI_A1 SPI slave mode Default mapping: Clock signal output – USCI_A1 SPI master mode			
P4.1/PM_UCB1SIMO/ PM_UCB1SDA	28	I/O	General-purpose digital I/O with reconfigurable port mapping secondary function Default mapping: Slave in, master out – USCI_B1 SPI mode Default mapping: I2C data – USCI_B1 I2C mode			
P4.2/PM_UCB1SOMI/ PM_UCB1SCL	29	I/O	General-purpose digital I/O with reconfigurable port mapping secondary function Default mapping: Slave out, master in – USCI_B1 SPI mode Default mapping: I2C clock – USCI_B1 I2C mode			
P4.3/PM_UCB1CLK/ PM_UCA1STE	30	I/O	General-purpose digital I/O with reconfigurable port mapping secondary function Default mapping: Clock signal input – USCI_B1 SPI slave mode Default mapping: Clock signal output – USCI_B1 SPI master mode Default mapping: Slave transmit enable – USCI_A1 SPI mode			
DVSS2	31		Digital ground supply			
DVCC2	32		Digital power supply			
P4.4/PM_UCA1TXD/ PM_UCA1SIMO	33	I/O	General-purpose digital I/O with reconfigurable port mapping secondary function Default mapping: Transmit data – USCI_A1 UART mode Default mapping: Slave in, master out – USCI_A1 SPI mode			
P4.5/PM_UCA1RXD/ PM_UCA1SOMI	34	I/O	General-purpose digital I/O with reconfigurable port mapping secondary function Default mapping: Receive data – USCI_A1 UART mode Default mapping: Slave out, master in – USCI_A1 SPI mode			
P4.6/PM_NONE	35	I/O	General-purpose digital I/O with reconfigurable port mapping secondary function Default mapping: no secondary function.			

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	Table 2. Terminal Functions (continued)						
TERMINAL		v(a)(1)					
NAME	NO.	1/0	DESCRIPTION				
P4.7/PM_NONE	36	I/O	General-purpose digital I/O with reconfigurable port mapping secondary function Default mapping: no secondary function.				
P5.7/TB0.1	37	I/O	General-purpose digital I/O TB0 CCR1 capture: CCI1A input, compare: Out1 output				
DVSS3	38		Digital ground supply				
P5.2/XT2IN	39	I/O	General-purpose digital I/O Input terminal for crystal oscillator XT2				
P5.3/XT2OUT	40	I/O	General-purpose digital I/O Output terminal of crystal oscillator XT2				
TEST/SBWTCK <sup>(3)</sup>	41	I	Test mode pin – Selects four wire JTAG operation. Spy-Bi-Wire input clock when Spy-Bi-Wire operation activated				
PJ.0/TDO <sup>(4)</sup>	42	I/O	General-purpose digital I/O JTAG test data output port				
PJ.1/TDI/TCLK <sup>(5)</sup>	43	I/O	General-purpose digital I/O JTAG test data input or test clock input				
PJ.2/TMS <sup>(5)</sup>	44	I/O	General-purpose digital I/O JTAG test mode select				
PJ.3/TCK <sup>(5)</sup>	45	I/O	General-purpose digital I/O JTAG test clock				
RST/NMI/SBWTDIO <sup>(6)</sup>	46	I/O	Reset input active low <sup>(7)</sup> Non-maskable interrupt input Spy-Bi-Wire data input/output when Spy-Bi-Wire operation activated.				
P6.1/CB1/A1	47	I/O	General-purpose digital I/O Comparator_B input CB1 Analog input A1 – ADC				
P6.2/CB2/A2	48	I/O	General-purpose digital I/O Comparator_B input CB2 Analog input A2 – ADC				
Thermal Pad			QFN package pad. Connection to V <sub>SS</sub> is recommended.				

See Bootstrap Loader (BSL) and JTAG Operation for use with BSL and JTAG functions See JTAG Operation for use with JTAG function. (3)

(4)

(5) See JTAG Operation for use with JTAG function.

(6) (7) See Bootstrap Loader (BSL) and JTAG Operation for use with BSL and JTAG functions

When this pin is configured as reset, the internal pullup resistor is enabled by default.

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#### Development Tools Support

All MSP430<sup>™</sup> microcontrollers are supported by a wide variety of software and hardware development tools. Tools are available from TI and various third parties. See them all at www.ti.com/msp430tools.

#### Hardware Features

See the Code Composer Studio for MSP430 User's Guide (SLAU157) for details on the available features.

MSP430 Architecture	4-Wire JTAG	2-Wire JTAG	Break- points (N)	Range Break- points	Clock Control	State Sequencer	Trace Buffer	LPMx.5 Debugging Support
MSP430Xv2	Yes	Yes	8	Yes	Yes	Yes	Yes	No

#### **Recommended Hardware Options**

#### Target Socket Boards

The target socket boards allow easy programming and debugging of the device using JTAG. They also feature header pin outs for prototyping. Target socket boards are orderable individually or as a kit with the JTAG programmer and debugger included. The following table shows the compatible target boards and the supported packages.

Package	Target Board and Programmer Bundle	Target Board Only		
48-pin VQFN (RGZ)	MSP-FET430U48B	MSP-TS430RGZ48B		

#### Experimenter Boards

Experimenter Boards and Evaluation kits are available for some MSP430 devices. These kits feature additional hardware components and connectivity for full system evaluation and prototyping. See <a href="https://www.ti.com/msp430tools">www.ti.com/msp430tools</a> for details.

#### **Debugging and Programming Tools**

Hardware programming and debugging tools are available from TI and from its third party suppliers. See the full list of available tools at www.ti.com/msp430tools.

#### **Production Programmers**

The production programmers expedite loading firmware to devices by programming several devices simultaneously.

Part Number	PC Port	Features	Provider
MSP-GANG	Serial and USB	Program up to eight devices at a time. Works with PC or standalone.	Texas Instruments

#### **Recommended Software Options**

#### **Integrated Development Environments**

Software development tools are available from TI or from third parties. Open source solutions are also available.

This device is supported by Code Composer Studio<sup>™</sup> IDE (CCS).

#### MSP430Ware

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MSP430Ware is a collection of code examples, data sheets, and other design resources for all MSP430 devices delivered in a convenient package. In addition to providing a complete collection of existing MSP430 design resources, MSP430Ware also includes a high-level API called MSP430 Driver Library. This library makes it easy to program MSP430 hardware. MSP430Ware is available as a component of CCS or as a standalone package.



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#### SYS/BIOS

SYS/BIOS is an advanced real-time operating system for the MSP430 microcontrollers. It features preemptive deterministic multi-tasking, hardware abstraction, memory management, and real-time analysis. SYS/BIOS is available free of charge and is provided with full source code.

#### **Command-Line Programmer**

**INSTRUMENTS** 

MSP430 Flasher is an open-source, shell-based interface for programming MSP430 microcontrollers through a FET programmer or eZ430 using JTAG or Spy-Bi-Wire (SBW) communication. MSP430 Flasher can be used to download binary files (.txt or .hex) files directly to the MSP430 microcontroller without the need for an IDE.

#### **Community Resources**

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

#### TI E2E Community

*TI's Engineer-to-Engineer (E2E) Community.* Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas, and help solve problems with fellow engineers.

#### TI Embedded Processors Wiki

*Texas Instruments Embedded Processors Wiki.* Established to help developers get started with embedded processors from Texas Instruments and to foster innovation and growth of general knowledge about the hardware and software surrounding these devices.

#### **Device and Development Tool Nomenclature**

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all MSP430<sup>™</sup> MCU devices and support tools. Each MSP430<sup>™</sup> MCU commercial family member has one of two prefixes: MSP or XMS (for example, MSP430F5259). Texas Instruments recommends two of three possible prefix designators for its support tools: MSP and MSPX. These prefixes represent evolutionary stages of product development from engineering prototypes (with XMS for devices and MSPX for tools) through fully qualified production devices and tools (with MSP for devices and MSP for tools).

Device development evolutionary flow:

**XMS** – Experimental device that is not necessarily representative of the final device's electrical specifications

**MSP** – Fully qualified production device

Support tool development evolutionary flow:

**MSPX** – Development-support product that has not yet completed Texas Instruments internal qualification testing.

**MSP** – Fully-qualified development-support product

XMS devices and MSPX development-support tools are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

MSP devices and MSP development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (XMS) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, PZP) and temperature range (for example, T). Figure 1 provides a legend for reading the complete device name for any family member.

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Part Number Decoder						
MSP 430	F 5 438 A	A I ZQW T	XX			
Processor Family			Optional: Additional Features			
430 MCU Platform			Optional: Tape and Reel			
Device Tv	vpe	Packa	aina			
<b>_</b>	Carias	Ontional: Tar				
	Series	Optional: Ter	nperature Range			
	Feature Set	Optional: A = Rev	vision			
Processor Family	CC = Embedded MSP = Mixed Si XMS = Experime	d RF Radio ignal Processor ental Silicon				
430 MCU Platform	TI's Low Power	Microcontroller Pla	atform			
Device Type	Memory Type C = ROM F = Flash FR = FRAM G = Flash (Value Line) L = No Nonvolatile Memory		Specialized Application AFE = Analog Front End BT = Preprogrammed with Bluetooth BQ = Contactless Power CG = ROM Medical FE = Flash Energy Meter FG = Flash Medical FW = Flash Electronic Flow Meter			
Series	1 Series = Up to 2 Series = Up to 3 Series = Lega 4 Series = Up to	9 8 MHz 9 16 MHz cy 9 16 MHz w/ LCD	5 Series = Up to 25 MHz 6 Series = Up to 25 MHz w/ LCD 0 = Low Voltage Series			
Feature Set	Various Levels of	of Integration With	in a Series			
Optional: A = Revision	N/A					
Optional: Temperature Range	S = 0°C to 50°C C = 0°C to 70°C I = -40°C to 85°C T = -40°C to 105	C 5°C				
Packaging	www.ti.com/pacl	kaging				
Optional: Tape and Reel	T = Small Reel ( R = Large Reel No Markings = 1	(7 inch) (11 inch) ſube or Tray				
Optional: Additional Features	*-EP = Enhance *-HT = Extreme	d Product (-40°C Temperature Part	to 105°C) s (-55°C to 150°C)			

Figure	1	Device	Nomenclature
Iguie		Device	Nomenciature



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### **Short-Form Description**

#### CPU

The MSP430 CPU has a 16-bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand.

The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-toregister operation execution time is one cycle of the CPU clock.

Four of the registers, R0 to R3, are dedicated as program counter, stack pointer, status register, and constant generator, respectively. The remaining registers are general-purpose registers.

Peripherals are connected to the CPU using data, address, and control buses, and can be handled with all instructions.

The instruction set consists of the original 51 instructions with three formats and seven address modes and additional instructions for the expanded address range. Each instruction can operate on word and byte data.



### **Operating Modes**

The MSP430 has one active mode and six software selectable low-power modes of operation. An interrupt event can wake up the device from any of the low-power modes, service the request, and restore back to the low-power mode on return from the interrupt program.

The following seven operating modes can be configured by software:

- Active mode (AM)
- All clocks are active
- Low-power mode 0 (LPM0)
  - CPU is disabled
  - ACLK and SMCLK remain active
  - MCLK is disabled
  - FLL loop control remains active
- Low-power mode 1 (LPM1)
  - CPU is disabled
  - FLL loop control is disabled
  - ACLK and SMCLK remain active
  - MCLK is disabled
- Low-power mode 2 (LPM2)
- CPU is disabled
- MCLK, FLL loop control, and DCOCLK are disabled
- DCO's dc-generator remains enabled
- ACLK remains active

- Low-power mode 3 (LPM3)
  - CPU is disabled
  - MCLK, FLL loop control, and DCOCLK are disabled
  - DCO's dc generator is disabled
  - ACLK remains active
  - Low-power mode 4 (LPM4)
    - CPU is disabled
    - ACLK is disabled
    - MCLK, FLL loop control, and DCOCLK are disabled

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- DCO's dc generator is disabled
- Crystal oscillator is stopped
- Complete data retention
- Low-power mode 4.5 (LPM4.5)
- Internal regulator disabled
- No data retention
- Wakeup from RST/NMI, P1, and P2

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#### Interrupt Vector Addresses

The interrupt vectors and the power-up start address are located in the address range 0FFFFh to 0FF80h. The vector contains the 16-bit address of the appropriate interrupt-handler instruction sequence.

#### Table 3. Interrupt Sources, Flags, and Vectors

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	WORD ADDRESS	PRIORITY
System Reset Power-Up External Reset Watchdog Timeout, Password Violation Flash Memory Password Violation PMM Password Violation	WDTIFG, KEYV (SYSRSTIV) <sup>(1) (2)</sup>	Reset	0FFFEh	63, highest
<b>System NMI</b> PMM Vacant Memory Access JTAG Mailbox	SVMLIFG, SVMHIFG, DLYLIFG, DLYHIFG, VLRLIFG, VLRHIFG, VMAIFG, JMBNIFG, JMBOUTIFG (SYSSNIV) <sup>(1)</sup>	(Non)maskable	0FFFCh	62
<b>User NMI</b> NMI Oscillator Fault Flash Memory Access Violation	NMIIFG, OFIFG, ACCVIFG, BUSIFG (SYSUNIV) <sup>(1) (2)</sup>	(Non)maskable	0FFFAh	61
Comp_B	Comparator B interrupt flags (CBIV) <sup>(1) (3)</sup>	Maskable	0FFF8h	60
ТВО	TB0CCR0 CCIFG0 <sup>(3)</sup>	Maskable	0FFF6h	59
ТВО	TB0CCR1 CCIFG1 to TB0CCR6 CCIFG6, TB0IFG (TB0IV) <sup>(1) (3)</sup>	Maskable	0FFF4h	58
Watchdog Timer_A Interval Timer Mode	WDTIFG	Maskable	0FFF2h	57
USCI_A0 Receive or Transmit	UCA0RXIFG, UCA0TXIFG (UCA0IV) <sup>(1) (3)</sup>	Maskable	0FFF0h	56
USCI_B0 Receive or Transmit	UCB0RXIFG, UCB0TXIFG (UCB0IV) <sup>(1) (3)</sup>	Maskable	0FFEEh	55
ADC12_A	ADC12IFG0 to ADC12IFG15 (ADC12IV) <sup>(1)</sup> (3) (4)	Maskable	0FFECh	54
TAO	TA0CCR0 CCIFG0 <sup>(3)</sup>	Maskable	0FFEAh	53
TAO	TA0CCR1 CCIFG1 to TA0CCR4 CCIFG4, TA0IFG (TA0IV) <sup>(1) (3)</sup>	Maskable	0FFE8h	52
Reserved	Reserved	Maskable	0FFE6h	51
DMA	DMA0IFG, DMA1IFG, DMA2IFG (DMAIV) <sup>(1) (3)</sup>	Maskable	0FFE4h	50
TA1	TA1CCR0 CCIFG0 <sup>(3)</sup>	Maskable	0FFE2h	49
TA1	TA1CCR1 CCIFG1 to TA1CCR2 CCIFG2, TA1IFG (TA1IV) <sup>(1) (3)</sup>	Maskable	0FFE0h	48
I/O Port P1	P1IFG.0 to P1IFG.7 (P1IV) <sup>(1) (3)</sup>	Maskable	0FFDEh	47
USCI_A1 Receive or Transmit	UCA1RXIFG, UCA1TXIFG (UCA1IV) <sup>(1) (3)</sup>	Maskable	0FFDCh	46
USCI_B1 Receive or Transmit	UCB1RXIFG, UCB1TXIFG (UCB1IV) <sup>(1) (3)</sup>	Maskable	0FFDAh	45
TA2	TA2CCR0 CCIFG0 <sup>(3)</sup>	Maskable	0FFD8h	44
TA2	TA2CCR1 CCIFG1 to TA2CCR2 CCIFG2, TA2IFG (TA2IV) <sup>(1) (3)</sup>	Maskable	0FFD6h	43
I/O Port P2	P2IFG.0 to P2IFG.7 (P2IV) <sup>(1)</sup> (3)	Maskable	0FFD4h	42
RTC_A	RTCRDYIFG, RTCTEVIFG, RTCAIFG, RT0PSIFG, RT1PSIFG (RTCIV) <sup>(1) (3)</sup>	Maskable	0FFD2h	41

(1) Multiple source flags

(2) A reset is generated if the CPU tries to fetch instructions from within peripheral space or vacant memory space.

(Non)maskable: the individual interrupt-enable bit can disable an interrupt event, but the general-interrupt enable cannot disable it.

- (3) Interrupt flags are located in the module.
- (4) Only on devices with ADC, otherwise reserved.

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# MSP430F5342, MSP430F5341, MSP430F5340

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#### Table 3. Interrupt Sources, Flags, and Vectors (continued)

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	WORD ADDRESS	PRIORITY
Reserved			0FFD0h	40
	Reserved <sup>(5)</sup>	÷	:	
			0FF80h	0, lowest

(5) Reserved interrupt vectors at addresses are not used in this device and can be used for regular program code if necessary. To maintain compatibility with other devices, it is recommended to reserve these locations.

#### **Memory Organization**

		MSP430F5340	MSP430F5341	MSP430F5342
Memory (flash) Main: interrupt vector	Total Size	64 KB 00FFFFh-00FF80h	96 KB 00FFFFh-00FF80h	128 KB 00FFFFh-00FF80h
	Bank D	N/A	N/A	32 KB 0243FFh-01C400h
Main: and moment	Bank C	N/A	32 KB 01C3FFh-014400h	32 KB 01C3FFh-014400h
Main: code memory	Bank B	32 KB 0143FFh-00C400h	32 KB 0143FFh-00C400h	32 KB 0143FFh-00C400h
	Total Size         664 KB         96 KB           00FFFFh-00FF80h         00FFFFh-00FF80h         00FFFFh-00FF           Bank D         N/A         N/A           Bank D         N/A         32 KB           Bank B         32 KB         32 KB           Bank A         00C3FFh-00C400h         0143FFh-00C400h           Bank A         00C3FFh-004400h         00C3FFh-0044           Sector 3         N/A         N/A           Sector 1         2 KB         2 KB           Sector 2         N/A         2 KB           0033FFh-002C00h         0033FFh-002C0h         0033FFh-002C0h           Sector 1         2 KB         2 KB           002BFFh-001C00h         0023FFh-001C0h         0023FFh-001C0h           Sector 7         2 KB         2 KB           0023FFh-001C00h         0013FFh-0012           Sector 7         2 KB         2 KB           0019FFh-001980h         0019FFh-0012           Info A         128 B         128 B           0019FFh-001980h         0019FFh-0012	32 KB 00C3FFh-004400h	32 KB 00C3FFh-004400h	
	Sector 3	N/A	N/A	2 KB 0043FFh-003C00h
	Sector 2	N/A	2 KB 003BFFh-003400h	2 KB 003BFFh-003400h
RAM	Sector 1	2 KB 0033FFh-002C00h	2 KB 0033FFh-002C00h	2 KB 0033FFh-002C00h
	Sector 0	2 KB 002BFFh-002400h	2 KB 002BFFh-002400h	2 KB 002BFFh-002400h
	Sector 7	2 KB 0023FFh-001C00h	2 KB 0023FFh-001C00h	2 KB 0023FFh-001C00h
	Info A	128 B 0019FFh-001980h	128 B 0019FFh-001980h	128 B 0019FFh-001980h
Information momory (flach)	Info B	128 B 00197Fh-001900h	128 B 00197Fh-001900h	128 B 00197Fh-001900h
mornation memory (nash)	Info C	128 B 0018FFh-001880h	128 B 0018FFh-001880h	128 B 0018FFh-001880h
	Info D	128 B 00187Fh-001800h	128 B 00187Fh-001800h	128 B 00187Fh-001800h
	BSL 3	512 B 0017FFh-001600h	512 B 0017FFh-001600h	512 B 0017FFh-001600h
Bootstrap loader (BSL)	BSL 2	512 B 0015FFh-001400h	512 B 0015FFh-001400h	512 B 0015FFh-001400h
memory (flash)	BSL 1	512 B 0013FFh-001200h	512 B 0013FFh-001200h	512 B 0013FFh-001200h
	BSL 0	512 B 0011FFh-001000h	512 B 0011FFh-001000h	512 B 0011FFh-001000h
Peripherals	Size	4 KB 000FFFh-0h	4 KB 000FFFh-0h	4 KB 000FFFh-0h

#### Table 4. Memory Organization<sup>(1)</sup>

(1) N/A = Not available





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#### Bootstrap Loader (BSL)

The BSL enables users to program the flash memory or RAM using a UART serial interface. Access to the device memory via the BSL is protected by an user-defined password. <u>Usage of the BSL requires four pins as shown in Table 5</u>. BSL entry requires a specific entry sequence on the RST/NMI/SBWTDIO and TEST/SBWTCK pins. For further details on interfacing to development tools and device programmers, see the *MSP430 Hardware Tools User's Guide* (SLAU278). For complete description of the features of the BSL and its implementation, see *MSP430 Programming Via the Bootstrap Loader* (SLAU319).

•		
DEVICE SIGNAL	BSL FUNCTION	
RST/NMI/SBWTDIO	Entry sequence signal	
TEST/SBWTCK	Entry sequence signal	
P1.1	Data transmit	
P1.2	Data receive	
VCC	Power supply	
VSS	Ground supply	

Tahlo 5	RSI	Pin	Requirements	and	Functions
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#### JTAG Operation

#### **JTAG Standard Interface**

The MSP430 family supports the standard JTAG interface which requires four signals for sending and receiving data. The JTAG signals are shared with general-purpose I/O. The TEST/SBWTCK pin is used to enable the JTAG signals. In addition to these signals, the RST/NMI/SBWTDIO is required to interface with MSP430 development tools and device programmers. The JTAG pin requirements are shown in Table 6. For further details on interfacing to development tools and device programmers, see the *MSP430 Hardware Tools User's Guide* (SLAU278). For a complete description of the features of the JTAG interface and its implementation, see *MSP430 Programming Via the JTAG Interface* (SLAU320).

DEVICE SIGNAL	DIRECTION	FUNCTION
PJ.3/TCK	IN	JTAG clock input
PJ.2/TMS	IN	JTAG state control
PJ.1/TDI/TCLK	IN	JTAG data input, TCLK input
PJ.0/TDO	OUT	JTAG data output
TEST/SBWTCK	IN	Enable JTAG pins
RST/NMI/SBWTDIO	IN	External reset
VCC		Power supply
VSS		Ground supply

#### **Table 6. JTAG Pin Requirements and Functions**

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#### **Spy-Bi-Wire Interface**

In addition to the standard JTAG interface, the MSP430 family supports the two wire Spy-Bi-Wire interface. Spy-Bi-Wire can be used to interface with MSP430 development tools and device programmers. The Spy-Bi-Wire interface pin requirements are shown in Table 7. For further details on interfacing to development tools and device programmers, see the MSP430 Hardware Tools User's Guide (SLAU278). For a complete description of the features of the JTAG interface and its implementation, see MSP430 Programming Via the JTAG Interface (SLAU320).

•	
DIRECTION	FUNCTION
IN	Spy-Bi-Wire clock input
IN, OUT	Spy-Bi-Wire data input/output
	Power supply
	Ground supply
	DIRECTION IN IN, OUT

#### Table 7. Spy-Bi-Wire Pin Requirements and Functions

#### Flash Memory

The flash memory can be programmed via the JTAG port, Spy-Bi-Wire (SBW), the BSL, or in-system by the CPU. The CPU can perform single-byte, single-word, and long-word writes to the flash memory. Features of the flash memory include:

- Flash memory has n segments of main memory and four segments of information memory (A to D) of 128 bytes each. Each segment in main memory is 512 bytes in size.
- Segments 0 to n may be erased in one step, or each segment may be individually erased.
- Segments A to D can be erased individually. Segments A to D are also called information memory.
- Segment A can be locked separately.

#### **RAM Memory**

The RAM memory is made up of n sectors. Each sector can be completely powered down to save leakage, however all data is lost. Features of the RAM memory include:

- RAM memory has n sectors. The size of a sector can be found in Memory Organization.
- Each sector 0 to n can be complete disabled, however data retention is lost.
- Each sector 0 to n automatically enters low power retention mode when possible.

#### Peripherals

Peripherals are connected to the CPU through data, address, and control buses and can be handled using all instructions. For complete module descriptions, see the MSP430x5xx and MSP430x6xx Family User's Guide (SLAU208).

#### **Digital I/O**

There are up to eight 8-bit I/O ports implemented: For 80 pin options, P1, P2, P3, P4, P5, P6, and P7 are complete. P8 is reduced to 3-bit I/O. For 64 pin options, P3 and P5 are reduced to 5-bit I/O and 6-bit I/O, respectively, and P7 and P8 are completely removed. Port PJ contains four individual I/O ports, common to all devices.

- All individual I/O bits are independently programmable. ٠
- Any combination of input, output, and interrupt conditions is possible.
- Pullup or pulldown on all ports is programmable.
- Drive strength on all ports is programmable.
- Edge-selectable interrupt and LPM4.5 wakeup input capability is available for all bits of ports P1 and P2.
- Read and write access to port-control registers is supported by all instructions.
- Ports can be accessed byte-wise (P1 through P8) or word-wise in pairs (PA through PD).

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#### Port Mapping Controller

The port mapping controller allows the flexible and reconfigurable mapping of digital functions to port P4.

#### Table 8. Port Mapping, Mnemonics and Functions

VALUE	PxMAPy MNEMONIC	INPUT PIN FUNCTION	OUTPUT PIN FUNCTION	
0	PM_NONE	None	DVSS	
4	PM_CBOUT0	-	Comparator_B output	
I	PM_TB0CLK	TB0 clock input		
2	PM_ADC12CLK	-	ADC12CLK	
2	PM_DMAE0	DMAE0 input		
2	PM_SVMOUT	-	SVM output	
3	PM_TB0OUTH	TB0 high impedance input TB0OUTH		
4	PM_TB0CCR0A	TB0 CCR0 capture input CCI0A	TB0 CCR0 compare output Out0	
5	PM_TB0CCR1A	TB0 CCR1 capture input CCI1A	TB0 CCR1 compare output Out1	
6	PM_TB0CCR2A	TB0 CCR2 capture input CCI2A	TB0 CCR2 compare output Out2	
7	PM_TB0CCR3A	TB0 CCR3 capture input CCI3A	TB0 CCR3 compare output Out3	
8	PM_TB0CCR4A	TB0 CCR4 capture input CCI4A	TB0 CCR4 compare output Out4	
9	PM_TB0CCR5A	TB0 CCR5 capture input CCI5A	TB0 CCR5 compare output Out5	
10	PM_TB0CCR6A	TB0 CCR6 capture input CCI6A	TB0 CCR6 compare output Out6	
11	PM_UCA1RXD	USCI_A1 UART RXD (Direction controlled by USCI - input) USCI_A1 SPI slave out master in (direction controlled by USCI)		
11	PM_UCA1SOMI			
10	PM_UCA1TXD	USCI_A1 UART TXD (Direction	on controlled by USCI - output)	
12	PM_UCA1SIMO	USCI_A1 SPI slave in master out (direction controlled by USCI)		
10	PM_UCA1CLK	USCI_A1 clock input/output (	(direction controlled by USCI)	
15	PM_UCB1STE	USCI_B1 SPI slave transmit enable (direction controlled by USCI)		
14	PM_UCB1SOMI	USCI_B1 SPI slave out master	in (direction controlled by USCI)	
14	PM_UCB1SCL	USCI_B1 I2C clock (open drain a	and direction controlled by USCI)	
15	PM_UCB1SIMO	USCI_B1 SPI slave in master o	ut (direction controlled by USCI)	
15	PM_UCB1SDA	USCI_B1 I2C data (open drain a	and direction controlled by USCI)	
16	PM_UCB1CLK	USCI_B1 clock input/output (	(direction controlled by USCI)	
10	PM_UCA1STE	USCI_A1 SPI slave transmit ena	ble (direction controlled by USCI)	
17	PM_CBOUT1	None	Comparator_B output	
18	PM_MCLK	None	MCLK	
19-30	Reserved	None	DVSS	
31 (0FFh) <sup>(1)</sup>	PM_ANALOG	Disables the output driver as well as parasitic cross currents wh	Disables the output driver as well as the input Schmitt-trigger to prevent parasitic cross currents when applying analog signals.	

(1) The value of the PM\_ANALOG mnemonic is set to 0FFh. The port mapping registers are only 5 bits wide, and the upper bits are ignored, which results in a read out value of 31.



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Table 9. Default Mapping					
PIN	PxMAPy MNEMONIC	INPUT PIN FUNCTION	OUTPUT PIN FUNCTION		
P4.0/P4MAP0	PM_UCB1STE/PM_UCA1CLK	USCI_B1 SPI slave transmit ena USCI_A1 clock input/output (	ble (direction controlled by USCI) direction controlled by USCI)		
P4.1/P4MAP1	PM_UCB1SIMO/PM_UCB1SDA	USCI_B1 SPI slave in master of USCI_B1 I2C data (open drain a	ut (direction controlled by USCI) and direction controlled by USCI)		
P4.2/P4MAP2	PM_UCB1SOMI/PM_UCB1SCL	USCI_B1 SPI slave out master USCI_B1 I2C clock (open drain a	in (direction controlled by USCI) and direction controlled by USCI)		
P4.3/P4MAP3	PM_UCB1CLK/PM_UCA1STE	USCI_A1 SPI slave transmit ena USCI_B1 clock input/output (	ble (direction controlled by USCI) direction controlled by USCI)		
P4.4/P4MAP4	PM_UCA1TXD/PM_UCA1SIMO	USCI_A1 UART TXD (Direction USCI_A1 SPI slave in master of USC	n controlled by USCI - output) ut (direction controlled by USCI)		
P4.5/P4MAP5	PM_UCA1RXD/PM_UCA1SOMI	USCI_A1 UART RXD (Directi USCI_A1 SPI slave out master	on controlled by USCI - input) in (direction controlled by USCI)		
P4.6/P4MAP6	PM_NONE	None	DVSS		
P4.7/P4MAP7	PM_NONE	None	DVSS		

#### **Oscillator and System Clock**

The clock system in the MSP430F534x family of devices is supported by the Unified Clock System (UCS) module that includes support for a 32-kHz watch crystal oscillator (XT1 LF mode; XT1 HF mode not supported), an internal very-low-power low-frequency oscillator (VLO), an internal trimmed low-frequency oscillator (REFO), an integrated internal digitally-controlled oscillator (DCO), and a high-frequency crystal oscillator XT2. The UCS module is designed to meet the requirements of both low system cost and low-power consumption. The UCS module features digital frequency locked loop (FLL) hardware that, in conjunction with a digital modulator, stabilizes the DCO frequency to a programmable multiple of the selected FLL reference frequency. The internal DCO provides a fast turn-on clock source and stabilizes in 3.5 µs (typical). The UCS module provides the following clock signals:

- Auxiliary clock (ACLK), sourced from a 32-kHz watch crystal (XT1), a high-frequency crystal (XT2), the internal low-frequency oscillator (VLO), the trimmed low-frequency oscillator (REFO), or the internal digitally-controlled oscillator (DCO).
- Main clock (MCLK), the system clock used by the CPU. MCLK can be sourced by same sources made available to ACLK.
- Sub-Main clock (SMCLK), the subsystem clock used by the peripheral modules. SMCLK can be sourced by same sources made available to ACLK.
- ACLK/n, the buffered output of ACLK, ACLK/2, ACLK/4, ACLK/8, ACLK/16, ACLK/32.

#### **Power Management Module (PMM)**

The PMM includes an integrated voltage regulator that supplies the core voltage to the device and contains programmable output levels to provide for power optimization. The PMM also includes supply voltage supervisor (SVS) and supply voltage monitoring (SVM) circuitry, as well as brownout protection. The brownout circuit is implemented to provide the proper internal reset signal to the device during power-on and power-off. The SVS and SVM circuitry detects if the supply voltage drops below a user-selectable level and supports both supply voltage supervision (the device is automatically reset) and supply voltage monitoring (the device is not automatically reset). SVS and SVM circuitry is available on the primary supply and core supply.

#### Hardware Multiplier

The multiplication operation is supported by a dedicated peripheral module. The module performs operations with 32-bit, 24-bit, 16-bit, and 8-bit operands. The module is capable of supporting signed and unsigned multiplication as well as signed and unsigned multiply and accumulate operations.





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### Real-Time Clock (RTC\_A)

The RTC\_A module can be used as a general-purpose 32-bit counter (counter mode) or as an integrated realtime clock (RTC) (calendar mode). In counter mode, the RTC\_A also includes two independent 8-bit timers that can be cascaded to form a 16-bit timer/counter. Both timers can be read and written by software. Calendar mode integrates an internal calendar which compensates for months with less than 31 days and includes leap year correction. The RTC\_A also supports flexible alarm functions and offset-calibration hardware.

#### Watchdog Timer (WDT\_A)

The primary function of the watchdog timer (WDT\_A) module is to perform a controlled system restart after a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the module can be configured as an interval timer and can generate interrupts at selected time intervals.

#### System Module (SYS)

The SYS module handles many of the system functions within the device. These include power on reset and power up clear handling, NMI source selection and management, reset interrupt vector generators, bootstrap loader entry mechanisms, as well as configuration management (device descriptors). It also includes a data exchange mechanism via JTAG called a JTAG mailbox that can be used in the application.

INTERRUPT VECTOR REGISTER	ADDRESS	INTERRUPT EVENT	VALUE	PRIORITY
SYSRSTIV, System Reset	019Eh	No interrupt pending	00h	
		Brownout (BOR)	02h	Highest
		RST/NMI (POR)	04h	
		PMMSWBOR (BOR)	06h	
		Wakeup from LPMx.5	08h	
		Security violation (BOR)	0Ah	
		SVSL (POR)	0Ch	
		SVSH (POR)	0Eh	
		SVML_OVP (POR)	10h	
		SVMH_OVP (POR)	12h	
		PMMSWPOR (POR)	14h	
		WDT timeout (PUC)	16h	
		WDT password violation (PUC)	18h	
		KEYV flash password violation (PUC)	1Ah	
		Reserved	1Ch	
		Peripheral area fetch (PUC)	1Eh	
		PMM password violation (PUC)	20h	
		Reserved	22h to 3Eh	Lowest
SYSSNIV, System NMI	019Ch	No interrupt pending	00h	
		SVMLIFG	02h	Highest
		SVMHIFG	04h	
		SVSMLDLYIFG	06h	
		SVSMHDLYIFG	08h	
		VMAIFG	0Ah	
		JMBINIFG	0Ch	
		JMBOUTIFG	0Eh	
		SVMLVLRIFG	10h	
		SVMHVLRIFG	12h	
		Reserved	14h to 1Eh	Lowest

#### Table 10. System Module Interrupt Vector Registers



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Table 10. System Module Interrupt Vector Registers (continued)				
INTERRUPT VECTOR REGISTER	ADDRESS	INTERRUPT EVENT	VALUE	PRIORITY
SYSUNIV, User NMI	019Ah	No interrupt pending	00h	
		NMIFG	02h	Highest
		OFIFG	04h	
		ACCVIFG	06h	
		Reserved	08h	
		Reserved	0Ah to 1Eh	Lowest

#### **DMA Controller**

The DMA controller allows movement of data from one memory address to another without CPU intervention. For example, the DMA controller can be used to move data from the ADC12\_A conversion memory to RAM. Using the DMA controller can increase the throughput of peripheral modules. The DMA controller reduces system power consumption by allowing the CPU to remain in sleep mode, without having to awaken to move data to or from a peripheral.

TRICCER	CHANNEL			
IRIGGER	0	1	2	
0	DMAREQ	DMAREQ	DMAREQ	
1	TA0CCR0 CCIFG	TA0CCR0 CCIFG	TA0CCR0 CCIFG	
2	TA0CCR2 CCIFG	TA0CCR2 CCIFG	TA0CCR2 CCIFG	
3	TA1CCR0 CCIFG	TA1CCR0 CCIFG	TA1CCR0 CCIFG	
4	TA1CCR2 CCIFG	TA1CCR2 CCIFG	TA1CCR2 CCIFG	
5	TA2CCR0 CCIFG	TA2CCR0 CCIFG	TA2CCR0 CCIFG	
6	TA2CCR2 CCIFG	TA2CCR2 CCIFG	TA2CCR2 CCIFG	
7	TB0CCR0 CCIFG	TB0CCR0 CCIFG	TB0CCR0 CCIFG	
8	TB0CCR2 CCIFG	TB0CCR2 CCIFG	TB0CCR2 CCIFG	
9	Reserved	Reserved	Reserved	
10	Reserved	Reserved	Reserved	
11	Reserved	Reserved	Reserved	
12	Reserved	Reserved	Reserved	
13	Reserved	Reserved	Reserved	
14	Reserved	Reserved	Reserved	
15	Reserved	Reserved	Reserved	
16	UCA0RXIFG	UCA0RXIFG	UCA0RXIFG	
17	UCA0TXIFG	UCA0TXIFG	UCA0TXIFG	
18	UCB0RXIFG	UCBORXIFG	UCBORXIFG	
19	UCB0TXIFG	<b>UCB0TXIFG</b>	UCB0TXIFG	
20	UCA1RXIFG	UCA1RXIFG	UCA1RXIFG	
21	UCA1TXIFG	UCA1TXIFG	UCA1TXIFG	
22	UCB1RXIFG	UCB1RXIFG	UCB1RXIFG	
23	UCB1TXIFG	UCB1TXIFG	UCB1TXIFG	
24	ADC12IFGx	ADC12IFGx	ADC12IFGx	
25	Reserved	Reserved	Reserved	
26	Reserved	Reserved	Reserved	
27	Reserved	Reserved	Reserved	
28	Reserved	Reserved	Reserved	
29	MPY ready	MPY ready	MPY ready	

#### Table 11. DMA Trigger Assignments<sup>(1)</sup>

(1) If a reserved trigger source is selected, no trigger is generated.





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Table 11. DMA Trigger A	Assignments <sup>(1)</sup>	(continued)
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TRICCER		CHANNEL	
IRIGGER	0	1	2
30	DMA2IFG	DMA0IFG	DMA1IFG
31	DMAE0	DMAE0	DMAE0

#### **Universal Serial Communication Interface (USCI)**

The USCI modules are used for serial data communication. The USCI module supports synchronous communication protocols such as SPI (3 or 4 pin) and  $I^2C$ , and asynchronous communication protocols such as UART, enhanced UART with automatic baudrate detection, and IrDA. Each USCI module contains two portions, A and B.

The USCI\_An module provides support for SPI (3 pin or 4 pin), UART, enhanced UART, or IrDA.

The USCI\_Bn module provides support for SPI (3 pin or 4 pin) or  $I^2C$ .

The MSP430F534x series includes two complete USCI modules (n = 0, 1).

#### TA0

TA0 is a 16-bit timer/counter (Timer\_A type) with five capture/compare registers. It can support multiple captures or compares, PWM outputs, and interval timing. It also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

INPUT PIN NUMBER	DEVICE INPUT SIGNAL	MODULE INPUT SIGNAL	MODULE BLOCK	MODULE OUTPUT SIGNAL	DEVICE OUTPUT SIGNAL	OUTPUT PIN NUMBER		
13-P1.0	TA0CLK	TACLK						
	ACLK (internal)	ACLK						
	SMCLK (internal)	SMCLK	Timer	NA	NA			
13-P1.0	TA0CLK	TACLK						
14-P1.1	TA0.0	CCI0A				14-P1.1		
	DV <sub>SS</sub>	CCI0B	CCPO	TAO	TAO 0			
	DV <sub>SS</sub>	GND	CCRU	TAU	140.0			
	DV <sub>CC</sub>	V <sub>CC</sub>						
15-P1.2	TA0.1	CCI1A		TA1			15-P1.2	
	CBOUT (internal)	CCI1B	CCR1		TA0.1	ADC12 (internal) ADC12SHSx = {1}		
	DV <sub>SS</sub>	GND						
	DV <sub>CC</sub>	V <sub>CC</sub>						
16-P1.3	TA0.2	CCI2A				16-P1.3		
	ACLK (internal)	CCI2B	CCP2	TAO	TA2	ТАр	TAO 2	
	DV <sub>SS</sub>	GND		172	170.2			
	DV <sub>CC</sub>	V <sub>CC</sub>						
17-P1.4	TA0.3	CCI3A				17-P1.4		
	DV <sub>SS</sub>	CCI3B	CCP3	TA3	TAO 3			
	DV <sub>SS</sub>	GND	CONS	143	140.5			
	DV <sub>CC</sub>	V <sub>CC</sub>						
18-P1.5	TA0.4	CCI4A				18-P1.5		
	DV <sub>SS</sub>	CCI4B	CCP4	ТАЛ	TAO 4			
	DV <sub>SS</sub>	GND	00114	174	170.4			
	DV <sub>CC</sub>	V <sub>CC</sub>						

#### Table 12. TA0 Signal Connections



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### TA1

TA1 is a 16-bit timer/counter (Timer\_A type) with three capture/compare registers. It can support multiple captures or compares, PWM outputs, and interval timing. It also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

INPUT PIN NUMBER	DEVICE INPUT SIGNAL	MODULE INPUT SIGNAL	MODULE BLOCK	MODULE OUTPUT SIGNAL	DEVICE OUTPUT SIGNAL	OUTPUT PIN NUMBER		
19-P1.6	TA1CLK	TACLK						
	ACLK (internal)	ACLK	Timer	Timer NA	NA			
	SMCLK (internal)	SMCLK	Timer					
19-P1.6	TA1CLK	TACLK						
20-P1.7	TA1.0	CCI0A			TA1.0	20-P1.7		
	DV <sub>SS</sub>	CCI0B	0000	<b>T</b> A0				
	DV <sub>SS</sub>	GND	CCRU	TAU				
	DV <sub>CC</sub>	V <sub>CC</sub>						
Not available	TA1.1	CCI1A				Not available		
	CBOUT (internal)	CCI1B	0001	TA1	TA1	TA1 TA1.1	<b>T</b> 4 4	
	DV <sub>SS</sub>	GND	CCRT				IAI.I	
	DV <sub>CC</sub>	V <sub>CC</sub>						
Not available	TA1.2	CCI2A				Not available		
	ACLK (internal)	CCI2B	CCR2	TAO	TA1.2			
	DV <sub>SS</sub>	GND		TAZ				
	DV <sub>CC</sub>	V <sub>CC</sub>						-

#### **Table 13. TA1 Signal Connections**

#### TA2

TA2 is a 16-bit timer/counter (Timer\_A type) with three capture/compare registers. It can support multiple captures or compares, PWM outputs, and interval timing. It also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

INPUT PIN NUMBER	DEVICE INPUT SIGNAL	MODULE INPUT SIGNAL	MODULE BLOCK	MODULE OUTPUT SIGNAL	DEVICE OUTPUT SIGNAL	OUTPUT PIN NUMBER		
Not available	TA2CLK	TACLK		NA				
	ACLK (internal)	ACLK	Timor					
	SMCLK (internal)	SMCLK	Timer	INA	INA			
Not available	TA2CLK	TACLK						
Not available	TA2.0	CCI0A				Not available		
	DV <sub>SS</sub>	CCI0B	CCBO	TAO	TA2.0			
	DV <sub>SS</sub>	GND	CCRU	TAU	TA2.0			
	DV <sub>CC</sub>	V <sub>CC</sub>						
Not available	TA2.1	CCI1A				Not available		
	CBOUT (internal)	CCI1B	CCP1	ΤΛ1	TAA TAO 4			
	DV <sub>SS</sub>	GND	CCRT	IAT	IAI		TA2.1	
	DV <sub>CC</sub>	V <sub>CC</sub>						
Not available	TA2.2	CCI2A				Not available		
	ACLK (internal)	CCI2B	CCR2	TAO	<b>T</b> AO O			
	DV <sub>SS</sub>	GND		IAZ	1 AZ.Z			
	DV <sub>CC</sub>	V <sub>CC</sub>						

#### Table 14. TA2 Signal Connections





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#### TB0

TB0 is a 16-bit timer/counter (Timer\_B type) with seven capture/compare registers. It can support multiple captures or compares, PWM outputs, and interval timing. It also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

INPUT PIN NUMBER <sup>(1)</sup>	DEVICE INPUT SIGNAL	MODULE INPUT SIGNAL	MODULE BLOCK	MODULE OUTPUT SIGNAL	DEVICE OUTPUT SIGNAL	OUTPUT PIN NUMBER <sup>(1)</sup>
	TB0CLK	TBCLK				
	ACLK (internal)	ACLK				
	SMCLK (internal)	SMCLK	Timer	NA	NA	
	TB0CLK	TBCLK				
	TB0.0	CCI0A				
	TB0.0	CCI0B	CCR0	TB0	TB0.0	ADC12 (internal) ADC12SHSx = {2}
	DV <sub>SS</sub>	GND				
	DV <sub>CC</sub>	V <sub>CC</sub>				
37-P5.7	TB0.1	CCI1A				37-P5.7
	CBOUT (internal)	CCI1B	CCR1	TB1	TB1 TB0.1	ADC12 (internal) ADC12SHSx = {3}
	DV <sub>SS</sub>	GND				
	DV <sub>CC</sub>	V <sub>CC</sub>				
	TB0.2	CCI2A	CCP2	TB2	TB0.2	
	TB0.2	CCI2B				
	DV <sub>SS</sub>	GND	00112			
	DV <sub>CC</sub>	V <sub>CC</sub>				
	TB0.3	CCI3A		ТВЗ	TB0.3	
	TB0.3	CCI3B	CCR3			
	DV <sub>SS</sub>	GND	CONC			
	DV <sub>CC</sub>	V <sub>CC</sub>				
	TB0.4	CCI4A				
	TB0.4	CCI4B	CCR4	TB4	TB0 4	
	DV <sub>SS</sub>	GND	001(4	104	100.4	
	DV <sub>CC</sub>	V <sub>CC</sub>				
	TB0.5	CCI5A				
	TB0.5	CCI5B	CCR5	TB5	TB0 5	
	DV <sub>SS</sub>	GND		100	100.0	
	DV <sub>CC</sub>	V <sub>CC</sub>				
	TB0.6	CCI6A				
	ACLK (internal)	CCI6B	CCR6	TB6	TBO 6	
	DV <sub>SS</sub>	GND	0010	100	100.0	
	DV <sub>CC</sub>	V <sub>CC</sub>				

#### Table 15. TB0 Signal Connections

(1) Timer functions selectable via the port mapping controller.



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#### Comparator\_B

The primary function of the Comparator\_B module is to support precision slope analog-to-digital conversions, battery voltage supervision, and monitoring of external analog signals.

#### ADC12\_A

The ADC12\_A module supports fast, 12-bit analog-to-digital conversions. The module implements a 12-bit SAR core, sample select control, reference generator and a 16 word conversion-and-control buffer. The conversion-and-control buffer allows up to 16 independent ADC samples to be converted and stored without any CPU intervention.

#### CRC16

The CRC16 module produces a signature based on a sequence of entered data values and can be used for data checking purposes. The CRC16 module signature is based on the CRC-CCITT standard.

#### **REF Voltage Reference**

The reference module (REF) is responsible for generation of all critical reference voltages that can be used by the various analog peripherals in the device.

#### **Embedded Emulation Module (EEM)**

The Embedded Emulation Module (EEM) supports real-time in-system debugging. The L version of the EEM implemented on all devices has the following features:

- Eight hardware triggers or breakpoints on memory access
- Two hardware trigger or breakpoint on CPU register write access
- Up to ten hardware triggers can be combined to form complex triggers or breakpoints
- Two cycle counters
- Sequencer
- State storage
- Clock control on module level



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#### Peripheral File Map

MODULE NAME	BASE ADDRESS	OFFSET ADDRESS RANGE
Special Functions (see Table 17)	0100h	000h-01Fh
PMM (see Table 18)	0120h	000h-010h
Flash Control (see Table 19)	0140h	000h-00Fh
CRC16 (see Table 20)	0150h	000h-007h
RAM Control (see Table 21)	0158h	000h-001h
Watchdog (see Table 22)	015Ch	000h-001h
UCS (see Table 23)	0160h	000h-01Fh
SYS (see Table 24)	0180h	000h-01Fh
Shared Reference (see Table 25)	01B0h	000h-001h
Port Mapping Control (see Table 26)	01C0h	000h-002h
Port Mapping Port P4 (see Table 26)	01E0h	000h-007h
Port P1 and P2 (see Table 27)	0200h	000h-01Fh
Port P3 and P4 (see Table 28)	0220h	000h-00Bh
Port P5 and P6 (see Table 29)	0240h	000h-00Bh
Port PJ (see Table 30)	0320h	000h-01Fh
TA0 (see Table 31)	0340h	000h-02Eh
TA1 (see Table 32)	0380h	000h-02Eh
TB0 (see Table 33)	03C0h	000h-02Eh
TA2 (see Table 34)	0400h	000h-02Eh
Real-Time Clock (RTC_A) (see Table 35)	04A0h	000h-01Bh
32-Bit Hardware Multiplier (see Table 36)	04C0h	000h-02Fh
DMA General Control (see Table 37)	0500h	000h-00Fh
DMA Channel 0 (see Table 37)	0510h	000h-00Ah
DMA Channel 1 (see Table 37)	0520h	000h-00Ah
DMA Channel 2 (see Table 37)	0530h	000h-00Ah
USCI_A0 (see Table 38)	05C0h	000h-01Fh
USCI_B0 (see Table 39)	05E0h	000h-01Fh
USCI_A1 (see Table 40)	0600h	000h-01Fh
USCI_B1 (see Table 41)	0620h	000h-01Fh
ADC12_A (see Table 42)	0700h	000h-03Eh
Comparator_B (see Table 43)	08C0h	000h-00Fh

#### Table 16. Peripherals



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Table 17. Special Function Registers (Base Address: 0100h)					
REGISTER DESCRIPTION REGISTER OFFSET					
SFR interrupt enable	SFRIE1	00h			
SFR interrupt flag	SFRIFG1	02h			
SFR reset pin control	SFRRPCR	04h			

#### Table 18. PMM Registers (Base Address: 0120h)

REGISTER DESCRIPTION	REGISTER	OFFSET
PMM Control 0	PMMCTL0	00h
PMM control 1	PMMCTL1	02h
SVS high side control	SVSMHCTL	04h
SVS low side control	SVSMLCTL	06h
PMM interrupt flags	PMMIFG	0Ch
PMM interrupt enable	PMMIE	0Eh
PMM power mode 5 control	PM5CTL0	10h

#### Table 19. Flash Control Registers (Base Address: 0140h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Flash control 1	FCTL1	00h
Flash control 3	FCTL3	04h
Flash control 4	FCTL4	06h

#### Table 20. CRC16 Registers (Base Address: 0150h)

REGISTER DESCRIPTION	REGISTER	OFFSET
CRC data input	CRC16DI	00h
CRC data input reverse byte	CRCDIRB	02h
CRC initialization and result	CRCINIRES	04h
CRC result reverse byte	CRCRESR	06h

#### Table 21. RAM Control Registers (Base Address: 0158h)

REGISTER DESCRIPTION	REGISTER	OFFSET
RAM control 0	RCCTL0	00h

#### Table 22. Watchdog Registers (Base Address: 015Ch)

	•	
REGISTER DESCRIPTION	REGISTER	OFFSET
Watchdog timer control	WDTCTL	00h

#### Table 23. UCS Registers (Base Address: 0160h)

REGISTER DESCRIPTION	REGISTER	OFFSET
UCS control 0	UCSCTL0	00h
UCS control 1	UCSCTL1	02h
UCS control 2	UCSCTL2	04h
UCS control 3	UCSCTL3	06h
UCS control 4	UCSCTL4	08h
UCS control 5	UCSCTL5	0Ah
UCS control 6	UCSCTL6	0Ch
UCS control 7	UCSCTL7	0Eh
UCS control 8	UCSCTL8	10h

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Table 24. SYS Registers (Base Address: 0180h)		
REGISTER DESCRIPTION	REGISTER	OFFSET
System control	SYSCTL	00h
Bootstrap loader configuration area	SYSBSLC	02h
JTAG mailbox control	SYSJMBC	06h
JTAG mailbox input 0	SYSJMBI0	08h
JTAG mailbox input 1	SYSJMBI1	0Ah
JTAG mailbox output 0	SYSJMBO0	0Ch
JTAG mailbox output 1	SYSJMBO1	0Eh
Bus Error vector generator	SYSBERRIV	18h
User NMI vector generator	SYSUNIV	1Ah
System NMI vector generator	SYSSNIV	1Ch
Reset vector generator	SYSRSTIV	1Eh

Table 25. Shared Reference Registers (Base Address: 01B0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Shared reference control	REFCTL	00h

# Table 26. Port Mapping Registers (Base Address of Port Mapping Control: 01C0h, Port P4: 01E0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Port mapping key/ID register	PMAPKEYID	00h
Port mapping control register	PMAPCTL	02h
Port P4.0 mapping register	P4MAP0	00h
Port P4.1 mapping register	P4MAP1	01h
Port P4.2 mapping register	P4MAP2	02h
Port P4.3 mapping register	P4MAP3	03h
Port P4.4 mapping register	P4MAP4	04h
Port P4.5 mapping register	P4MAP5	05h
Port P4.6 mapping register	P4MAP6	06h
Port P4.7 mapping register	P4MAP7	07h



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Table 27. Port P1 and P2 Registers (Base Address: 0200h)		
REGISTER DESCRIPTION	REGISTER	OFFSET
Port P1 input	P1IN	00h
Port P1 output	P1OUT	02h
Port P1 direction	P1DIR	04h
Port P1 pullup/pulldown enable	P1REN	06h
Port P1 drive strength	P1DS	08h
Port P1 selection	P1SEL	0Ah
Port P1 interrupt vector word	P1IV	0Eh
Port P1 interrupt edge select	P1IES	18h
Port P1 interrupt enable	P1IE	1Ah
Port P1 interrupt flag	P1IFG	1Ch
Port P2 input	P2IN	01h
Port P2 output	P2OUT	03h
Port P2 direction	P2DIR	05h
Port P2 pullup/pulldown enable	P2REN	07h
Port P2 drive strength	P2DS	09h
Port P2 selection	P2SEL	0Bh
Port P2 interrupt vector word	P2IV	1Eh
Port P2 interrupt edge select	P2IES	19h
Port P2 interrupt enable	P2IE	1Bh
Port P2 interrupt flag	P2IFG	1Dh

#### Table 28. Port P3 and P4 Registers (Base Address: 0220h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Port P3 input	P3IN	00h
Port P3 output	P3OUT	02h
Port P3 direction	P3DIR	04h
Port P3 pullup/pulldown enable	P3REN	06h
Port P3 drive strength	P3DS	08h
Port P3 selection	P3SEL	0Ah
Port P4 input	P4IN	01h
Port P4 output	P4OUT	03h
Port P4 direction	P4DIR	05h
Port P4 pullup/pulldown enable	P4REN	07h
Port P4 drive strength	P4DS	09h
Port P4 selection	P4SEL	0Bh



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Table 29. Port P5 and P6 Registers (Base Address: 0240h)		
REGISTER DESCRIPTION	REGISTER	OFFSET
Port P5 input	P5IN	00h
Port P5 output	P5OUT	02h
Port P5 direction	P5DIR	04h
Port P5 pullup/pulldown enable	P5REN	06h
Port P5 drive strength	P5DS	08h
Port P5 selection	P5SEL	0Ah
Port P6 input	P6IN	01h
Port P6 output	P6OUT	03h
Port P6 direction	P6DIR	05h
Port P6 pullup/pulldown enable	P6REN	07h
Port P6 drive strength	P6DS	09h
Port P6 selection	P6SEL	0Bh

Table 30. Port J Registers (Base Address: 0320h)		
REGISTER DESCRIPTION	REGISTER	OFFSET
Port PJ input	PJIN	00h
Port PJ output	PJOUT	02h
Port PJ direction	PJDIR	04h
Port PJ pullup/pulldown enable	PJREN	06h
Port PJ drive strength	PJDS	08h

Table 31. TA0 Registers	(Base Address: 0340h)
-------------------------	-----------------------

REGISTER DESCRIPTION	REGISTER	OFFSET
TA0 control	TA0CTL	00h
Capture/compare control 0	TA0CCTL0	02h
Capture/compare control 1	TA0CCTL1	04h
Capture/compare control 2	TA0CCTL2	06h
Capture/compare control 3	TA0CCTL3	08h
Capture/compare control 4	TA0CCTL4	0Ah
TA0 counter register	TAOR	10h
Capture/compare register 0	TA0CCR0	12h
Capture/compare register 1	TA0CCR1	14h
Capture/compare register 2	TA0CCR2	16h
Capture/compare register 3	TA0CCR3	18h
Capture/compare register 4	TA0CCR4	1Ah
TA0 expansion register 0	TA0EX0	20h
TA0 interrupt vector	TAOIV	2Eh



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Table 32. TA1 Registers (Base Address: 0380h)		
REGISTER DESCRIPTION	REGISTER	OFFSET
TA1 control	TA1CTL	00h
Capture/compare control 0	TA1CCTL0	02h
Capture/compare control 1	TA1CCTL1	04h
Capture/compare control 2	TA1CCTL2	06h
TA1 counter register	TA1R	10h
Capture/compare register 0	TA1CCR0	12h
Capture/compare register 1	TA1CCR1	14h
Capture/compare register 2	TA1CCR2	16h
TA1 expansion register 0	TA1EX0	20h
TA1 interrupt vector	TA1IV	2Eh

#### Table 33. TB0 Registers (Base Address: 03C0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
TB0 control	TB0CTL	00h
Capture/compare control 0	TB0CCTL0	02h
Capture/compare control 1	TB0CCTL1	04h
Capture/compare control 2	TB0CCTL2	06h
Capture/compare control 3	TB0CCTL3	08h
Capture/compare control 4	TB0CCTL4	0Ah
Capture/compare control 5	TB0CCTL5	0Ch
Capture/compare control 6	TB0CCTL6	0Eh
TB0 register	TB0R	10h
Capture/compare register 0	TB0CCR0	12h
Capture/compare register 1	TB0CCR1	14h
Capture/compare register 2	TB0CCR2	16h
Capture/compare register 3	TB0CCR3	18h
Capture/compare register 4	TB0CCR4	1Ah
Capture/compare register 5	TB0CCR5	1Ch
Capture/compare register 6	TB0CCR6	1Eh
TB0 expansion register 0	TB0EX0	20h
TB0 interrupt vector	TB0IV	2Eh

#### Table 34. TA2 Registers (Base Address: 0400h)

REGISTER DESCRIPTION	REGISTER	OFFSET
TA2 control	TA2CTL	00h
Capture/compare control 0	TA2CCTL0	02h
Capture/compare control 1	TA2CCTL1	04h
Capture/compare control 2	TA2CCTL2	06h
TA2 counter register	TA2R	10h
Capture/compare register 0	TA2CCR0	12h
Capture/compare register 1	TA2CCR1	14h
Capture/compare register 2	TA2CCR2	16h
TA2 expansion register 0	TA2EX0	20h
TA2 interrupt vector	TA2IV	2Eh

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Table 35. Real-Time Clock Registers (Base Address: 04A0h)		
REGISTER DESCRIPTION	REGISTER	OFFSET
RTC control 0	RTCCTL0	00h
RTC control 1	RTCCTL1	01h
RTC control 2	RTCCTL2	02h
RTC control 3	RTCCTL3	03h
RTC prescaler 0 control	RTCPS0CTL	08h
RTC prescaler 1 control	RTCPS1CTL	0Ah
RTC prescaler 0	RTCPS0	0Ch
RTC prescaler 1	RTCPS1	0Dh
RTC interrupt vector word	RTCIV	0Eh
RTC seconds, RTC counter register 1	RTCSEC, RTCNT1	10h
RTC minutes, RTC counter register 2	RTCMIN, RTCNT2	11h
RTC hours, RTC counter register 3	RTCHOUR, RTCNT3	12h
RTC day of week, RTC counter register 4	RTCDOW, RTCNT4	13h
RTC days	RTCDAY	14h
RTC month	RTCMON	15h
RTC year low	RTCYEARL	16h
RTC year high	RTCYEARH	17h
RTC alarm minutes	RTCAMIN	18h
RTC alarm hours	RTCAHOUR	19h
RTC alarm day of week	RTCADOW	1Ah
RTC alarm days	RTCADAY	1Bh



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Table 36. 32-Bit Hardware Multiplier Registers (Base Address: 04C0h)		
REGISTER DESCRIPTION	REGISTER	OFFSET
16-bit operand 1 – multiply	MPY	00h
16-bit operand 1 – signed multiply	MPYS	02h
16-bit operand 1 – multiply accumulate	MAC	04h
16-bit operand 1 – signed multiply accumulate	MACS	06h
16-bit operand 2	OP2	08h
16 × 16 result low word	RESLO	0Ah
16 × 16 result high word	RESHI	0Ch
16 x 16 sum extension register	SUMEXT	0Eh
32-bit operand 1 – multiply low word	MPY32L	10h
32-bit operand 1 – multiply high word	MPY32H	12h
32-bit operand 1 – signed multiply low word	MPYS32L	14h
32-bit operand 1 – signed multiply high word	MPYS32H	16h
32-bit operand 1 – multiply accumulate low word	MAC32L	18h
32-bit operand 1 – multiply accumulate high word	MAC32H	1Ah
32-bit operand 1 - signed multiply accumulate low word	MACS32L	1Ch
32-bit operand 1 - signed multiply accumulate high word	MACS32H	1Eh
32-bit operand 2 – low word	OP2L	20h
32-bit operand 2 – high word	OP2H	22h
32 × 32 result 0 – least significant word	RES0	24h
32 × 32 result 1	RES1	26h
32 × 32 result 2	RES2	28h
32 × 32 result 3 – most significant word	RES3	2Ah
MPY32 control register 0	MPY32CTL0	2Ch





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# Table 37. DMA Registers (Base Address DMA General Control: 0500h, DMA Channel 0: 0510h, DMA Channel 1: 0520h, DMA Channel 2: 0530h)

REGISTER DESCRIPTION	REGISTER	OFFSET
DMA channel 0 control	DMA0CTL	00h
DMA channel 0 source address low	DMA0SAL	02h
DMA channel 0 source address high	DMA0SAH	04h
DMA channel 0 destination address low	DMA0DAL	06h
DMA channel 0 destination address high	DMA0DAH	08h
DMA channel 0 transfer size	DMA0SZ	0Ah
DMA channel 1 control	DMA1CTL	00h
DMA channel 1 source address low	DMA1SAL	02h
DMA channel 1 source address high	DMA1SAH	04h
DMA channel 1 destination address low	DMA1DAL	06h
DMA channel 1 destination address high	DMA1DAH	08h
DMA channel 1 transfer size	DMA1SZ	0Ah
DMA channel 2 control	DMA2CTL	00h
DMA channel 2 source address low	DMA2SAL	02h
DMA channel 2 source address high	DMA2SAH	04h
DMA channel 2 destination address low	DMA2DAL	06h
DMA channel 2 destination address high	DMA2DAH	08h
DMA channel 2 transfer size	DMA2SZ	0Ah
DMA module control 0	DMACTL0	00h
DMA module control 1	DMACTL1	02h
DMA module control 2	DMACTL2	04h
DMA module control 3	DMACTL3	06h
DMA module control 4	DMACTL4	08h
DMA interrupt vector	DMAIV	0Eh

#### Table 38. USCI\_A0 Registers (Base Address: 05C0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
USCI control 1	UCA0CTL1	00h
USCI control 0	UCA0CTL0	01h
USCI baud rate 0	UCA0BR0	06h
USCI baud rate 1	UCA0BR1	07h
USCI modulation control	UCA0MCTL	08h
USCI status	UCA0STAT	0Ah
USCI receive buffer	UCA0RXBUF	0Ch
USCI transmit buffer	UCA0TXBUF	0Eh
USCI LIN control	UCA0ABCTL	10h
USCI IrDA transmit control	UCA0IRTCTL	12h
USCI IrDA receive control	UCA0IRRCTL	13h
USCI interrupt enable	UCA0IE	1Ch
USCI interrupt flags	UCA0IFG	1Dh
USCI interrupt vector word	UCA0IV	1Eh



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Table 39. USCI_B0 Registers (Base Address: 05E0h)		
REGISTER DESCRIPTION	REGISTER	OFFSET
USCI synchronous control 1	UCB0CTL1	00h
USCI synchronous control 0	UCB0CTL0	01h
USCI synchronous bit rate 0	UCB0BR0	06h
USCI synchronous bit rate 1	UCB0BR1	07h
USCI synchronous status	UCB0STAT	0Ah
USCI synchronous receive buffer	UCBORXBUF	0Ch
USCI synchronous transmit buffer	UCB0TXBUF	0Eh
USCI I2C own address	UCB0I2COA	10h
USCI I2C slave address	UCB0I2CSA	12h
USCI interrupt enable	UCB0IE	1Ch
USCI interrupt flags	UCB0IFG	1Dh
USCI interrupt vector word	UCB0IV	1Eh

#### Table 40. USCI\_A1 Registers (Base Address: 0600h)

REGISTER DESCRIPTION	REGISTER	OFFSET
USCI control 1	UCA1CTL1	00h
USCI control 0	UCA1CTL0	01h
USCI baud rate 0	UCA1BR0	06h
USCI baud rate 1	UCA1BR1	07h
USCI modulation control	UCA1MCTL	08h
USCI status	UCA1STAT	0Ah
USCI receive buffer	UCA1RXBUF	0Ch
USCI transmit buffer	UCA1TXBUF	0Eh
USCI LIN control	UCA1ABCTL	10h
USCI IrDA transmit control	UCA1IRTCTL	12h
USCI IrDA receive control	UCA1IRRCTL	13h
USCI interrupt enable	UCA1IE	1Ch
USCI interrupt flags	UCA1IFG	1Dh
USCI interrupt vector word	UCA1IV	1Eh

#### Table 41. USCI\_B1 Registers (Base Address: 0620h)

REGISTER DESCRIPTION	REGISTER	OFFSET
USCI synchronous control 1	UCB1CTL1	00h
USCI synchronous control 0	UCB1CTL0	01h
USCI synchronous bit rate 0	UCB1BR0	06h
USCI synchronous bit rate 1	UCB1BR1	07h
USCI synchronous status	UCB1STAT	0Ah
USCI synchronous receive buffer	UCB1RXBUF	0Ch
USCI synchronous transmit buffer	UCB1TXBUF	0Eh
USCI I2C own address	UCB1I2COA	10h
USCI I2C slave address	UCB1I2CSA	12h
USCI interrupt enable	UCB1IE	1Ch
USCI interrupt flags	UCB1IFG	1Dh
USCI interrupt vector word	UCB1IV	1Eh

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		055057
REGISTER DESCRIPTION	REGISTER	OFFSET
Control register 0	ADC12CTL0	00h
Control register 1	ADC12CTL1	02h
Control register 2	ADC12CTL2	04h
Interrupt-flag register	ADC12IFG	0Ah
Interrupt-enable register	ADC12IE	0Ch
Interrupt-vector-word register	ADC12IV	0Eh
ADC memory-control register 0	ADC12MCTL0	10h
ADC memory-control register 1	ADC12MCTL1	11h
ADC memory-control register 2	ADC12MCTL2	12h
ADC memory-control register 3	ADC12MCTL3	13h
ADC memory-control register 4	ADC12MCTL4	14h
ADC memory-control register 5	ADC12MCTL5	15h
ADC memory-control register 6	ADC12MCTL6	16h
ADC memory-control register 7	ADC12MCTL7	17h
ADC memory-control register 8	ADC12MCTL8	18h
ADC memory-control register 9	ADC12MCTL9	19h
ADC memory-control register 10	ADC12MCTL10	1Ah
ADC memory-control register 11	ADC12MCTL11	1Bh
ADC memory-control register 12	ADC12MCTL12	1Ch
ADC memory-control register 13	ADC12MCTL13	1Dh
ADC memory-control register 14	ADC12MCTL14	1Eh
ADC memory-control register 15	ADC12MCTL15	1Fh
Conversion memory 0	ADC12MEM0	20h
Conversion memory 1	ADC12MEM1	22h
Conversion memory 2	ADC12MEM2	24h
Conversion memory 3	ADC12MEM3	26h
Conversion memory 4	ADC12MEM4	28h
Conversion memory 5	ADC12MEM5	2Ah
Conversion memory 6	ADC12MEM6	2Ch
Conversion memory 7	ADC12MEM7	2Eh
Conversion memory 8	ADC12MEM8	30h
Conversion memory 9	ADC12MEM9	32h
Conversion memory 10	ADC12MEM10	34h
Conversion memory 11	ADC12MEM11	36h
Conversion memory 12	ADC12MEM12	38h
Conversion memory 13	ADC12MEM13	3Ah
Conversion memory 14	ADC12MEM14	3Ch
Conversion memory 15	ADC12MEM15	3Eh



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Table 43. Comparator_B Registers (Base Address: 08C0h)		
REGISTER DESCRIPTION	REGISTER	OFFSET
Comp_B control register 0	CBCTL0	00h
Comp_B control register 1	CBCTL1	02h
Comp_B control register 2	CBCTL2	04h
Comp_B control register 3	CBCTL3	06h
Comp_B interrupt register	CBINT	0Ch
Comp_B interrupt vector word	CBIV	0Eh




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# Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

Voltage applied at $V_{CC}$ to $V_{SS}$	-0.3 V to 4.1 V
Voltage applied to any pin (excluding VCORE) <sup>(2)</sup>	-0.3 V to V <sub>CC</sub> + 0.3 V
Diode current at any device pin	±2 mA
Storage temperature range, T <sub>stg</sub> <sup>(3)</sup>	-55°C to 150°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltages referenced to  $V_{SS}$ . VCORE is for internal device usage only. No external DC loading or voltage should be applied. Higher temperature may be applied during board soldering according to the current JEDEC J-STD-020 specification with peak reflow

(2) (3)

temperatures not higher than classified on the device label on the shipping boxes or reels.

#### **Thermal Packaging Characteristics**

$\theta_{JA}$	Junction-to-ambient thermal resistance, still air	High-K board (JESD51-7)	VQFN (RGZ)	27.8	°C/W
$\theta_{\text{JC}}$	Junction-to-case thermal resistance		VQFN (RGZ)	13.6	°C/W
$\theta_{JB}$	Junction-to-board thermal resistance		VQFN (RGZ)	4.7	°C/W



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#### **Recommended Operating Conditions**

Typical values are specified at  $V_{CC}$  = 3.3 V and  $T_A$  = 25°C (unless otherwise noted)

			MIN	NOM	MAX	UNIT
		PMMCOREVx = 0	1.8		3.6	V
V	Supply voltage during program execution and flash	PMMCOREVx = 0, 1	2.0		3.6	V
VCC	programming (AVCCx = DVCCx = $V_{CC}$ ) <sup>(1)(2)</sup>	PMMCOREVx = 0, 1, 2	2.2		3.6	٧
		PMMCOREVx = 0, 1, 2, 3	2.4		3.6	V
V <sub>SS</sub>	Supply voltage (AVSSx = DVSSx = V <sub>SS</sub> )			0		V
T <sub>A</sub>	Operating free-air temperature		-40		85	°C
TJ	Operating junction temperature		-40		85	°C
C <sub>VCORE</sub>	Recommended capacitor at VCORE			470		nF
C <sub>DVCC</sub> / C <sub>VCORE</sub>	Capacitor ratio of DVCC to VCORE		10			
		$\begin{array}{l} PMMCOREVx = 0, \\ 1.8 \ V \leq V_{CC} \leq 3.6 \ V \\ (\text{default condition}) \end{array}$	0		8.0	
<b>f</b> SYSTEM	Processor frequency (maximum MCLK frequency) <sup>(3)</sup>	$\begin{array}{l} PMMCOREVx = 1, \\ 2.0 V \leq V_{CC} \leq 3.6 \ V \end{array}$	0		12.0	MHz
	(see Figure 2)	$\begin{array}{l} PMMCOREVx = 2, \\ 2.2 \ V \leq V_{CC} \leq 3.6 \ V \end{array}$	0		20.0	
		PMMCOREVx = 3, 2.4 V $\leq$ V <sub>CC</sub> $\leq$ 3.6 V	0		25.0	

(1) It is recommended to power AVCC and DVCC from the same source. A maximum difference of 0.3 V between AVCC and DVCC can be tolerated during power up and operation.

(2) The minimum supply voltage is defined by the supervisor SVS levels when it is enabled. See the PMM, SVS High Side threshold parameters for the exact values and further details.

(3) Modules may have a different maximum input clock specification. See the specification of the respective module in this data sheet.



The numbers within the fields denote the supported PMMCOREVx settings.

Figure 2. Maximum System Frequency

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# **Electrical Characteristics**

# Active Mode Supply Current Into V<sub>cc</sub> Excluding External Current

over recommended operating free-air temperature (unless otherwise noted)<sup>(1) (2) (3)</sup>

						FRE		CY (f <sub>DC</sub>	о = f <sub>MCI</sub>	_k = f <sub>SN</sub>	ICLK)								
PARAMETER	MEMORY	MEMORY	MEMORY	V <sub>cc</sub>	PMMCOREVx	1 N	١Hz	8 N	/Hz	12 MH:		12 MHz 🔅		20	20 MHz		25 MHz		
									TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
1			0	0.36	0.47	2.32	2.60												
	L Eloob	Flash	Floop	2.1/	1	0.40		2.65		4.0	4.4								
AM, Flash	Flash		3 V	2	0.44		2.90		4.3		7.1	7.7			mA				
			3	0.46		3.10		4.6		7.6		10.1	11.0						
			0	0.20	0.24	1.20	1.30												
	DAM	2.1/	1	0.22		1.35		2.0	2.2										
I <sub>AM,</sub> RAM	RAM	3 V	2	0.24		1.50		2.2		3.7	4.2			mA					
			3	0.26		1.60		2.4		3.9		5.3	6.2						

(1)

All inputs are tied to 0 V or to V<sub>CC</sub>. Outputs do not source or sink any current. The currents are characterized with a Micro Crystal MS1V-T1K crystal with a load capacitance of 12.5 pF. The internal and external load (2) capacitance are chosen to closely match the required 12.5 pF.

Characterized with program executing typical data processing. (3)  $f_{ACLK} = 32786 \ \text{Hz}, \ f_{DCO} = f_{MCLK} = f_{SMCLK} \ \text{at specified frequency}. \\ XTS = CPUOFF = SCG0 = SCG1 = OSCOFF = SMCLKOFF = 0.$ 



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# Low-Power Mode Supply Currents (Into V<sub>cc</sub>) Excluding External Current

	interfueu ranges or suppr	y voltay	e and operating	nee-an	tempe					u)		
	PARAMETER	Vcc	PMMCOREVx	-40	°C	25	°C	60	°C	85	°C	UNIT
				TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	•••••
	Low power mode $O^{(3)}$ (4)	2.2 V	0	73		77	85	80		85	97	
LPM0,1MHz	Low-power mode 0	3 V	3	79		83	92	88		95	105	μΑ
L	Low power mode $2^{(5)}$ (4)	2.2 V	0	6.5		6.5	12	10		11	17	
'LPM2		3 V	3	7.0		7.0	13	11		12	18	μΑ
			0	1.60		1.90		2.6		5.6		
		2.2 V	1	1.65		2.00		2.7		5.9		
	Low-power mode 3, crystal mode <sup>(6) (4)</sup>		2	1.75		2.15		2.9		6.1		
I <sub>LPM3,XT1LF</sub>		3 V	0	1.8		2.1	2.9	2.8		5.8	8.3	μA
			1	1.9		2.3		2.9		6.1		
			2	2.0		2.4		3.0		6.3		
			3	2.0		2.5	3.9	3.1		6.4	9.3	
			0	1.1		1.4	2.7	1.9		4.9	7.4	
	Low-power mode 3,	2.1/	1	1.1		1.4		2.0		5.2		
LPM3,VLO	VLO mode <sup>(7) (4)</sup>	3 V	2	1.2		1.5		2.1		5.3		μΑ
			3	1.3		1.6	3.0	2.2		5.4	8.5	
			0	0.9		1.1	1.5	1.8		4.8	7.3	
	4 (8) (4)	2.14	1	1.1		1.2		2.0		5.1		
ILPM4	Low-power mode 4	3 V	2	1.2		1.2		2.1		5.2		μA
			3	1.3		1.3	1.6	2.2		5.3	8.1	
I <sub>LPM4.5</sub>	Low-power mode 4.5 <sup>(9)</sup>	3 V		0.15		0.18	0.35	0.26		0.5	1.0	μA

(1) All inputs are tied to 0 V or to  $V_{CC}$ . Outputs do not source or sink any current.

(2) The currents are characterized with a Micro Crystal MS1V-T1K crystal with a load capacitance of 12.5 pF. The internal and external load capacitance are chosen to closely match the required 12.5 pF.

(3) Current for watchdog timer clocked by SMCLK included. ACLK = low frequency crystal operation (XTS = 0, XT1DRIVEx = 0).

CPUOFF = 1, SCG0 = 0, SCG1 = 0, OSCOFF = 0 (LPM0); f<sub>ACLK</sub> = 32768 Hz, f<sub>MCLK</sub> = 0 MHz, f<sub>SMCLK</sub> = f<sub>DC0</sub> = 1 MHz
(4) Current for brownout, high side supervisor (SVS<sub>H</sub>) normal mode included. Low-side supervisor and monitors disabled (SVS<sub>L</sub>, SVM<sub>L</sub>). High-side monitor disabled (SVM<sub>H</sub>). RAM retention enabled.

(5) Current for watchdog timer and RTC clocked by ACLK included. ACLK = low frequency crystal operation (XTS = 0, XT1DRIVEx = 0). CPUOFF = 1, SCG0 = 0, SCG1 = 1, OSCOFF = 0 (LPM2); f<sub>ACLK</sub> = 32768 Hz, f<sub>MCLK</sub> = 0 MHz, f<sub>SMCLK</sub> = f<sub>DC0</sub> = 0 MHz; DCO setting = 1 MHz operation, DCO bias generator enabled.)

(6) Current for watchdog timer and RTC clocked by ACLK included. ACLK = low frequency crystal operation (XTS = 0, XT1DRIVEx = 0). CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0 (LPM3); f<sub>ACLK</sub> = 32768 Hz, f<sub>MCLK</sub> = f<sub>SMCLK</sub> = f<sub>DCO</sub> = 0 MHz

(7) Current for watchdog timer and RTC clocked by ACLK included. ACLK = VLO.

 $CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0 (LPM3); f_{ACLK} = f_{VLO}, f_{MCLK} = f_{SMCLK} = f_{DCO} = 0 MHz$ 

(8) CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 1 (LPM4);  $f_{DC0} = f_{ACLK} = f_{MCLK} = 0$  MHz

(9) Internal regulator disabled. No data retention.

CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 1, PMMREGOFF = 1 (LPM4.5);  $f_{DCO} = f_{ACLK} = f_{MCLK} = f_{SMCLK} = 0$  MHz





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#### Schmitt-Trigger Inputs – General Purpose I/O<sup>(1)</sup> (P1.0 to P1.7, P2.7, P3.0 to P3.4, P4.0 to P4.7) (P5.0 to P5.5, P5.7, P6.1 to P6.5, PJ.0 to PJ.3, RST/NMI)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	V <sub>cc</sub>	MIN	TYP	MAX	UNIT
V	Depitive going input threshold voltage		1.8 V	0.80		1.40	V
VIT+	Positive-going input threshold voltage		3 V	1.50		2.10	v
V	Negative going input throughold voltage		1.8 V	0.45		1.00	V
VIT-	negative-going input threshold voltage		3 V	0.75		1.65	v
V			1.8 V	0.3		0.8	V
v <sub>hys</sub>	Input voltage hysteresis ( $v_{\text{IT+}} - v_{\text{IT-}}$ )		3 V	0.4		1.0	v
R <sub>Pull</sub>	Pullup/pulldown resistor <sup>(2)</sup>	For pullup: $V_{IN} = V_{SS}$ For pulldown: $V_{IN} = V_{CC}$		20	35	50	kΩ
CI	Input capacitance	$V_{IN} = V_{SS}$ or $V_{CC}$			5		pF

(1) Same parametrics apply to clock input pin when crystal bypass mode is used on XT1 (XIN) or XT2 (XT2IN).

(2) Also applies to RST pin when pullup or pulldown resistor is enabled.

#### Inputs – Ports P1 and P2<sup>(1)</sup> (P1.0 to P1.7, P2.0 to P2.7)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V <sub>cc</sub>	MIN	MAX	UNIT
t <sub>(int)</sub>	External interrupt timing <sup>(2)</sup>	External trigger pulse width to set interrupt flag	2.2 V, 3 V	20		ns

(1) Some devices may contain additional ports with interrupts. See the block diagram and terminal function descriptions.

(2) An external signal sets the interrupt flag every time the minimum interrupt pulse duration t<sub>(int)</sub> is met. It may be set by trigger signals shorter than t<sub>(int)</sub>.

#### Leakage Current – General Purpose I/O (P1.0 to P1.7, P2.7, P3.0 to P3.4, P4.0 to P4.7) (P5.0 to P5.5, P5.7, P6.1 to P6.5, PJ.0 to PJ.3, RST/NMI)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAME	TER	TEST CONDITIONS	Vcc	MIN MAX	UNIT
I <sub>Ikg(Px.x)</sub> High-impedance leaka	age current	(1) (2)	1.8 V, 3 V	±50	nA

(1) The leakage current is measured with  $V_{SS}$  or  $V_{CC}$  applied to the corresponding pin(s), unless otherwise noted.

(2) The leakage of the digital port pins is measured individually. The port pin is selected for input and the pullup/pulldown resistor is disabled.



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#### Outputs – General Purpose I/O (Full Drive Strength) (P1.0 to P1.7, P2.7, P3.0 to P3.4, P4.0 to P4.7) (P5.0 to P5.5, P5.7, P6.1 to P6.5, PJ.0 to PJ.3)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	Vcc	MIN	MAX	UNIT
	High-level output voltage	$I_{(OHmax)} = -3 \text{ mA}^{(1)}$	1 9 \/	$V_{CC} - 0.25$	V <sub>CC</sub>	
V <sub>OH</sub>		$I_{(OHmax)} = -10 \text{ mA}^{(2)}$	1.0 V	V <sub>CC</sub> – 0.60	V <sub>CC</sub>	v
		$I_{(OHmax)} = -5 \text{ mA}^{(1)}$	2.1/	V <sub>CC</sub> - 0.25	V <sub>CC</sub>	v
		$I_{(OHmax)} = -15 \text{ mA}^{(2)}$	3 V	V <sub>CC</sub> - 0.60	V <sub>CC</sub>	
		$I_{(OLmax)} = 3 \text{ mA}^{(1)}$	4.0.1/	V <sub>SS</sub>	$V_{SS} + 0.25$	V
V		$I_{(OLmax)} = 10 \text{ mA}^{(2)}$	1.0 V	V <sub>SS</sub>	$V_{SS} + 0.60$	
V <sub>OL</sub>	Low-level output voltage	$I_{(OLmax)} = 5 \text{ mA}^{(1)}$	2.1/	V <sub>SS</sub>	V <sub>SS</sub> + 0.25	
		$I_{(OLmax)} = 15 \text{ mA}^{(2)}$	3 V	V <sub>SS</sub>	$V_{SS} + 0.60$	

(1) The maximum total current, I<sub>(OHmax)</sub> and I<sub>(OLmax)</sub>, for all outputs combined should not exceed ±48 mA to hold the maximum voltage drop specified.

(2) The maximum total current, I<sub>(OHmax)</sub> and I<sub>(OLmax)</sub>, for all outputs combined should not exceed ±100 mA to hold the maximum voltage drop specified.

#### Outputs – General Purpose I/O (Reduced Drive Strength) (P1.0 to P1.7, P2.7, P3.0 to P3.4, P4.0 to P4.7) (P5.0 to P5.5, P5.7, P6.1 to P6.5, PJ.0 to PJ.3)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)<sup>(1)</sup>

	PARAMETER	TEST CONDITIONS	V <sub>cc</sub>	MIN	MAX	UNIT
V <sub>OH</sub>		$I_{(OHmax)} = -1 \text{ mA}^{(2)}$	1 0 \/	$V_{CC} - 0.25$	V <sub>CC</sub>	
	High lovel output voltage	$I_{(OHmax)} = -3 \text{ mA}^{(3)}$	1.0 V	$V_{CC} - 0.60$	V <sub>CC</sub>	V
	High-level output voltage	$I_{(OHmax)} = -2 \text{ mA}^{(2)}$	3.\/	V <sub>CC</sub> – 0.25	V <sub>CC</sub>	
		$I_{(OHmax)} = -6 \text{ mA}^{(3)}$	3 V	V <sub>CC</sub> - 0.60	V <sub>CC</sub>	
		$I_{(OLmax)} = 1 \text{ mA}^{(2)}$	4.0.1/	V <sub>SS</sub>	$V_{SS} + 0.25$	- V
V		$I_{(OLmax)} = 3 \text{ mA}^{(3)}$	1.0 V	V <sub>SS</sub>	$V_{SS} + 0.60$	
V <sub>OL</sub>	Low-level output voltage	$I_{(OLmax)} = 2 \text{ mA}^{(2)}$	2.14	V <sub>SS</sub>	V <sub>SS</sub> + 0.25	
		$I_{(OLmax)} = 6 \text{ mA}^{(3)}$	3 V	V <sub>SS</sub>	$V_{SS} + 0.60$	

(1) Selecting reduced drive strength may reduce EMI.

(2) The maximum total current, I<sub>(OHmax)</sub> and I<sub>(OLmax)</sub>, for all outputs combined, should not exceed ±48 mA to hold the maximum voltage drop specified.

(3) The maximum total current, I<sub>(OHmax)</sub> and I<sub>(OLmax)</sub>, for all outputs combined, should not exceed ±100 mA to hold the maximum voltage drop specified.

#### Output Frequency – General Purpose I/O (P1.0 to P1.7, P2.7, P3.0 to P3.4, P4.0 to P4.7) (P5.0 to P5.5, P5.7, P6.1 to P6.5, PJ.0 to PJ.3)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MAX	UNIT
£	Port output frequency (with load)	(1) (2)	$V_{CC} = 1.8 V$ , PMMCOREVx = 0		16	M⊔⇒
T <sub>Px.y</sub>		(., (_)	$V_{CC} = 3 V$ , PMMCOREVx = 3		25	IVITZ
	Clock output frequency	ACLK,	$V_{CC} = 1.8 V$ , PMMCOREVx = 0		16	
f <sub>Port_CLK</sub>		SMCLK, MCLK , $C_L = 20 \text{ pF}^{(2)}$	V <sub>CC</sub> = 3 V, PMMCOREVx = 3		25	MHz

(1) A resistive divider with  $2 \times R1$  between V<sub>CC</sub> and V<sub>SS</sub> is used as load. The output is connected to the center tap of the divider. For full drive strength, R1 = 550  $\Omega$ . For reduced drive strength, R1 = 1.6 k $\Omega$ . C<sub>L</sub> = 20 pF is connected to the output to V<sub>SS</sub>.

(2) The output voltage reaches at least 10% and 90% V<sub>CC</sub> at the specified toggle frequency.

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# Crystal Oscillator, XT1, Low-Frequency Mode<sup>(1)</sup>

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	V <sub>cc</sub>	MIN	ΤΥΡ Ι	MAX	UNIT
		$f_{OSC} = 32768$ Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVEx = 1, T <sub>A</sub> = 25°C		0	.075		
$\Delta I_{DVCC.LF}$	Differential XT1 oscillator crystal current consumption from lowest drive setting, LF mode	$f_{OSC} = 32768$ Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVEx = 2, $T_A = 25^{\circ}C$	3 V	0	.170		μA
		$\label{eq:fosc} \begin{array}{l} f_{OSC} = 32768 \text{ Hz}, \text{ XTS} = 0, \\ \text{XT1BYPASS} = 0, \text{ XT1DRIVEx} = 3, \\ \text{T}_{\text{A}} = 25^{\circ}\text{C} \end{array}$	-	0	.290		
f <sub>XT1,LF0</sub>	XT1 oscillator crystal frequency, LF mode	XTS = 0, XT1BYPASS = 0		32	2768		Hz
f <sub>XT1,LF,SW</sub>	XT1 oscillator logic-level square- wave input frequency, LF mode	XTS = 0, XT1BYPASS = 1 <sup>(2) (3)</sup>		10 32	.768	50	kHz
<u></u>	Oscillation allowance for	$\begin{array}{l} \text{XTS} = 0, \\ \text{XT1BYPASS} = 0, \text{XT1DRIVEx} = 0, \\ \text{f}_{\text{XT1,LF}} = 32768 \text{ Hz}, \text{C}_{\text{L,eff}} = 6 \text{ pF} \end{array}$			210		1-0
UA <sub>LF</sub>	LF crystals <sup>(4)</sup>	$\begin{array}{l} \text{XTS} = 0, \\ \text{XT1BYPASS} = 0, \text{XT1DRIVEx} = 1, \\ \text{f}_{\text{XT1,LF}} = 32768 \text{ Hz}, \text{C}_{\text{L,eff}} = 12 \text{ pF} \end{array}$			300		K12
		$XTS = 0, XCAPx = 0^{(6)}$			2		
0	Integrated effective load	XTS = 0, XCAPx = 1			5.5		~ Г
C <sub>L,eff</sub>	capacitance, LF mode <sup>(5)</sup>	XTS = 0, XCAPx = 2			8.5		рг
		XTS = 0, XCAPx = 3			12.0		
	Duty cycle, LF mode	XTS = 0, Measured at ACLK, $f_{XT1,LF} = 32768 \text{ Hz}$		30		70	%
f <sub>Fault,LF</sub>	Oscillator fault frequency, LF mode <sup>(7)</sup>	$XTS = 0^{(8)}$		10	1(	0000	Hz
+	Startup time LE mode	$ \begin{array}{l} f_{OSC} = 32768 \text{ Hz}, \text{ XTS} = 0, \\ \text{XT1BYPASS} = 0, \text{ XT1DRIVEx} = 0, \\ \text{T}_{\text{A}} = 25^{\circ}\text{C}, \text{ C}_{\text{L,eff}} = 6 \text{ pF} \end{array} $	2 \/	1	1000		me
t <sub>START,LF</sub>	Startup time, LF mode		5 V		500		1112

(1) To improve EMI on the XT1 oscillator, the following guidelines should be observed.

(a) Keep the trace between the device and the crystal as short as possible.

(b) Design a good ground plane around the oscillator pins.

(c) Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.

(d) Avoid running PCB traces underneath or adjacent to the XIN and XOUT pins.

(e) Use assembly materials and techniques that avoid any parasitic load on the oscillator XIN and XOUT pins.

(f) If conformal coating is used, make sure that it does not induce capacitive or resistive leakage between the oscillator pins.

When XT1BYPASS is set, XT1 circuits are automatically powered down. Input signal is a digital square wave with parametrics defined in (2) the Schmitt-trigger Inputs section of this datasheet.

Maximum frequency of operation of the entire device cannot be exceeded. (3)

Oscillation allowance is based on a safety factor of 5 for recommended crystals. The oscillation allowance is a function of the XT1DRIVEx settings and the effective load. In general, comparable oscillator allowance can be achieved based on the following (4)guidelines, but should be evaluated based on the actual crystal selected for the application:

- (a) For XT1DRIVEx = 0,  $C_{L,eff} \le 6 \text{ pF.}$ (b) For XT1DRIVEx = 1,  $6 \text{ pF} \le C_{L,eff} \le 9 \text{ pF.}$ (c) For XT1DRIVEx = 2,  $6 \text{ pF} \le C_{L,eff} \le 10 \text{ pF.}$ (d) For XT1DRIVEx = 3,  $C_{L,eff} \le 6 \text{ pF.}$
- Includes parasitic bond and package capacitance (approximately 2 pF per pin). (5) Because the PCB adds additional capacitance, it is recommended to verify the correct load by measuring the ACLK frequency. For a correct setup, the effective load capacitance should always match the specification of the used crystal.

Requires external capacitors at both terminals. Values are specified by crystal manufacturers. (6)

Frequencies below the MIN specification set the fault flag. Frequencies above the MAX specification do not set the fault flag. (7)

Frequencies in between might set the flag.

(8) Measured with logic-level input frequency but also applies to operation with crystals.

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INSTRUMENTS

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# MSP430F5342, MSP430F5341, MSP430F5340

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# Crystal Oscillator, XT2

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)<sup>(1) (2)</sup>

	PARAMETER	TEST CONDITIONS	Vcc	MIN	TYP	MAX	UNIT	
		$f_{OSC} = 4 \text{ MHz}, \text{ XT2OFF} = 0,$ XT2BYPASS = 0, XT2DRIVEx = 0, T <sub>A</sub> = 25°C			200			
	XT2 oscillator crystal current	$f_{OSC}$ = 12 MHz, XT2OFF = 0, XT2BYPASS = 0, XT2DRIVEx = 1, T <sub>A</sub> = 25°C	2.1/		260			
DVCC.XT2	consumption	$f_{OSC}$ = 20 MHz, XT2OFF = 0, XT2BYPASS = 0, XT2DRIVEx = 2, T <sub>A</sub> = 25°C	3 V		325		μΑ	
		$f_{OSC}$ = 32 MHz, XT2OFF = 0, XT2BYPASS = 0, XT2DRIVEx = 3, T <sub>A</sub> = 25°C			450			
f <sub>XT2,HF0</sub>	XT2 oscillator crystal frequency, mode 0	XT2DRIVEx = 0, XT2BYPASS = $0^{(3)}$		4		8	MHz	
f <sub>XT2,HF1</sub>	XT2 oscillator crystal frequency, mode 1	XT2DRIVEx = 1, XT2BYPASS = $0^{(3)}$		8		16	MHz	
f <sub>XT2,HF2</sub>	XT2 oscillator crystal frequency, mode 2	XT2DRIVEx = 2, XT2BYPASS = $0^{(3)}$		16		24	MHz	
f <sub>XT2,HF3</sub>	XT2 oscillator crystal frequency, mode 3	XT2DRIVEx = 3, XT2BYPASS = $0^{(3)}$		24		32	MHz	
f <sub>XT2,HF,SW</sub>	XT2 oscillator logic-level square-wave input frequency, bypass mode	XT2BYPASS = 1 <sup>(4) (3)</sup>		0.7		32	MHz	
		$\begin{array}{l} XT2DRIVEx = 0, \ XT2BYPASS = 0, \\ f_{XT2,HF0} = 6 \ MHz, \ C_{L,eff} = 15 \ pF \end{array}$			450			
0.0	Oscillation allowance for	$\begin{array}{l} XT2DRIVEx = 1, \ XT2BYPASS = 0, \\ f_{XT2,HF1} = 12 \ MHz, \ C_{L,eff} = 15 \ pF \end{array}$			320		0	
OA <sub>HF</sub>	HF crystals <sup>(5)</sup>	$\begin{array}{l} XT2DRIVEx = 2, \ XT2BYPASS = 0, \\ f_{XT2,HF2} = 20 \ \text{MHz}, \ C_{L,eff} = 15 \ \text{pF} \end{array}$			200		Ω	
		$\begin{array}{l} XT2DRIVEx = 3, \ XT2BYPASS = 0, \\ f_{XT2,HF3} = 32 \ MHz, \ C_{L,eff} = 15 \ pF \end{array}$			200			
+	Startup time		2 \/		0.5			
'START,HF		$ \begin{array}{l} f_{OSC} = 20 \text{ MHz}, \\ \text{XT2BYPASS} = 0, \text{ XT2DRIVEx} = 2, \\ \text{T}_{\text{A}} = 25^{\circ}\text{C}, \text{ C}_{\text{L,eff}} = 15 \text{ pF} \end{array} $	5 V		0.3		1115	
C <sub>L,eff</sub>	Integrated effective load capacitance, HF mode <sup>(6) (1)</sup>				1		pF	
	Duty cycle	Measured at ACLK, $f_{XT2,HF2} = 20 \text{ MHz}$		40	50	60	%	
f <sub>Fault,HF</sub>	Oscillator fault frequency <sup>(7)</sup>	$XT2BYPASS = 1^{(8)}$		30		300	kHz	

(1) Requires external capacitors at both terminals. Values are specified by crystal manufacturers. In general, an effective load capacitance of up to 18 pF can be supported.

(2) To improve EMI on the XT2 oscillator the following guidelines should be observed.

(a) Keep the traces between the device and the crystal as short as possible.

(b) Design a good ground plane around the oscillator pins.

(c) Prevent crosstalk from other clock or data lines into oscillator pins XT2IN and XT2OUT.

(d) Avoid running PCB traces underneath or adjacent to the XT2IN and XT2OUT pins.

(e) Use assembly materials and techniques that avoid any parasitic load on the oscillator XT2IN and XT2OUT pins.

(f) If conformal coating is used, make sure that it does not induce capacitive or resistive leakage between the oscillator pins.

(3) This represents the maximum frequency that can be input to the device externally. Maximum frequency achievable on the device

operation is based on the frequencies present on ACLK, MCLK, and SMCLK cannot be exceed for a given range of operation.

(4) When XT2BYPASS is set, the XT2 circuit is automatically powered down. Input signal is a digital square wave with parametrics defined in the Schmitt-trigger Inputs section of this datasheet.

(5) Oscillation allowance is based on a safety factor of 5 for recommended crystals.

(6) Includes parasitic bond and package capacitance (approximately 2 pF per pin).

Because the PCB adds additional capacitance, it is recommended to verify the correct load by measuring the ACLK frequency. For a correct setup, the effective load capacitance should always match the specification of the used crystal.

(7) Frequencies below the MIN specification set the fault flag. Frequencies above the MAX specification do not set the fault flag.

Frequencies in between might set the flag.

(8) Measured with logic-level input frequency but also applies to operation with crystals.

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#### Internal Very-Low-Power Low-Frequency Oscillator (VLO)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	V <sub>cc</sub>	MIN	TYP	MAX	UNIT
f <sub>VLO</sub>	VLO frequency	Measured at ACLK	1.8 V to 3.6 V	6	9.4	14	kHz
$df_{VLO}/d_T$	VLO frequency temperature drift	Measured at ACLK <sup>(1)</sup>	1.8 V to 3.6 V		0.5		%/°C
$df_{VLO}/dV_{CC}$	VLO frequency supply voltage drift	Measured at ACLK <sup>(2)</sup>	1.8 V to 3.6 V		4		%/V
	Duty cycle	Measured at ACLK	1.8 V to 3.6 V	40	50	60	%

(1) Calculated using the box method:  $(MAX(-40 \text{ to } 85^{\circ}\text{C}) - MIN(-40 \text{ to } 85^{\circ}\text{C})) / MIN(-40 \text{ to } 85^{\circ}\text{C}) / (85^{\circ}\text{C} - (-40^{\circ}\text{C}))$ (2) Calculated using the box method: (MAX(1.8 to 3.6 V) - MIN(1.8 to 3.6 V)) / MIN(1.8 to 3.6 V) / (3.6 V - 1.8 V)

#### (2) Calculated using the box method. $(M \land (1.0 to 3.0 t)) = M ((1.0 to 3.0 t)) / M ((1.0 to 3.0 t)) / (3.0 to 3.0 t))$

# Internal Reference, Low-Frequency Oscillator (REFO)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	V <sub>cc</sub>	MIN	TYP	MAX	UNIT
I <sub>REFO</sub>	REFO oscillator current consumption	$T_A = 25^{\circ}C$	1.8 V to 3.6 V		3		μA
	REFO frequency calibrated	Measured at ACLK	1.8 V to 3.6 V		32768		Hz
f <sub>REFO</sub>	REFO absolute tolerance calibrated	Full temperature range	1.8 V to 3.6 V			±3.5	%
		$T_A = 25^{\circ}C$	3 V			±1.5	%
$df_{REFO}/d_{T}$	REFO frequency temperature drift	Measured at ACLK <sup>(1)</sup>	1.8 V to 3.6 V		0.01		%/°C
$df_{REFO}/dV_{CC}$	REFO frequency supply voltage drift	Measured at ACLK <sup>(2)</sup>	1.8 V to 3.6 V		1.0		%/V
	Duty cycle	Measured at ACLK	1.8 V to 3.6 V	40	50	60	%
t <sub>START</sub>	REFO startup time	40%/60% duty cycle	1.8 V to 3.6 V		25		μs

(1) Calculated using the box method:  $(MAX(-40 \text{ to } 85^{\circ}\text{C}) - MIN(-40 \text{ to } 85^{\circ}\text{C})) / MIN(-40 \text{ to } 85^{\circ}\text{C}) / (85^{\circ}\text{C} - (-40^{\circ}\text{C}))$ 

(2) Calculated using the box method: (MAX(1.8 to 3.6 V) - MIN(1.8 to 3.6 V)) / MIN(1.8 to 3.6 V) / (3.6 V - 1.8 V)



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#### **DCO Frequency**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f <sub>DCO(0,0)</sub>	DCO frequency (0, 0) <sup>(1)</sup>	DCORSELx = 0, $DCOx = 0$ , $MODx = 0$	0.07		0.20	MHz
f <sub>DCO(0,31)</sub>	DCO frequency (0, 31) <sup>(1)</sup>	DCORSELx = 0, DCOx = 31, MODx = 0	0.70		1.70	MHz
f <sub>DCO(1,0)</sub>	DCO frequency (1, 0) <sup>(1)</sup>	DCORSELx = 1, DCOx = 0, MODx = 0	0.15		0.36	MHz
f <sub>DCO(1,31)</sub>	DCO frequency (1, 31) <sup>(1)</sup>	DCORSELx = 1, DCOx = 31, MODx = 0	1.47		3.45	MHz
f <sub>DCO(2,0)</sub>	DCO frequency (2, 0) <sup>(1)</sup>	DCORSELx = 2, $DCOx = 0$ , $MODx = 0$	0.32		0.75	MHz
f <sub>DCO(2,31)</sub>	DCO frequency (2, 31) <sup>(1)</sup>	DCORSELx = 2, DCOx = 31, MODx = 0	3.17		7.38	MHz
f <sub>DCO(3,0)</sub>	DCO frequency (3, 0) <sup>(1)</sup>	DCORSELx = 3, $DCOx = 0$ , $MODx = 0$	0.64		1.51	MHz
f <sub>DCO(3,31)</sub>	DCO frequency (3, 31) <sup>(1)</sup>	DCORSELx = 3, DCOx = 31, MODx = 0	6.07		14.0	MHz
f <sub>DCO(4,0)</sub>	DCO frequency (4, 0) <sup>(1)</sup>	DCORSELx = 4, $DCOx = 0$ , $MODx = 0$	1.3		3.2	MHz
f <sub>DCO(4,31)</sub>	DCO frequency (4, 31) <sup>(1)</sup>	DCORSELx = 4, DCOx = 31, MODx = 0	12.3		28.2	MHz
f <sub>DCO(5,0)</sub>	DCO frequency (5, 0) <sup>(1)</sup>	DCORSELx = 5, $DCOx = 0$ , $MODx = 0$	2.5		6.0	MHz
f <sub>DCO(5,31)</sub>	DCO frequency (5, 31) <sup>(1)</sup>	DCORSELx = 5, DCOx = 31, MODx = 0	23.7		54.1	MHz
f <sub>DCO(6,0)</sub>	DCO frequency (6, 0) <sup>(1)</sup>	DCORSELx = 6, $DCOx = 0$ , $MODx = 0$	4.6		10.7	MHz
f <sub>DCO(6,31)</sub>	DCO frequency (6, 31) <sup>(1)</sup>	DCORSELx = 6, DCOx = 31, MODx = 0	39.0		88.0	MHz
f <sub>DCO(7,0)</sub>	DCO frequency (7, 0) <sup>(1)</sup>	DCORSELx = 7, $DCOx = 0$ , $MODx = 0$	8.5		19.6	MHz
f <sub>DCO(7,31)</sub>	DCO frequency (7, 31) <sup>(1)</sup>	DCORSELx = 7, DCOx = 31, MODx = 0	60		135	MHz
S <sub>DCORSEL</sub>	Frequency step between range DCORSEL and DCORSEL + 1	$S_{RSEL} = f_{DCO(DCORSEL+1,DCO)}/f_{DCO(DCORSEL,DCO)}$	1.2		2.3	ratio
S <sub>DCO</sub>	Frequency step between tap DCO and DCO + 1	$S_{DCO} = f_{DCO(DCORSEL, DCO+1)}/f_{DCO(DCORSEL, DCO)}$	1.02		1.12	ratio
	Duty cycle	Measured at SMCLK	40	50	60	%
df <sub>DCO</sub> /dT	DCO frequency temperature drift <sup>(2)</sup>	f <sub>DCO</sub> = 1 MHz,		0.1		%/°C
df <sub>DCO</sub> /dV <sub>CC</sub>	DCO frequency voltage drift <sup>(3)</sup>	f <sub>DCO</sub> = 1 MHz		1.9		%/V

When selecting the proper DCO frequency range (DCORSELx), the target DCO frequency, f<sub>DCO</sub>, should be set to reside within the (1) range of  $f_{DCO(n, 0),MAX} \le f_{DCO} \le f_{DCO(n, 31),MIN}$ , where  $f_{DCO(n, 0),MAX}$  represents the maximum frequency specified for the DCO frequency, range n, tap 0 (DCOx = 0) and  $f_{DCO(n, 31),MIN}$  represents the minimum frequency specified for the DCO frequency, range n, tap 31 (DCOx = 31). This ensures that the target DCO frequency resides within the range selected. It should also be noted that if the actual  $f_{DCO}$  frequency for the selected range causes the FLL or the application to select tap 0 or 31, the DCO fault flag is set to report that the selected range is at its minimum or maximum tap setting. Calculated using the box method: (MAX(-40 to 85°C) – MIN(-40 to 85°C)) / MIN(-40 to 85°C) / (85°C – (-40°C)) Calculated using the box method: (MAX(1.8 to 3.6 V) – MIN(1.8 to 3.6 V)) / MIN(1.8 to 3.6 V) / (3.6 V – 1.8 V)

(2)(3)





Product Folder Links: MSP430F5342 MSP430F5341 MSP430F5340





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#### PMM, Brown-Out Reset (BOR)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V <sub>(DVCC_BOR_IT-)</sub>	$BOR_{H}$ on voltage, $DV_{CC}$ falling level	$  dDV_{CC}/d_t   < 3 V/s$			1.45	V
V <sub>(DVCC_BOR_IT+)</sub>	BOR <sub>H</sub> off voltage, DV <sub>CC</sub> rising level	$  dDV_{CC}/d_t   < 3 V/s$	0.80	1.30	1.50	V
V <sub>(DVCC_BOR_hys)</sub>	BOR <sub>H</sub> hysteresis		60		250	mV
t <sub>RESET</sub>	Pulse duration required at $\overline{\text{RST}}/\text{NMI}$ pin to accept a reset		2			μs

#### PMM, Core Voltage

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN TYP MAX	UNIT
V <sub>CORE3</sub> (AM)	Core voltage, active mode, PMMCOREV = 3	$2.4 \text{ V} \leq \text{DV}_{\text{CC}} \leq 3.6 \text{ V}$	1.90	V
V <sub>CORE2</sub> (AM)	Core voltage, active mode, PMMCOREV = 2	$2.2 \text{ V} \leq \text{DV}_{\text{CC}} \leq 3.6 \text{ V}$	1.80	V
V <sub>CORE1</sub> (AM)	Core voltage, active mode, PMMCOREV = 1	$2.0 \text{ V} \leq \text{DV}_{\text{CC}} \leq 3.6 \text{ V}$	1.60	V
V <sub>CORE0</sub> (AM)	Core voltage, active mode, PMMCOREV = 0	$1.8 \text{ V} \le \text{DV}_{\text{CC}} \le 3.6 \text{ V}$	1.40	V
V <sub>CORE3</sub> (LPM)	Core voltage, low-current mode, PMMCOREV = 3	$2.4 \text{ V} \leq \text{DV}_{\text{CC}} \leq 3.6 \text{ V}$	1.94	V
V <sub>CORE2</sub> (LPM)	Core voltage, low-current mode, PMMCOREV = 2	$2.2 \text{ V} \leq \text{DV}_{\text{CC}} \leq 3.6 \text{ V}$	1.84	V
V <sub>CORE1</sub> (LPM)	Core voltage, low-current mode, PMMCOREV = 1	$2.0 \text{ V} \leq \text{DV}_{\text{CC}} \leq 3.6 \text{ V}$	1.64	V
V <sub>CORE0</sub> (LPM)	Core voltage, low-current mode, PMMCOREV = 0	$1.8 \text{ V} \le \text{DV}_{\text{CC}} \le 3.6 \text{ V}$	1.44	V



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# PMM, SVS High Side

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
		SVSHE = 0, DV <sub>CC</sub> = 3.6 V		0		nA
I <sub>(SVSH)</sub>	SVS current consumption	SVSHE = 1, DV <sub>CC</sub> = 3.6 V, SVSHFP = 0		200		nA
		SVSHE = 1, DV <sub>CC</sub> = 3.6 V, SVSHFP = 1		1.5		μA
		SVSHE = 1, SVSHRVL = 0	1.57	1.68	1.78	
V	$\Omega \setminus \Omega$ on voltage level <sup>(1)</sup>	SVSHE = 1, SVSHRVL = 1	1.79	1.88	1.98	V
V(SVSH_IT-)	SVSH on voltage level (*)	SVSHE = 1, SVSHRVL = 2	1.98	2.08	2.21	
		SVSHE = 1, SVSHRVL = 3	2.10	2.18	2.31	
	$SVS_H$ off voltage level <sup>(1)</sup>	SVSHE = 1, SVSMHRRL = 0	1.62	1.74	1.85	
		SVSHE = 1, SVSMHRRL = 1	1.88	1.94	2.07	- - - -
		SVSHE = 1, SVSMHRRL = 2	2.07	2.14	2.28	
		SVSHE = 1, SVSMHRRL = 3	2.20	2.30	2.42	
V(SVSH_IT+)		SVSHE = 1, SVSMHRRL = 4	2.32	2.40	2.55	
		SVSHE = 1, SVSMHRRL = 5	2.52	2.70	2.88	
		SVSHE = 1, SVSMHRRL = 6	2.90	3.10	3.23	
		SVSHE = 1, SVSMHRRL = 7	2.90	3.10	3.23	
	0)/0	SVSHE = 1, dV <sub>DVCC</sub> /dt = 10 mV/µs, SVSHFP = 1		2.5		
<sup>t</sup> pd(SVSH)	SVS <sub>H</sub> propagation delay	SVSHE = 1, $dV_{DVCC}/dt = 1 \text{ mV/}\mu\text{s}$ , SVSHFP = 0		20		μs
		$\begin{array}{l} {\sf SVSHE}=0\rightarrow 1,{\sf dV}_{{\sf DVCC}}/{\sf dt}=10{\sf mV}/\mu{\sf s},\\ {\sf SVSHFP}=1 \end{array}$		12.5		
t <sub>(SVSH)</sub>	SVS <sub>H</sub> on or off delay time	$\label{eq:VSHE} \hline \begin{array}{l} \text{SVSHE} = 0 \rightarrow 1,  dV_{DVCC}/dt = 1   mV/\mu s, \\ \text{SVSHFP} = 0 \end{array}$		100		μs
dV <sub>DVCC</sub> /dt	DV <sub>CC</sub> rise time		0		1000	V/s

(1) The SVS<sub>H</sub> settings available depend on the VCORE (PMMCOREVx) setting. See the Power Management Module and Supply Voltage Supervisor chapter in the MSP430x5xx and MSP430x6xx Family User's Guide (SLAU208) on recommended settings and usage.

Product Folder Links: MSP430F5342 MSP430F5341 MSP430F5340



# MSP430F5342, MSP430F5341, MSP430F5340

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#### PMM, SVM High Side

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
		SVMHE = 0, DV <sub>CC</sub> = 3.6 V		0		nA
I <sub>(SVMH)</sub>	SVM <sub>H</sub> current consumption	SVMHE= 1, DV <sub>CC</sub> = 3.6 V, SVMHFP = 0		200		nA
		SVMHE = 1, DV <sub>CC</sub> = 3.6 V, SVMHFP = 1		1.5		μA
		SVMHE = 1, SVSMHRRL = 0	1.62	1.74	1.85	
		SVMHE = 1, SVSMHRRL = 1	1.88	1.94	2.07	
		SVMHE = 1, SVSMHRRL = 2	2.07	2.14	2.28	1
	$\mathrm{SVM}_\mathrm{H}$ on or off voltage level $^{(1)}$	SVMHE = 1, SVSMHRRL = 3	2.20	2.30	2.42	
V <sub>(SVMH)</sub>		SVMHE = 1, SVSMHRRL = 4	2.32	2.40	2.55	V
		SVMHE = 1, SVSMHRRL = 5	2.52	2.70	2.88	
		SVMHE = 1, SVSMHRRL = 6	2.90	3.10	3.23	
		SVMHE = 1, SVSMHRRL = 7	2.90	3.10	3.23	
		SVMHE = 1, SVMHOVPE = 1		3.75		
		SVMHE = 1, dV <sub>DVCC</sub> /dt = 10 mV/µs, SVMHFP = 1		2.5		
t <sub>pd(SVMH)</sub>	SVM <sub>H</sub> propagation delay	SVMHE = 1, $dV_{DVCC}/dt = 1 \text{ mV/}\mu\text{s}$ , SVMHFP = 0		20		μs
	$SVM_H$ on or off delay time	$\begin{array}{l} \text{SVMHE} = 0 \rightarrow 1,  \text{dV}_{\text{DVCC}}/\text{dt} = 10  \text{mV}/\mu\text{s}, \\ \text{SVMHFP} = 1 \end{array}$		12.5		
t <sub>(SVMH)</sub>		$ \begin{array}{l} \text{SVMHE}=0\rightarrow1,\text{dV}_{\text{DVCC}}/\text{dt}=1\text{mV}/\mu\text{s},\\ \text{SVMHFP}=0 \end{array} \end{array} $		100		μs

(1) The SVM<sub>H</sub> settings available depend on the VCORE (PMMCOREVx) setting. See the *Power Management Module and Supply Voltage Supervisor* chapter in the *MSP430x5xx and MSP430x6xx Family User's Guide* (SLAU208) on recommended settings and usage.

#### PMM, SVS Low Side

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
		SVSLE = 0, PMMCOREV = 2	0			nA
I <sub>(SVSL)</sub>	$SVS_L$ current consumption	SVSLE = 1, PMMCOREV = 2, SVSLFP = 0	200		nA	
		SVSLE = 1, PMMCOREV = 2, SVSLFP = 1		1.5		μA
		SVSLE = 1, dV <sub>CORE</sub> /dt = 10 mV/µs, SVSLFP = 1		2.5		
tpd(SVSL)	SVSL propagation delay	SVSLE = 1, dV <sub>CORE</sub> /dt = 1 mV/µs, SVSLFP = 0		20		μs
t <sub>(SVSL)</sub>	CV/C on or off dolou time	SVSLE = 0 $\rightarrow$ 1, dV <sub>CORE</sub> /dt = 10 mV/µs, SVSLFP = 1		12.5		
	SVSL on or on delay time	SVSLE = 0 $\rightarrow$ 1, dV <sub>CORE</sub> /dt = 1 mV/µs, SVSLFP = 0		100		μs

#### PMM, SVM Low Side

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
	SVM <sub>L</sub> current consumption	SVMLE = 0, PMMCOREV = 2		0		nA	
I <sub>(SVML)</sub>		SVMLE= 1, PMMCOREV = 2, SVMLFP = 0		200		nA	
		SVMLE= 1, PMMCOREV = 2, SVMLFP = 1		1.5		μA	
		SVMLE = 1, dV <sub>CORE</sub> /dt = 10 mV/µs, SVMLFP = 1		2.5			
t <sub>pd</sub> (SVML)	SVIML propagation delay	SVMLE = 1, dV <sub>CORE</sub> /dt = 1 mV/µs, SVMLFP = 0		20		μs	
t <sub>(SVML)</sub>	$SVM_L$ on or off delay time	SVMLE = 0 $\rightarrow$ 1, dV <sub>CORE</sub> /dt = 10 mV/µs, SVMLFP = 1		12.5			
		SVMLE = 0 $\rightarrow$ 1, dV <sub>CORE</sub> /dt = 1 mV/µs, SVMLFP = 0		100		μs	



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# Wake Up From Low Power Modes and Reset

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

	PARAMETER	TEST CONDITIO	NS	MIN	TYP	MAX	UNIT
	Wake-up time from LPM2,	PMMCOREV = SVSMLRRL = n	f <sub>MCLK</sub> ≥ 4.0 MHz		3.5	7.5	
t <sub>WAKE-UP-FAST</sub>	LPM3, or LPM4 to active mode <sup>(1)</sup>	(where n = 0, 1, 2, or 3), SVSLFP = 1	1.0 MHz < f <sub>MCLK</sub> < 4.0 MHz		4.5	9	μs
t <sub>WAKE-UP-SLOW</sub>	Wake-up time from LPM2, LPM3 or LPM4 to active mode <sup>(2)</sup>	$\begin{array}{l} PMMCOREV = SVSMLRRL = n \\ (\text{where } n = 0,  1,  2,  \text{or } 3), \\ SVSLFP = 0 \end{array}$			150	165	μs
t <sub>WAKE-UP-LPM5</sub>	Wake-up time from LPM4.5 to active mode <sup>(3)</sup>				2	3	ms
t <sub>WAKE-UP-RESET</sub>	Wake-up time from $\overline{\text{RST}}$ or BOR event to active mode <sup>(3)</sup>				2	3	ms

(1) This value represents the time from the wakeup event to the first active edge of MCLK. The wakeup time depends on the performance mode of the low side supervisor (SVS<sub>L</sub>) and low side monitor (SVM<sub>L</sub>). Fastest wakeup times are possible with SVS<sub>L</sub> and SVM<sub>L</sub> in full performance mode or disabled when operating in AM, LPM0, and LPM1. Various options are available for SVS<sub>L</sub> and SVM<sub>L</sub> while operating in LPM2, LPM3, and LPM4. See the *Power Management Module and Supply Voltage Supervisor* chapter in the *MSP430x5xx* and *MSP430x6xx Family User's Guide* (SLAU208).

(2) This value represents the time from the wakeup event to the first active edge of MCLK. The wakeup time depends on the performance mode of the low side supervisor (SVS<sub>L</sub>) and low side monitor (SVM<sub>L</sub>). In this case, the SVS<sub>L</sub>and SVM<sub>L</sub> are in normal mode (low current) mode when operating in AM, LPM0, and LPM1. Various options are available for SVS<sub>L</sub>and SVM<sub>L</sub> while operating in LPM2, LPM3, and LPM4. See the *Power Management Module and Supply Voltage Supervisor* chapter in the *MSP430x5xx and MSP430x6xx Family User's Guide* (SLAU208).

(3) This value represents the time from the wakeup event to the reset vector execution.

#### Timer\_A

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	V <sub>cc</sub>	MIN	TYP	MAX	UNIT
f <sub>TA</sub>	Timer_A input clock frequency	Internal: SMCLK, ACLK, External: TACLK, Duty cycle = 50% ± 10%	1.8 V, 3 V			25	MHz
t <sub>TA,cap</sub>	Timer_A capture timing	All capture inputs, minimum pulse duration required for capture	1.8 V, 3 V	20			ns

#### Timer\_B

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V <sub>cc</sub>	MIN TYP MAX		MAX	UNIT
f <sub>TB</sub>	Timer_B input clock frequency	Internal: SMCLK, ACLK, External: TBCLK, Duty cycle = 50% ± 10%	1.8 V, 3 V			25	MHz
t <sub>TB,cap</sub>	Timer_B capture timing	All capture inputs, minimum pulse duration required for capture	1.8 V, 3 V	20			ns

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USCI (UART Mode) Recommended Operating Conditions											
	PARAMETER	CONDITIONS	V <sub>cc</sub>	MIN	TYP	MAX	UNIT				
f <sub>USCI</sub>	USCI input clock frequency	Internal: SMCLK, ACLK, External: UCLK, Duty cycle = $50\% \pm 10\%$				f <sub>SYSTEM</sub>	MHz				
f <sub>BITCLK</sub>	BITCLK clock frequency (equals baud rate in MBaud)					1	MHz				

#### USCI (UART Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	V <sub>cc</sub>	MIN	TYP MAX	UNIT
t <sub>r</sub>	UART receive deglitch time <sup>(1)</sup>		2.2 V	50	600	
			3 V	50	600	ns

(1)Pulses on the UART receive input (UCxRX) shorter than the UART receive deglitch time are suppressed. To ensure that pulses are correctly recognized their width should exceed the maximum specification of the deglitch time.

#### USCI (SPI Master Mode) Recommended Operating Conditions

PARAMETER		CONDITIONS	V <sub>cc</sub>	MIN	TYP	MAX	UNIT
f <sub>USCI</sub>	USCI input clock frequency	Internal: SMCLK, ACLK, Duty cycle = 50% ± 10%				f <sub>SYSTEM</sub>	MHz

#### **USCI (SPI Master Mode)**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

(see Note <sup>(1)</sup>, Figure 12 and Figure 13)

	PARAMETER	TEST CONDITIONS	V <sub>cc</sub>	MIN	TYP	MAX	UNIT
f <sub>USCI</sub>	USCI input clock frequency	SMCLK, ACLK, Duty cycle = $50\% \pm 10\%$			fg	SYSTEM	MHz
			1.8 V	55			20
4	SOM input data actus tima	PMMCOREV = 0	3 V	38			ns
<sup>L</sup> SU,MI	SOMI input data setup time		2.4 V	30			
		PMINCOREV = 3	3 V	25			ns
			1.8 V	0			
	SOMI input data hold time	PMIMCOREV = 0	3 V	0			ns
t <sub>HD,MI</sub>		PMMCOREV = 3	2.4 V	0			
			3 V	0			ns
		UCLK edge to SIMO valid,	1.8 V			20	
		$C_L = 20 \text{ pF}, \text{PMMCOREV} = 0$	3 V			18	ns
t <sub>VALID,MO</sub>	SIMO output data valid time <sup>(2)</sup>	UCLK edge to SIMO valid.	2.4 V			16	
		$C_L = 20 \text{ pF}, \text{PMMCOREV} = 3$	3 V			15	ns
			1.8 V	-10			
t <sub>HD,MO</sub>		$C_L = 20 \text{ pr}, \text{PMMCOREV} = 0$	3 V	-8			ns
	SIMO output data hold time ()		2.4 V	-10			-
		$G_L = 20 \text{ pr}, \text{PMMCOREV} = 3$	3 V	-8			ns

 f<sub>UCxCLK</sub> = 1/2t<sub>LO/HI</sub> with t<sub>LO/HI</sub> ≥ max(t<sub>VALID,MO(USCI</sub>) + t<sub>SU,SI(Slave</sub>), t<sub>SU,MI(USCI</sub>) + t<sub>VALID,SO(Slave</sub>)). For the slave's parameters t<sub>SU,SI(Slave</sub>) and t<sub>VALID,SO(Slave</sub>) refer to the SPI parameters of the attached slave.
Specifies the time to drive the next valid data to the SIMO output after the output changing UCLK clock edge. See the timing diagrams in Figure 12 and Figure 13.

(3) Specifies how long data on the SIMO output is valid after the output changing UCLK clock edge. Negative values indicate that the data on the SIMO output can become invalid before the output changing clock edge observed on UCLK. See the timing diagrams in Figure 12 and Figure 13.



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Figure 12. SPI Master Mode, CKPH = 0



Figure 13. SPI Master Mode, CKPH = 1



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#### **USCI (SPI Slave Mode)**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note <sup>(1)</sup>, Figure 14 and Figure 15)

	PARAMETER	TEST CONDITIONS	V <sub>cc</sub>	MIN	ΤΥΡ ΜΑΧ	UNIT
			1.8 V	11		
		PMMCOREV = 0	3 V	8		ns
t <sub>STE,LEAD</sub>	STE lead time, STE low to clock		2.4 V	7		
		PMMCOREV = 3	3 V	6		ns
			1.8 V	3		
		PMMCOREV = 0	3 V	3		ns
t <sub>STE,LAG</sub>	STE lag time, last clock to STE high		2.4 V	3		
		PMMCOREV = 3	3 V	3		ns
			1.8 V		66	
	STE access time. STE low to SOMI data	PMMCOREV = 0	3 V		50	ns
t <sub>STE,ACC</sub>	out		2.4 V		36	
		PMMCOREV = 3	3 V		30	ns
			1.8 V		30	
	STE disable time. STE high to SOMI high	PMMCOREV = 0	3 V		23	ns
t <sub>STE,DIS</sub>	impedance		2.4 V		16	
		PMMCOREV = 3	3 V		13	ns
			1.8 V	5		
		PMMCOREV = 0	3 V	5		ns
t <sub>SU,SI</sub>	SIMO input data setup time		2.4 V	2		
		PMMCOREV = 3	3 V	2		ns
			1.8 V	5		
		PMMCOREV = 0	3 V	5		ns
t <sub>HD,SI</sub>	SIMO input data noid time		2.4 V	5		
		PIMINCOREV = 3	3 V	5		ns
		UCLK edge to SOMI valid,	1.8 V		76	
	$\mathbf{cond}$ subsub data walid time (2)	$C_L = 20 \text{ pF}, \text{PMMCOREV} = 0$	3 V		60	ns
t <sub>VALID,SO</sub>		UCLK edge to SOMI valid,	2.4 V		44	
		$C_L = 20 \text{ pF}, \text{PMMCOREV} = 3$	3 V		40	ns
			1.8 V	18		
	$\mathbf{COM}$ subsut data hold time <sup>(3)</sup>	$G_L = 20 \text{ pr}, \text{PIVIVICOREV} = 0$	3 V	12		ns
'HD,SO			2.4 V	10		<b>n</b> 0
		$G_{L} = 20 \text{ pr}, \text{PIVIIVICOREV} = 3$	3 V	8		ns

(1)

 $\begin{array}{l} f_{UCxCLK} = 1/2t_{LO/HI} \text{ with } t_{LO/HI} \geq max(t_{VALID,MO(Master)} + t_{SU,SI(USCI)}, t_{SU,MI(Master)} + t_{VALID,SO(USCI)}). \\ \\ For the master's parameters t_{SU,MI(Master)} and t_{VALID,MO(Master)} refer to the SPI parameters of the attached slave. \\ \\ Specifies the time to drive the next valid data to the SOMI output after the output changing UCLK clock edge. See the timing diagrams \\ \end{array}$ (2) in Figure 12 and Figure 13.

Specifies how long data on the SOMI output is valid after the output changing UCLK clock edge. See the timing diagrams in Figure 12 (3) and Figure 13.



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Figure 14. SPI Slave Mode, CKPH = 0







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#### USCI (I2C Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 16)

	PARAMETER	TEST CONDITIONS	V <sub>cc</sub>	MIN	ΤΥΡ Ι	MAX	UNIT
f <sub>USCI</sub>	USCI input clock frequency	Internal: SMCLK, ACLK External: UCLK Duty cycle = 50% ± 10%			f <sub>SY</sub>	STEM	MHz
f <sub>SCL</sub>	SCL clock frequency		2.2 V, 3 V	0		400	kHz
	Hold time (repeated) START	f <sub>SCL</sub> ≤ 100 kHz	221/21/	4.0			19
<sup>I</sup> HD,STA	Hold lime (repeated) START	f <sub>SCL</sub> > 100 kHz	2.2 V, 3 V	0.6			μs
+	Satur time for a repeated START	f <sub>SCL</sub> ≤ 100 kHz	221/21/	4.7			
<sup>I</sup> SU,STA	Setup time for a repeated START	f <sub>SCL</sub> > 100 kHz	2.2 V, 3 V	0.6			μs
t <sub>HD,DAT</sub>	Data hold time		2.2 V, 3 V	0			ns
t <sub>SU,DAT</sub>	Data setup time		2.2 V, 3 V	250			ns
	Setur time for STOD	f <sub>SCL</sub> ≤ 100 kHz	221/21/	4.0			
ISU,STO	Setup time for STOP	f <sub>SCL</sub> > 100 kHz	2.2 V, 3 V	0.6			μs
	Dulas width of aniles annuance d having at filles		2.2 V	50		600	
ISP	Pulse width of spikes suppressed by input filter		3 V	50		600	ns



Figure 16. I2C Mode Timing



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#### 12-Bit ADC, Power Supply and Input Range Conditions

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)<sup>(1)</sup>

	PARAMETER	TEST CONDITIONS	V <sub>cc</sub>	MIN	TYP	MAX	UNIT
AV <sub>CC</sub>	Analog supply voltage	AVCC and DVCC are connected together, AVSS and DVSS are connected together, $V_{(AVSS)} = V_{(DVSS)} = 0 V$		2.2		3.6	V
V <sub>(Ax)</sub>	Analog input voltage range <sup>(2)</sup>	All ADC12 analog input pins Ax		0		$AV_{CC}$	V
	Operating supply current into	f = 5 0 MHz <sup>(4)</sup>	2.2 V		125	155	
ADC12_A	AVCC terminal <sup>(3)</sup>	ADC12CLK = 5.0 MIHZ	3 V		150	220	μΑ
CI	Input capacitance	Only one terminal Ax can be selected at one time	2.2 V		20	25	pF
RI	Input MUX ON resistance	$0 V \le V_{Ax} \le AVCC$		10	200	1900	Ω

(1) The leakage current is specified by the digital I/O input leakage.

(2) The analog input voltage range must be within the selected reference voltage range V<sub>R+</sub> to V<sub>R-</sub> for valid conversion results. If the reference voltage is supplied by an external source or if the internal reference voltage is used and REFOUT = 1, then decoupling capacitors are required. See REF, External Reference and REF, Built-In Reference.

(3) The internal reference supply current is not included in current consumption parameter IADC12\_A.

(4) ADC12ON = 1, REFON = 0, SHT0 = 0, SHT1 = 0, ADC12DIV = 0.

#### 12-Bit ADC, Timing Parameters

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	V <sub>cc</sub>	MIN	TYP	MAX	UNIT
		For specified performance of ADC12 linearity parameters using an external reference voltage or AVCC as reference <sup>(1)</sup>		0.45	4.8	5.0	
f <sub>ADC12CLK</sub>	ADC conversion clock	For specified performance of ADC12 linearity parameters using the internal reference <sup>(2)</sup>	2.2 V, 3 V	0.45	2.4	4.0	MHz
		For specified performance of ADC12 linearity parameters using the internal reference <sup>(3)</sup>		0.45	2.4	2.7	
f <sub>ADC12OSC</sub>	Internal ADC12 oscillator <sup>(4)</sup>	ADC12DIV = 0, $f_{ADC12CLK} = f_{ADC12OSC}$	2.2 V, 3 V	4.2	4.8	5.4	MHz
	Occurring time	REFON = 0, Internal oscillator, ADC12OSC used for ADC conversion clock	2.2 V, 3 V	2.4		3.1	
<sup>t</sup> CONVERT	Conversion time	External $f_{ADC12CLK}$ from ACLK, MCLK, or SMCLK, ADC12SSEL $\neq$ 0			(5)		μs
t <sub>Sample</sub>	Sampling time	$R_{S} = 400 \Omega, R_{I} = 1000 \Omega, C_{I} = 20 pF,$ τ = [R <sub>S</sub> + R <sub>I</sub> ] × C <sub>I</sub> <sup>(6)</sup>	2.2 V, 3 V	1000			ns

(1) REFOUT = 0, external reference voltage: SREF2 = 0, SREF1 = 1, SREF0 = 0. AVCC as reference voltage: SREF2 = 0, SREF1 = 0, SREF0 = 0. The specified performance of the ADC12 linearity is ensured when using the ADC12OSC. For other clock sources, the specified performance of the ADC12 linearity is ensured with  $f_{ADC12CLK}$  maximum of 5.0 MHz.

(2) SREF2 = 0, SREF1 = 1, SREF0 = 0, ADC12SR = 0, REFOUT = 1

(a) SREF2 = 0, SREF1 = 1, SREF0 = 0, ADC12SR = 0, REFOUT = 0. The specified performance of the ADC12 linearity is ensured when using the ADC12OSC divided by 2.

(4) The ADC12OSC is sourced directly from MODOSC inside the UCS.

(5) 13 × ADC12DIV × 1/f<sub>ADC12CLK</sub>

(6) Approximately ten Tau ( $\tau$ ) are needed to get an error of less than ±0.5 LSB:

 $t_{\text{Sample}} = \ln(2^{n+1}) \times (R_S + R_I) \times C_I + 800 \text{ ns}, \text{ where } n = \text{ADC resolution} = 12, R_S = \text{external source resistance}$ 





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# 12-Bit ADC, Linearity Parameters Using an External Reference Voltage or AVCC as Reference Voltage

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	V <sub>cc</sub>	MIN	TYP	MAX	UNIT
-	Integral linearity error <sup>(1)</sup>	$1.4 \text{ V} \le \text{dVREF} \le 1.6 \text{ V}^{(2)}$	221/21/			±2.0	
El		1.6 V < dVREF <sup>(2)</sup>	2.2 V, 3 V			±1.7	LOD
ED	Differential linearity error <sup>(1)</sup>	(2)	2.2 V, 3 V			±1.0	LSB
_	Offset error <sup>(3)</sup>	dVREF ≤ 2.2 V <sup>(2)</sup>	2.2 V, 3 V		±1.0	±2.0	LSB
EO		dVREF > 2.2 V <sup>(2)</sup>	2.2 V, 3 V		±1.0	±2.0	
$E_{G}$	Gain error <sup>(3)</sup>	(2)	2.2 V, 3 V		±1.0	±2.0	LSB
-	Total upodivisted error	dVREF ≤ 2.2 V <sup>(2)</sup>	2.2 V, 3 V		±1.4	±3.5	
ΕT	l otal unadjusted error	dVREF > 2.2 V <sup>(2)</sup>	2.2 V, 3 V		±1.4	±3.5	LOD

(1) Parameters are derived using the histogram method.

(2) The external reference voltage is selected by: SREF2 = 0 or 1, SREF1 = 1, SREF0 = 0. dVREF = V<sub>R+</sub> - V<sub>R-</sub>, V<sub>R+</sub> < AVCC, V<sub>R-</sub> > AVSS. Unless otherwise mentioned, dVREF > 1.5 V. Impedance of the external reference voltage R < 100 Ω and two decoupling capacitors, 10 µF and 100 nF, should be connected to VREF to decouple the dynamic current. See also the *MSP430x5xx and MSP430x6xx Family User's Guide* (SLAU208).

(3) Parameters are derived using a best fit curve.

#### 12-Bit ADC, Linearity Parameters Using the Internal Reference Voltage

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

	PARAMETER	TEST CON	DITIONS <sup>(1)</sup>	V <sub>cc</sub>	MIN	TYP	MAX	UNIT
-	Integral	ADC12SR = 0, REFOUT = 1	f <sub>ADC12CLK</sub> ≤ 4.0 MHz	221/21/			±1.7	
ΓI	linearity error <sup>(2)</sup>	ADC12SR = 0, REFOUT = 0	f <sub>ADC12CLK</sub> ≤ 2.7 MHz	2.2 V, 3 V			±2.5	LOD
		ADC12SR = 0, REFOUT = 1	f <sub>ADC12CLK</sub> ≤ 4.0 MHz		-1.0		+2.0	
$E_D$	Differential linearity error <sup>(2)</sup>	ADC12SR = 0, REFOUT = 1	f <sub>ADC12CLK</sub> ≤ 2.7 MHz	2.2 V, 3 V	-1.0		+1.5	LSB
	integrity error	ADC12SR = 0, REFOUT = 0	f <sub>ADC12CLK</sub> ≤ 2.7 MHz		-1.0		+2.5	
-	Offeet error <sup>(3)</sup>	ADC12SR = 0, REFOUT = 1	f <sub>ADC12CLK</sub> ≤ 4.0 MHz	227 27		±1.0	±2.0	
⊏o	Oliset enor	ADC12SR = 0, REFOUT = 0	f <sub>ADC12CLK</sub> ≤ 2.7 MHz	2.2 V, 3 V		±1.0	±2.0	LOB
-		ADC12SR = 0, REFOUT = 1	f <sub>ADC12CLK</sub> ≤ 4.0 MHz	227 27		±1.0	±2.0	LSB
⊏G	$E_G$ Gain error <sup>(3)</sup>	ADC12SR = 0, REFOUT = 0	f <sub>ADC12CLK</sub> ≤ 2.7 MHz	2.2 V, 3 V			±1.5% <sup>(4)</sup>	VREF
	Total	ADC12SR = 0, REFOUT = 1	f <sub>ADC12CLK</sub> ≤ 4.0 MHz			±1.4	±3.5	LSB
Ε <sub>T</sub>	unadjusted error	ADC12SR = 0, REFOUT = 0	f <sub>ADC12CLK</sub> ≤ 2.7 MHz	2.2 V, 3 V			±1.5% <sup>(4)</sup>	VREF

(1) The internal reference voltage is selected by: SREF2 = 0 or 1, SREF1 = 1, SREF0 = 1. dVREF =  $V_{R+}$  -  $V_{R-}$ .

(2) Parameters are derived using the histogram method.

(3) Parameters are derived using a best fit curve.

(4) The gain error and total unadjusted error are dominated by the accuracy of the integrated reference module absolute accuracy. In this mode the reference voltage used by the ADC12\_A is not available on a pin.



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# MSP430F5342, MSP430F5341, MSP430F5340

SLAS706E - JULY 2011 - REVISED AUGUST 2013

#### 12-Bit ADC, Temperature Sensor and Built-In V<sub>MID</sub><sup>(1)</sup>

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	V <sub>cc</sub>	MIN	TYP	MAX	UNIT
	<b>C</b> = = (2)	ADC12ON = 1, INCH = 0Ah,	2.2 V		680		
VSENSOR	See	$T_A = 0^{\circ}C$	3 V		680		mv
то			2.2 V		2.25		m)//0C
I C <sub>SENSOR</sub>		ADC120N = 1, INCIT = 0AIT	3 V		2.25		IIIV/ C
	Sample time required if	ADC12ON = 1, INCH = 0Ah,	2.2 V	100			
t <sub>SENSOR(sample)</sub>	channel 10 is selected <sup>(3)</sup>	Error of conversion result ≤ 1 LSB	3 V	100			μs
	$AV_{CC}$ divider at channel 11, $V_{AVCC}$ factor	ADC12ON = 1, INCH = 0Bh		0.48	0.5	0.52	V <sub>AVCC</sub>
V <sub>MID</sub>	A)/ divider at abapped 11		2.2 V	1.06	1.1	1.14	V
	Av <sub>CC</sub> divider at channel 11	ADC12ON = 1, INCH = 0BI1	3 V	1.44	1.5	1.56	V
t <sub>VMID(sample)</sub>	Sample time required if channel 11 is selected <sup>(4)</sup>	ADC12ON = 1, INCH = 0Bh, Error of conversion result ≤ 1 LSB	2.2 V, 3 V	1000			ns

(1) The temperature sensor is provided by the REF module. See the REF module parametric, I<sub>REF+</sub>, regarding the current consumption of the temperature sensor.

(2) The temperature sensor offset can be significant. A single-point calibration is recommended in order to minimize the offset error of the built-in temperature sensor. The TLV structure contains calibration values for 30°C ± 3°C and 85°C ± 3°C for each of the available reference voltage levels. The sensor voltage can be computed as V<sub>SENSE</sub> = TC<sub>SENSOR</sub> \* (Temperature,°C) + V<sub>SENSOR</sub>, where TC<sub>SENSOR</sub> and V<sub>SENSOR</sub> can be computed from the calibration values for higher accuracy. See also the MSP430x5xx and MSP430x6xx Family User's Guide (SLAU208).

(3) The typical equivalent impedance of the sensor is 51 k $\Omega$ . The sample time required includes the sensor-on time t<sub>SENSOR(on)</sub>.

(4) The on-time t<sub>VMID(on)</sub> is included in the sampling time t<sub>VMID(sample)</sub>; no additional on time is needed.



Figure 17. Typical Temperature Sensor Voltage





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#### **REF, External Reference**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)<sup>(1)</sup>

	PARAMETER	TEST CONDITIONS	V <sub>cc</sub>	MIN	TYP MAX	UNIT
V <sub>eREF+</sub>	Positive external reference voltage input	$V_{eREF+} > V_{REF}/V_{eREF-}$ <sup>(2)</sup>		1.4	$AV_{CC}$	V
V <sub>REF-</sub> /V <sub>eREF-</sub>	Negative external reference voltage input	$V_{eREF+} > V_{REF}/V_{eREF-}$ <sup>(3)</sup>		0	1.2	V
(V <sub>eREF+</sub> - V <sub>REF-</sub> /V <sub>eREF-</sub> )	Differential external reference voltage input	$V_{eREF+} > V_{REF}/V_{eREF-}$ <sup>(4)</sup>		1.4	$AV_{CC}$	V
Iveref+, Ivref-/veref-	Static input ourset	$\begin{array}{l} 1.4 \ V \leq V_{eREF+} \leq V_{AVCC}, \\ V_{eREF-} = 0 \ V, \ f_{ADC12CLK} = 5 \ MHz, \\ ADC12SHTx = 1h, \\ Conversion \ rate \ 200 \ ksps \end{array}$	2.2 V, 3 V	-26	26	μA
		$ \begin{array}{l} 1.4 \hspace{0.1cm} V \leq V_{eREF+} \leq V_{AVCC}, \\ V_{eREF-} = 0 \hspace{0.1cm} V, \hspace{0.1cm} f_{ADC12CLK} = 5 \hspace{0.1cm} MHz, \\ ADC12SHTx = 8h, \\ Conversion \hspace{0.1cm} rate \hspace{0.1cm} 20 \hspace{0.1cm} ksps \end{array} $	2.2 V, 3 V	-1	1	μA
C <sub>VREF+/-</sub>	Capacitance at VREF+ or VREF- terminal			<sup>(5)</sup> 10		μF

(1) The external reference is used during ADC conversion to charge and discharge the capacitance array. The input capacitance, C<sub>i</sub>, is also the dynamic load for an external reference during conversion. The dynamic impedance of the reference supply should follow the recommendations on analog-source impedance to allow the charge to settle for 12-bit accuracy.

(2) The accuracy limits the minimum positive external reference voltage. Lower reference voltage levels may be applied with reduced accuracy requirements.

(3) The accuracy limits the maximum negative external reference voltage. Higher reference voltage levels may be applied with reduced accuracy requirements.

(4) The accuracy limits minimum external differential reference voltage. Lower differential reference voltage levels may be applied with reduced accuracy requirements.

(5) Two decoupling capacitors, 10µF and 100nF, should be connected to VREF to decouple the dynamic current required for an external reference source if it is used for the ADC12\_A. See also the *MSP430x5xx and MSP430x6xx Family User's Guide* (SLAU208).



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# **REF, Built-In Reference**

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over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)<sup>(1)</sup>

	PARAMETER	TEST CONDITIONS	V <sub>cc</sub>	MIN	TYP	MAX	UNIT
		REFVSEL = $\{2\}$ for 2.5 V, REFON = REFOUT = 1, I <sub>VREF+</sub> = 0 A	3 V	2.4625	2.50	2.5375	
V <sub>REF+</sub>	Positive built-in reference voltage output	$\begin{array}{l} REFVSEL = \{1\} \text{ for } 2.0 \text{ V}, \\ REFON = REFOUT = 1, I_{VREF+} = 0 \text{ A} \end{array}$	3 V	1.9503	1.98	2.0097	V
		REFVSEL = $\{0\}$ for 1.5 V, REFON = REFOUT = 1, I <sub>VREF+</sub> = 0 A	2.2 V/ 3 V	1.4677	1.49	1.5124	
	AV <sub>cc</sub> minimum voltage.	REFVSEL = {0} for 1.5 V		2.2			
AV <sub>CC(min)</sub>	Positive built-in reference	REFVSEL = {1} for 2.0 V		2.3			V
	active	REFVSEL = {2} for 2.5 V		2.8			
		ADC12SR = $1^{(4)}$ , REFON = 1, REFOUT = 0, REFBURST = 0	3 V		70	100	μA
I <sub>REF+</sub>	Operating supply current into	ADC12SR = $1^{(4)}$ , REFON = 1, REFOUT = 1, REFBURST = 0	3 V		0.45	0.75	mA
	AVCC terminal <sup>(2) (3)</sup>	ADC12SR = $0^{(4)}$ , REFON = 1, REFOUT = 0, REFBURST = 0	3 V		210	310	μA
		ADC12SR = $0^{(4)}$ , REFON = 1, REFOUT = 1, REFBURST = $0$	3 V		0.95	1.7	mA
I <sub>L(VREF+)</sub>	Load-current regulation, VREF+ terminal <sup>(5)</sup>	$\begin{array}{l} REFVSEL=(0,1,2),\\ I_{VREF^+}=+10\;\muA\text{-}1000\;\muA,\\ AV_{CC}=AV_{CC}\;(\text{min})\;\text{for each reference level},\\ REFVSEL=(0,1,2\},\;REFON=REFOUT=1 \end{array}$				2500	μV/mA
C <sub>VREF+</sub>	Capacitance at VREF+ terminals	REFON = REFOUT = 1		20		100	pF
TC <sub>REF+</sub>	Temperature coefficient of built-in reference <sup>(6)</sup>	I <sub>VREF+</sub> = 0 A, REFVSEL = (0, 1, 2}, REFON = 1, REFOUT = 0 or 1			30	50	ppm/ °C
PSRR_DC	Power supply rejection ratio (DC)				120	300	μV/V
PSRR_AC	Power supply rejection ratio (AC)				6.4		mV/V
tsettle	Settling time of reference	$\begin{array}{l} AV_{CC} = AV_{CC} \; (\text{min}) \; \text{-} \; AV_{CC(\text{max})}, \\ \text{REFVSEL} = (0,  1,  2\}, \; \text{REFOUT} = 0, \\ \text{REFON} = 0 \rightarrow 1 \end{array}$			75		
	voltage <sup>(7)</sup>	$\begin{array}{l} AV_{CC} = AV_{\overline{CC}\ (min)} - AV_{CC(max)},\\ C_{VREF} = C_{VREF}(max),\\ REFVSEL = \{0, 1, 2\}, REFOUT = 1,\\ REFON = 0 \rightarrow 1 \end{array}$			75		μs

The reference is supplied to the ADC by the REF module and is buffered locally inside the ADC. The ADC uses two internal buffers, one (1) smaller and one larger, for driving the VREF+ terminal. When REFOUT = 1, the reference is available at the VREF+ terminal and is used as the reference for the conversion and utilizes the larger buffer. When REFOUT = 0, the reference is only used as the reference for the conversion and utilizes the smaller buffer.

The internal reference current is supplied via terminal AVCC. Consumption is independent of the ADC12ON control bit, unless a (2) conversion is active. REFOUT = 0 represents the current contribution of the smaller buffer. REFOUT = 1 represents the current contribution of the larger buffer without external load.

The temperature sensor is provided by the REF module. Its current is supplied via terminal AVCC and is equivalent to IREF+ with (3) REFON =1 and REFOUT = 0.

For devices without the ADC12, the parametric with ADC12SR = 0 are applicable.

Contribution only due to the reference and buffer including package. This does not include resistance due to PCB trace, etc. Calculated using the box method:  $(MAX(-40 \text{ to } 85^{\circ}C) - MIN(-40 \text{ to } 85^{\circ}C)) / MIN(-40 \text{ to } 85^{\circ}C) / (85^{\circ}C - (-40^{\circ}C))$ . (5)

(6)

The condition is that the error in a conversion started after t<sub>REFON</sub> is less than ±0.5 LSB. The settling time depends on the external (7)capacitive load when REFOUT = 1.



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#### **Comparator B**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	Vcc	MIN	TYP	MAX	UNIT
V <sub>CC</sub>	Supply voltage			1.8		3.6	V
			1.8 V			40	
		CBPWRMD = 00	2.2 V		30	50	
I <sub>AVCC_COMP</sub>	Comparator operating supply current into		3 V		40	65	μA
		CBPWRMD = 01	2.2/3 V		10	30	
		CBPWRMD = 10	2.2/3 V		0.1	0.5	
I <sub>AVCC_REF</sub>	Quiescent current of local reference voltage amplifier into AVCC	CBREFACC = 1, CBREFLx = 01				22	μA
V <sub>IC</sub>	Common mode input range			0		V <sub>CC</sub> -1	V
V	Input offect veltoge	CBPWRMD = 00				±20	mV
VOFFSET	Input onset voltage	CBPWRMD = 01, 10				±10	mV
C <sub>IN</sub>	Input capacitance				5		pF
R <sub>SIN</sub>	Sorias input registance	ON, switch closed			3	4	kΩ
	Selles input resistance	OFF, switch opened		30			MΩ
		CBPWRMD = 00, CBF = 0				450	ns
t <sub>PD</sub>	Propagation delay, response time	CBPWRMD = 01, CBF = 0				600	ns
		CBPWRMD = 10, CBF = 0				50	μs
		$\begin{array}{l} CBPWRMD = 00,  CBON = 1, \\ CBF = 1,  CBFDLY = 00 \end{array}$		0.35	0.6	1.0	μs
	Propagation delay with filter active	CBPWRMD = 00, CBON = 1, CBF = 1, CBFDLY = 01		0.6	1.0	1.8	μs
<sup>t</sup> PD,filter		CBPWRMD = 00, CBON = 1, CBF = 1, CBFDLY = 10		1.0	1.8	3.4	μs
		CBPWRMD = 00, CBON = 1, CBF = 1, CBFDLY = 11		1.8	3.4	6.5	μs
t <sub>EN_CMP</sub>	Comparator enable time, settling time	CBON = 0 to CBON = 1 CBPWRMD = 00, 01, 10			1	2	μs
t <sub>EN_REF</sub>	Resistor reference enable time	CBON = 0 to CBON = 1			1	1.5	μs
V <sub>CB_REF</sub>	Reference voltage for a given tap	VIN = reference into resistor ladder (n = 0 to 31)			VIN × (n+1) / 32		V



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#### **Flash Memory**

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over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	ТҮР	MAX	UNIT
DV <sub>CC(PGM/ERASE)</sub>	Program or erase supply voltage		1.8		3.6	V
I <sub>PGM</sub>	Average supply current from DVCC during program			3	5	mA
I <sub>ERASE</sub>	Average supply current from DVCC during erase			6	11	mA
I <sub>MERASE</sub> , I <sub>BANK</sub>	Average supply current from DVCC during mass erase or bank erase			6	11	mA
t <sub>CPT</sub>	Cumulative program time	See (1)			16	ms
	Program and erase endurance		10 <sup>4</sup>	10 <sup>5</sup>		cycles
t <sub>Retention</sub>	Data retention duration	T <sub>J</sub> = 25°C	100			years
t <sub>Word</sub>	Word or byte program time	See (2)	64		85	μs
t <sub>Block, 0</sub>	Block program time for first byte or word	See (2)	49		65	μs
t <sub>Block, 1-(N-1)</sub>	Block program time for each additional byte or word, except for last byte or word	See (2)	37		49	μs
t <sub>Block, N</sub>	Block program time for last byte or word	See (2)	55		73	μs
t <sub>Erase</sub>	Erase time for segment, mass erase, and bank erase (when available)	See (2)	23		32	ms
f <sub>MCLK,MGR</sub>	MCLK frequency in marginal read mode (FCTL4.MGR0 = 1 or FCTL4. MGR1 = 1)		0		1	MHz

(1) The cumulative program time must not be exceeded when writing to a 128-byte flash block. This parameter applies to all programming methods: individual word/byte write and block write modes.

(2) These values are hardwired into the flash controller's state machine.

#### JTAG and Spy-Bi-Wire Interface

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

	PARAMETER	V <sub>cc</sub>	MIN	TYP	MAX	UNIT
f <sub>SBW</sub>	Spy-Bi-Wire input frequency	2.2 V, 3 V	0		20	MHz
t <sub>SBW,Low</sub>	Spy-Bi-Wire low clock pulse length	2.2 V, 3 V	0.025		15	μs
t <sub>SBW, En</sub>	Spy-Bi-Wire enable time, TEST high to acceptance of first clock edge <sup>(1)</sup>	2.2 V, 3 V			1	μs
t <sub>SBW,Rst</sub>	Spy-Bi-Wire return to normal operation time		15		100	μs
f <sub>TCK</sub>	TCK input frequency, 4-wire JTAG <sup>(2)</sup>		0		5	MHz
			0		10	MHz
R <sub>internal</sub>	Internal pulldown resistance on TEST	2.2 V, 3 V	45	60	80	kΩ

 Tools accessing the Spy-Bi-Wire interface must wait for the t<sub>SBW,En</sub> time after pulling the TEST/SBWTCK pin high before applying the first SBWTCK clock edge.

(2) f<sub>TCK</sub> may be restricted to meet the timing requirements of the module selected.



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# **INPUT/OUTPUT SCHEMATICS**

# Port P1, P1.0 to P1.7, Input/Output With Schmitt Trigger





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			CONTROL BI	TS/SIGNALS
PIN NAME (P1.x)	x	FUNCTION	P1DIR.x	P1SEL.x
P1.0/TA0CLK/ACLK	0	P1.0 (I/O)	l: 0; O: 1	0
		TAOCLK	0	1
		ACLK	1	1
P1.1/TA0.0	1	P1.1 (I/O)	I: 0; O: 1	0
		TA0.CCI0A	0	1
		TA0.0	1	1
P1.2/TA0.1	2	P1.2 (I/O)	I: 0; O: 1	0
		TA0.CCI1A	0	1
		TA0.1	1	1
P1.3/TA0.2	3	P1.3 (I/O)	I: 0; O: 1	0
		TA0.CCI2A	0	1
		TA0.2	1	1
P1.4/TA0.3	4	P1.4 (I/O)	I: 0; O: 1	0
		TA0.CCI3A	0	1
		TA0.3	1	1
P1.5/TA0.4	5	P1.5 (I/O)	I: 0; O: 1	0
		TA0.CCI4A	0	1
		TA0.4	1	1
P1.6/TA1CLK/CBOUT	6	P1.6 (I/O)	I: 0; O: 1	0
		TA1CLK	0	1
		CBOUT comparator B	1	1
P1.7/TA1.0	7	P1.7 (I/O)	I: 0; O: 1	0
		TA1.CCI0A	0	1
		TA1.0	1	1

Product Folder Links: MSP430F5342 MSP430F5341 MSP430F5340



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#### Table 45. Port P2 (P2.7) Pin Functions

PIN NAME (P2.x)		FUNCTION	CONTROL BITS/SIGNALS <sup>(1)</sup>		
		FUNCTION	P2DIR.x	P2SEL.x	
P2.7/UCB0STE/UCA0CLK	7	P2.7 (I/O)	I: 0; O: 1	0	
		UCB0STE/UCA0CLK <sup>(2) (3)</sup>	Х	1	

(1) X = Don't care

(2) The pin direction is controlled by the USCI module.

(3) UCA0CLK function takes precedence over UCB0STE function. If the pin is required as UCA0CLK input or output, USCI B0 is forced to 3-wire SPI mode if 4-wire SPI mode is selected.



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#### Port P3, P3.0 to P3.4, Input/Output With Schmitt Trigger



#### Table 46. Port P3 (P3.0 to P3.4) Pin Functions

		EUNCTION	CONTROL BITS/SIGNALS <sup>(1)</sup>			
PIN NAME (P3.X)	x	FUNCTION	P3DIR.x	P3SEL.x		
P3.0/UCB0SIMO/UCB0SDA	0	P3.0 (I/O)	I: 0; O: 1	0		
		UCB0SIMO/UCB0SDA <sup>(2)</sup> (3)	Х	1		
P3.1/UCB0SOMI/UCB0SCL	1	P3.1 (I/O)	I: 0; O: 1	0		
		UCB0SOMI/UCB0SCL <sup>(2)</sup> (3)	Х	1		
P3.2/UCB0CLK/UCA0STE	2	P3.2 (I/O)	I: 0; O: 1	0		
		UCB0CLK/UCA0STE <sup>(2) (4)</sup>	Х	1		
P3.3/UCA0TXD/UCA0SIMO	3	P3.3 (I/O)	I: 0; O: 1	0		
		UCA0TXD/UCA0SIMO <sup>(2)</sup>	Х	1		
P3.4/UCA0RXD/UCA0SOMI	4	P3.4 (I/O)	I: 0; O: 1	0		
		UCA0RXD/UCA0SOMI <sup>(2)</sup>	х	1		

X = Don't care (1)

The pin direction is controlled by the USCI module. (2)

(3) (4)

If the I2C functionality is selected, the output drives only the logical 0 to V<sub>SS</sub> level. UCB0CLK function takes precedence over UCA0STE function. If the pin is required as UCB0CLK input or output, USCI A0 is forced to 3-wire SPI mode if 4-wire SPI mode is selected.



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# Port P4, P4.0 to P4.7, Input/Output With Schmitt Trigger



#### Table 47. Port P4 (P4.0 to P4.7) Pin Functions

		FUNCTION	CONTROL BITS/SIGNALS <sup>(1)</sup>					
PIN NAME (P4.X)	X	FUNCTION	P4DIR.x <sup>(2)</sup>	P4SEL.x	P4MAPx			
P4.0/P4MAP0	0	P4.0 (I/O)	I: 0; O: 1	0	Х			
		Mapped secondary digital function	Х	1	≤ 30			
P4.1/P4MAP1	1	P4.1 (I/O)	I: 0; O: 1	0	Х			
		Mapped secondary digital function	Х	1	≤ 30			
P4.2/P4MAP2	2	P4.2 (I/O)	I: 0; O: 1	0	Х			
		Mapped secondary digital function	Х	1	≤ 30			
P4.3/P4MAP3	3	P4.3 (I/O)	I: 0; O: 1	0	Х			
		Mapped secondary digital function	Х	1	≤ 30			
P4.4/P4MAP4	4	P4.4 (I/O)	I: 0; O: 1	0	Х			
		Mapped secondary digital function	Х	1	≤ 30			
P4.5/P4MAP5	5	P4.5 (I/O)	I: 0; O: 1	0	Х			
		Mapped secondary digital function	Х	1	≤ 30			
P4.6/P4MAP6	6	P4.6 (I/O)	I: 0; O: 1	0	Х			
		Mapped secondary digital function	Х	1	≤ 30			
P4.7/P4MAP7	7	P4.7 (I/O)	I: 0; O: 1	0	х			
		Mapped secondary digital function	Х	1	≤ 30			

(1) X = Don't care

(2) The direction of some mapped secondary functions are controlled directly by the module. See Table 8 for specific direction control information of mapped secondary functions.



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Port P5, P5.0 and P5.1, Input/Output With Schmitt Trigger

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#### Pad Logic to/from Reference to ADC12 INCHx = xP5REN.x ■ D\ 0 D١ P5DIR.x P5OUT.x 0 From module P5.0/A8/VREF+/VeREF+ P5DS.x P5.1/A9/VREF-/VeREF-P5SEL.x 0: Low drive 1: High drive P5IN.x Bus EN Keeper D To module

#### Table 48. Port P5 (P5.0 and P5.1) Pin Functions

		FUNCTION	CONTROL BITS/SIGNALS <sup>(1)</sup>			
FIN NAME (F3.X)	×		P5DIR.x	P5SEL.x	REFOUT	
P5.0/A8/VREF+/VeREF+	0	P5.0 (I/O) <sup>(2)</sup>	I: 0; O: 1	0	Х	
		A8/VeREF+ <sup>(3)</sup>	Х	1	0	
		A8/VREF+ <sup>(4)</sup>	Х	1	1	
P5.1/A9/VREF-/VeREF-	1	P5.1 (I/O) <sup>(2)</sup>	I: 0; O: 1	0	Х	
		A9/VeREF- <sup>(5)</sup>	Х	1	0	
		A9/VREF- <sup>(6)</sup>	Х	1	1	

(1)X = Don't care

Default condition (2)

Setting the P5SEL.0 bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying (3) analog signals. An external voltage can be applied to VeREF+ and used as the reference for the ADC12\_A. Channel A8, when selected with the INCHx bits, is connected to the VREF+/VeREF+ pin.

(4) Setting the P5SEL.0 bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. The VREF+ reference is available at the pin. Channel A8, when selected with the INCHx bits, is connected to the VREF+/VeREF+ pin.

Setting the P5SEL1 bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying (5) analog signals. An external voltage can be applied to VeREF- and used as the reference for the ADC12\_A. Channel A9, when selected with the INCHx bits, is connected to the VREF-/VeREF- pin.

Setting the P5SEL.1 bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying (6) analog signals. The VREF- reference is available at the pin. Channel A9, when selected with the INCHx bits, is connected to the VREF-/VeREF- pin.

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#### Port P5, P5.2, Input/Output With Schmitt Trigger





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#### Table 49. Port P5 (P5.2, P5.3) Pin Functions

		EUNCTION	CONTROL BITS/SIGNALS <sup>(1)</sup>					
PIN NAME (PS.X)	×	FUNCTION	P5DIR.x	P5SEL.2	P5SEL.3	XT2BYPASS		
P5.2/XT2IN	2	P5.2 (I/O)	I: 0; O: 1	0	Х	Х		
		XT2IN crystal mode <sup>(2)</sup>	Х	1	Х	0		
		XT2IN bypass mode <sup>(2)</sup>	Х	1	Х	1		
P5.3/XT2OUT	3	P5.3 (I/O)	I: 0; O: 1	0	х	Х		
		XT2OUT crystal mode <sup>(3)</sup>	Х	1	Х	0		
		P5.3 (I/O) <sup>(3)</sup>	Х	1	Х	1		

(1) X = Don't care

(2) Setting P5SEL.2 causes the general-purpose I/O to be disabled. Pending the setting of XT2BYPASS, P5.2 is configured for crystal mode or bypass mode.

(3) Setting PSSEL.2 causes the general-purpose I/O to be disabled in crystal mode. When using bypass mode, P5.3 can be used as general-purpose I/O.


# MSP430F5342, MSP430F5341, MSP430F5340



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### Port P5, P5.4 and P5.5 Input/Output With Schmitt Trigger







## MSP430F5342, MSP430F5341, MSP430F5340

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Table 50. Port P5 (P5.4 and P5.5) Pin Functions

PIN NAME (P5.x)	~	FUNCTION	CONTROL BITS/SIGNALS <sup>(1)</sup>						
FIN NAME (F5.X)	×	FUNCTION	P5DIR.x	P5SEL.4	P5SEL.5	XT1BYPASS			
P5.4/XIN	4	P5.4 (I/O)	I: 0; O: 1	0	Х	Х			
		XIN crystal mode <sup>(2)</sup>	Х	1	Х	0			
		XIN bypass mode <sup>(2)</sup>	Х	1	Х	1			
P5.5/XOUT	5	P5.5 (I/O)	I: 0; O: 1	0	Х	Х			
		XOUT crystal mode <sup>(3)</sup>	Х	1	Х	0			
		P5.5 (I/O) <sup>(3)</sup>	Х	1	Х	1			

X = Don't care (1)

(2) Setting P5SEL.4 causes the general-purpose I/O to be disabled. Pending the setting of XT1BYPASS, P5.4 is configured for crystal mode or bypass mode.

Setting P5SEL.4 causes the general-purpose I/O to be disabled in crystal mode. When using bypass mode, P5.5 can be used as (3) general-purpose I/O.



## MSP430F5342, MSP430F5341, MSP430F5340



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### Port P5, P5.7, Input/Output With Schmitt Trigger



#### Table 51. Port P5 (P5.7) Pin Functions

PIN NAME (P5.x)	~	EUNCTION	CONTROL BITS/SIGNALS			
	X	FUNCTION	P5DIR.x	P5SEL.x		
P5.7/TB0.1	7	TB0.CCI1A	0	1		
		TB0.1	1	1		



TEXAS INSTRUMENTS

### MSP430F5342, MSP430F5341, MSP430F5340

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#### Port P6, P6.1 to P6.5, Input/Output With Schmitt Trigger Pad Logic to ADC12 INCHx = xto Comparator\_B from Comparator\_B CBPD.x P6REN.x DVSS C DVCC P6DIR.x Direction 0: Input 1: Output P6OUT.x 0 From module 1 P6.1/CB1/A1 I P6DS.x P6.2/CB2/A2 P6SEL.x 0: Low drive P6.3/CB3/A3 1: High drive I P6.4/CB4/A4 P6IN.x < P6.5/CB5/A5 Bus ΕN Keeper To module D

### Table 52. Port P6 (P6.1 to P6.5) Pin Functions

		FUNCTION	CONTROL BITS/SIGNALS <sup>(1)</sup>				
PIN NAME (PO.X)	x	FUNCTION	P6DIR.x	P6SEL.x	CBPD		
P6.1/CB1/A1	1	P6.1 (I/O)	I: 0; O: 1	0	0		
		A1	Х	1	Х		
		CB1 <sup>(2)</sup>	Х	Х	1		
P6.2/CB2/A2	2	P6.2 (I/O)	I: 0; O: 1	0	0		
		A2	Х	1	Х		
		CB2 <sup>(2)</sup>	Х	Х	1		
P6.3/CB3/A3	3	P6.3 (I/O)	I: 0; O: 1	0	0		
		A3	Х	1	Х		
		CB3 <sup>(2)</sup>	х	х	1		

(1) X = Don't care

(2) Setting the CBPD.x bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. Selecting the CBx input pin to the comparator multiplexer with the CBx bits automatically disables output driver and input buffer for that pin, regardless of the state of the associated CBPD.x bit.

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		Table 52. Fort F0 (F0.1 to F0.5) Fill Functions	(continued)							
		FUNCTION	CONTROL BITS/SIGNA							
PIN NAME (P6.X)	x	FUNCTION	CONTROL BI           FUNCTION         P6DIR.x         P6S           I: 0; 0: 1         X         X           X         I: 0; 0: 1         X           I: 0; 0: 1         X         X           X         X         X           X         X         X           X         X         X           X         X         X           X         X         X	P6SEL.x	CBPD					
P6.4/CB4/A4	4	P6.4 (I/O)	I: 0; O: 1	0	0					
		A4	Х	1	Х					
		CB4 <sup>(2)</sup>	Х	х	1					
P6.5/CB5/A5	5	P6.5 (I/O)	I: 0; O: 1	0	0					
		A5	Х	1	Х					
		CB5 <sup>(2)</sup>	Х	Х	1					

### Table 52. Port P6 (P6.1 to P6.5) Pin Functions (continued)



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IEXAS INSTRUMENTS

### MSP430F5342, MSP430F5341, MSP430F5340

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### Port J, J.0 JTAG pin TDO, Input/Output With Schmitt Trigger or Output

Port J, J.1 to J.3 JTAG pins TMS, TCK, TDI/TCLK, Input/Output With Schmitt Trigger or Output







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### Table 53. Port PJ (PJ.0 to PJ.3) Pin Functions

PIN NAME (PJ.x)	x	FUNCTION	CONTROL BITS/ SIGNALS <sup>(1)</sup>
			PJDIR.x
PJ.0/TDO	0	PJ.0 (I/O) <sup>(2)</sup>	I: 0; O: 1
		TDO <sup>(3)</sup>	Х
PJ.1/TDI/TCLK	1	PJ.1 (I/O) <sup>(2)</sup>	I: 0; O: 1
		TDI/TCLK <sup>(3) (4)</sup>	Х
PJ.2/TMS	2	PJ.2 (I/O) <sup>(2)</sup>	I: 0; O: 1
		TMS <sup>(3) (4)</sup>	Х
PJ.3/TCK	3	PJ.3 (I/O) <sup>(2)</sup>	I: 0; O: 1
		TCK <sup>(3) (4)</sup>	Х

X = Don't care (1)

Default condition

The pin direction is controlled by the JTAG module.

(2) (3) (4) In JTAG mode, pullups are activated automatically on TMS, TCK, and TDI/TCLK. PJREN.x are do not care.



## MSP430F5342, MSP430F5341, MSP430F5340

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### **DEVICE DESCRIPTORS**

Table 54 lists the complete contents of the device descriptor tag-length-value (TLV) structure for each device type.

			Size	'F5342	'F5341	'F5340
	Description	Address	bytes	Value	Value	Value
Info Block	Info length	01A00h	1	06h	06h	06h
	CRC length	01A01h	1	06h	06h	06h
	CRC value	01A02h	2	per unit	per unit	per unit
	Device ID	01A04h	1	1Eh	1Dh	1Ch
	Device ID	01A05h	1	81h	81h	81h
	Hardware revision	01A06h	1	per unit	per unit	per unit
	Firmware revision	01A07h	1	per unit	per unit	per unit
Die Record	Die Record Tag	ord Tag 01A08h 1 0		08h	08h	08h
	Die Record length	01A09h	1	0Ah	0Ah	0Ah
	Lot/Wafer ID	01A0Ah	4	per unit	per unit	per unit
	Die X position	01A0Eh	2	per unit	per unit	per unit
	Die Y position	01A10h	2	per unit	per unit	per unit
	Test results	01A12h	2	per unit	per unit	per unit
ADC12 Calibration	ADC12 Calibration Tag	01A14h	1	11h	11h	11h
	ADC12 Calibration length	01A15h	1	10h	10h	10h
	ADC Gain Factor	01A16h	2	per unit	per unit	per unit
	ADC Offset	01A18h	2	per unit	per unit	per unit
	ADC 1.5-V Reference Temp. Sensor 30°C	01A1Ah	2	per unit	per unit	per unit
	ADC 1.5-V Reference Temp. Sensor 85°C	01A1Ch	2	per unit	per unit	per unit
	ADC 2.0-V Reference Temp. Sensor 30°C	01A1Eh	2	per unit	per unit	per unit
	ADC 2.0-V Reference Temp. Sensor 85°C	01A20h	2	per unit	per unit	per unit
	ADC 2.5-V Reference Temp. Sensor 30°C	01A22h	2	per unit	per unit	per unit
	ADC 2.5-V Reference Temp. Sensor 85°C	01A24h	2	per unit	per unit	per unit
<b>REF</b> Calibration	REF Calibration Tag	01A26h	1	12h	12h	12h
	REF Calibration length	01A27h	1	06h	06h	06h
	REF 1.5-V Reference Factor	01A28h	2	per unit	per unit	per unit
	REF 2.0-V Reference Factor	01A2Ah	2	per unit	per unit	per unit
	REF 2.5-V Reference Factor	01A2Ch	2	per unit	per unit	per unit
Peripheral Descriptor	Peripheral Descriptor Tag	01A2Eh	1	02h	02h	02h
	Peripheral Descriptor Length	01A2Fh	1	5Eh	5Eh	5Eh
	Memory 1		2	08h 8Ah	08h 8Ah	08h 8Ah
	Memory 2		2	0Ch 86h	0Ch 86h	0Ch 86h
	Memory 3		2	0Eh 2Fh	0Eh 2Eh	0Eh 2Dh

Table 54	'F534x	Device	Descriptor	Table <sup>(1)</sup>
1 4 10 0 1		001100	Doooliptoi	IGNIC

(1) NA = Not applicable, blank = unused and reads FFh.





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Table 54. 'F534x Device Descriptor Table <sup>(1)</sup> (continued)										
Description	Address	Size	'F5342	'F5341	'F5340					
Description	Address	bytes	Value	Value	Value					
Memory 4		2	2Ah 22h	22h 95h	2Ah 22h					
Memory 5		1	96h	92h	94h					
delimiter		1	00h	00h	00h					
Peripheral count		1	1Fh	1Fh	1Fh					
MSP430CPUXV2		2	00h 23h	00h 23h	00h 23h					
JTAG		2	00h 09h	00h 09h	00h 09h					
SBW		2	00h 0Fh	00h 0Fh	00h 0Fh					
EEM-L		2	00h 05h	00h 05h	00h 05h					
TI BSL		2	00h FCh	00h FCh	00h FCh					
SFR		2	10h 41h	10h 41h	10h 41h					
РММ		2	02h 30h	02h 30h	02h 30h					
FCTL		2	02h 38h	02h 38h	02h 38h					
CRC16		2	01h 3Ch	01h 3Ch	01h 3Ch					
CRC16_RB		2	00h 3Dh	00h 3Dh	00h 3Dh					
RAMCTL		2	00h 44h	00h 44h	00h 44h					
WDT_A		2	00h 40h	00h 40h	00h 40h					
UCS		2	01h 48h	01h 48h	01h 48h					
SYS		2	02h 42h	02h 42h	02h 42h					
REF		2	03h A0h	03h A0h	03h A0h					
Port Mapping		2	01h 10h	01h 10h	01h 10h					
Port 1/2		2	04h 51h	04h 51h	04h 51h					
Port 3/4		2	02h 52h	02h 52h	02h 52h					
Port 5/6		2	02h 53h	02h 53h	02h 53h					
JTAG		2	0Eh 5Fh	0Eh 5Fh	0Eh 5Fh					
TAO		2	02h 62h	02h 62h	02h 62h					
TA1		2	04h 61h	04h 61h	04h 61h					
ТВО		2	04h 67h	04h 67h	04h 67h					
TA2		2	04h 61h	04h 61h	04h 61h					



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# MSP430F5342, MSP430F5341, MSP430F5340

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	Table 54. 'F534x Dev	vice Descriptor	Table <sup>(1)</sup> (o	(continued)						
	Decemination	Address	Size	'F5342	'F5341	'F5340				
	Description	Address	bytes	Value	Value	Value				
	RTC		2	0Ah 68h	0Ah 68h	0Ah 68h				
	MPY32		2	02h 85h	02h 85h	02h 85h				
	DMA-3		2	04h 47h	04h 47h	04h 47h				
	USCI_A/B		2	0Ch 90h	0Ch 90h	0Ch 90h				
	USCI_A/B		2	04h 90h	04h 90h	04h 90h				
	ADC12_A		2	10h D1h	10h D1h	10h D1h				
	COMP_B		2	1Ch A8h	1Ch A8h	1Ch A8h				
Interrupts	COMP_B		1	A8h	A8h	A8h				
	TB0.CCIFG0		1	64h	64h	64h				
	TB0.CCIFG16		1	65h	65h	65h				
	WDTIFG		1	40h	40h	40h				
	USCI_A0		1	90h	90h	90h				
	USCI_B0		1	91h	91h	91h				
	ADC12_A		1	D0h	D0h	D0h				
	TA0.CCIFG0		1	60h	60h	60h				
	TA0.CCIFG14		1	61h	61h	61h				
	Reserved		1	01h	01h	01h				
	DMA		1	46h	46h	46h				
	TA1.CCIFG0		1	62h	62h	62h				
	TA1.CCIFG12		1	63h	63h	63h				
	P1		1	50h	50h	50h				
	USCI_A1		1	92h	92h	92h				
	USCI_B1		1	93h	93h	93h				
	TA1.CCIFG0		1	66h	66h	66h				
	TA1.CCIFG12		1	67h	67h	67h				
	P2		1	51h	51h	51h				
	RTC_A		1	68h	68h	68h				
	delimiter		1	00h	00h	00h				





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### **REVISION HISTORY**

REVISION	DESCRIPTION
SLAS706	Product Preview release
SLAS706A	Updated Product Preview release
SLAS706B	Production Data release
SLAS706C	<ul> <li>Pinout and Terminal Functions, Added recommendation to connect exposed thermal pad to V<sub>SS</sub>.</li> <li>Terminal Functions, Changed ACLK description (added dividers up to 32).</li> <li>Table 10, Changed SYSRSTIV interrupt event at 1Ch to Reserved.</li> <li>Recommended Operating Conditions, Added note regarding interaction between minimum V<sub>CC</sub> and SVS.</li> <li>12-Bit ADC, Temperature Sensor and Built-In VMID, Changed ADC12 t<sub>SENSOR(sample)</sub> MIN to 100 µs; changed note (2).</li> <li>Table 45 and Table 46, Corrected notes regarding USCI CLK functions taking precedence over USCI STE functions.</li> <li>Port P6, P6.1 to P6.5, Input/Output With Schmitt Trigger, Changed schematic.</li> </ul>
SLAS706D	Recommended Operating Conditions, Added test conditions for typical characteristics. DCO Frequency, Added note (1). Flash Memory, Changed I <sub>ERASE</sub> and I <sub>MERASE</sub> values.
SLAS706E	Added Applications, Development Tools Support, and Device and Development Tool Nomenclature. Table 2, Added note on RST/NMI/SBWTDIO pin about internal pullup resistor. Added Device Descriptors.



16-Jun-2016

#### PACKAGING INFORMATION

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Orderable Device	Status	Package Type	Package	Pins	Package	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Device Marking	Samples
	(1)		Drawing		Qty	(2)	(6)	(3)		(4/5)	
MSP430F5340IRGZR	ACTIVE	VQFN	RGZ	48	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	M430 F5340	Samples
MSP430F5340IRGZT	ACTIVE	VQFN	RGZ	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	M430 F5340	Samples
MSP430F5341IRGZR	ACTIVE	VQFN	RGZ	48	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	M430 F5341	Samples
MSP430F5341IRGZT	ACTIVE	VQFN	RGZ	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	M430 F5341	Samples
MSP430F5342IRGZR	ACTIVE	VQFN	RGZ	48	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	M430 F5342	Samples
MSP430F5342IRGZT	ACTIVE	VQFN	RGZ	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	M430 F5342	Samples

<sup>(1)</sup> The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs. LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect. NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available. OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/(Green conversion plan has not been defined. Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes. Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above. Green (RoHS & no Sh/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device

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(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TEXAS INSTRUMENTS

# PACKAGE MATERIALS INFORMATION

25-Mar-2015

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### TAPE AND REEL INFORMATION





### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal												
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MSP430F5340IRGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2
MSP430F5340IRGZT	VQFN	RGZ	48	250	180.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2
MSP430F5341IRGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2
MSP430F5341IRGZT	VQFN	RGZ	48	250	180.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2
MSP430F5342IRGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2
MSP430F5342IRGZT	VQFN	RGZ	48	250	180.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2



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# PACKAGE MATERIALS INFORMATION

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Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MSP430F5340IRGZR	VQFN	RGZ	48	2500	367.0	367.0	38.0
MSP430F5340IRGZT	VQFN	RGZ	48	250	210.0	185.0	35.0
MSP430F5341IRGZR	VQFN	RGZ	48	2500	367.0	367.0	38.0
MSP430F5341IRGZT	VQFN	RGZ	48	250	210.0	185.0	35.0
MSP430F5342IRGZR	VQFN	RGZ	48	2500	367.0	367.0	38.0
MSP430F5342IRGZT	VQFN	RGZ	48	250	210.0	185.0	35.0



# **MECHANICAL DATA**



NOTES:

- Β. This drawing is subject to change without notice.
  - Quad Flatpack, No-leads (QFN) package configuration. C.
  - The package thermal pad must be soldered to the board for thermal and mechanical performance. D.
  - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions. E.
  - F. Falls within JEDEC MO-220.





# THERMAL PAD MECHANICAL DATA

#### RGZ (S-PVQFN-N48) PLASTIC QUAD FLATPACK NO-LEAD THERMAL INFORMATION This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC). For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com. The exposed thermal pad dimensions for this package are shown in the following illustration. PIN 1 INDICATOR 12 C 0,30 $\Pi \Pi \Pi$ $\overline{U}\overline{U}\overline{U}$ Π Π U 48 13 $\subset$ Exposed Thermal Pad C 2 7 C C $5,15\pm0,10$ C C C C 7 $\subset$ 24 37 IN $\cap \cap$ 36 25 5,15±0,10 -Bottom View Exposed Thermal Pad Dimensions 4206354-2/Z 03/15







# LAND PATTERN DATA

RGZ (S-PVQFN-N48)

PLASTIC QUAD FLATPACK NO-LEAD



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <a href="http://www.ti.com">http://www.ti.com</a>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
- contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations. F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.
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