ISO764xFM Low-Power Quad-Channel Digital Isolators

1 Features

- Signaling Rate: 150 Mbps
- Low Power Consumption, Typical I_{CC} per Channel (3.3-V Supplies):
  - ISO7640FM: 2 mA at 25 Mbps
  - ISO7641FM: 2.4 mA at 25 Mbps
- Low Propagation Delay: 7-ns Typical
- Output Defaults to Low-State in Fail-Safe Mode
- Wide Temperature Range: –40°C to 125°C
- 50-KV/µs Transient Immunity, Typical
- Long Life With SiO_2 Isolation Barrier
- Operates From 2.7-V, 3.3-V, and 5-V Supply and Logic Levels
- Wide Body SOIC-16 Package
- Safety and Regulatory Approvals
  - 6000 V_{PK} / 4243 V_{RMS} for 1 Minute per UL 1577
  - VDE 6000 V_{PK} Transient Overvoltage, 1414 V_{PK} Working Voltage per DIN V VDE V 0884-10 (VDE V 0884-10):2006-12
  - CSA Component Acceptance Notice 5A, IEC 60950-1, IEC 61010-1, and IEC 60601-1 End Equipment Standards
  - TUV 5 KV_{RMS} Reinforced Insulation per EN/UL/CSA 60950-1 and EN/UL/CSA 61010-1
  - CQC Reinforced Insulation per GB4943.1-2011

2 Applications

- Optocoupler Replacement in:
  - Industrial Fieldbus
    - Profibus
    - Modbus
    - DeviceNet™ Data Buses
  - Servo Control Interface
  - Motor Control
  - Power Supplies
  - Battery Packs

3 Description

ISO7640FM and ISO7641FM provide galvanic isolation up to 6 KV_{PK} for 1 minute per UL and VDE. These devices are also certified up to 5-KV_{RMS} Reinforced isolation at a working voltage of 400 V_{RMS} per end equipment standards EN/UL/CSA 60950-1 and 61010-1. ISO7640F and ISO7641F are quad-channel isolators; ISO7640F has four forward and ISO7641F has three forward and one reverse-direction channels. Suffix F indicates that output defaults to Low-state in fail-safe conditions (see Table 4). M-Grade devices are high-speed isolators capable of 150-Mbps data rate with fast propagation delays.

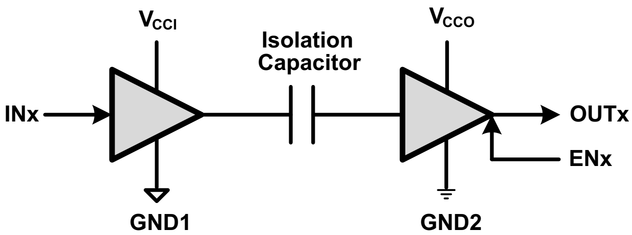
Each isolation channel has a logic input and output buffer separated by a silicon dioxide (SiO_2) insulation barrier. Used in conjunction with isolated power supplies, these devices prevent noise currents on a data bus or other circuits from entering the local ground and interfering with or damaging sensitive circuitry. The devices have TTL input thresholds and can operate from 2.7-V, 3.3-V, and 5-V supplies. All inputs are 5-V tolerant when supplied from 3.3-V or 2.7-V supplies.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
ISO7640FM	SOIC (16)	10.30 mm × 7.50 mm
ISO7641FM		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision F (September 2013) to Revision G	Page
• Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1
• VDE standard changed to DIN V VDE V 0884-10 (VDE V 0884-10):2006-12.	1

Changes from Revision E (January 2013) to Revision F	Page
• Changed the REGULATORY INFORMATION table, TUV column From: Certificate Number: U8V 13 07 77311 009 To: Certificate Number: U8V 13 09 77311 010	23

Changes from Revision D (July 2012) to Revision E	Page
• Changed Z to Undetermined in the OUTPUT (OUTx) column of the FUNCTION TABLE.	25

Changes from Revision C (January 2012) to Revision D **Page**

- Deleted devices: ISO7631FM, ISO7631FC, ISO7640FC, ISO7641FC from the data sheet ... 1
- Changed the Title From: Low Power Triple and Quad Channels Digital Isolators To: Low Power Quad Channels Digital Isolators ... 1
- Deleted devices from the Features List ... 1
- Changed the DESCRIPTION ... 1
- Changed EN1 and EN2 Pin Descriptions ... 5
- Changed the ELECTRICAL, SWITCHING, and SUPPLY CURRENT CHARACTERISTICS tables ... 7
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- Changed the TYPICAL CHARACTERISTICS section ... 17
- Deleted device from the Available Options Table ... 21
- Deleted devices from the TYPICAL SUPPLY CURRENT EQUATIONS section ... 28

Changes from Revision B (December 2011) to Revision C **Page**

- Changed Safety and Regulatory Approvals bullet From: 6000 V_{PK} / 4243 V_{RMS} for 1 Minute per UL1577 (pending) To: 6000 V_{PK} / 4243 V_{RMS} for 1 Minute per UL 1577 (approved) ... 1
- Changed Description text From: The devices have TTL input thresholds and can operate from 2.7 V, 3.3 V and 5 V supplies. To: The devices have TTL input thresholds and can operate from 2.7 V (M-Grade), 3.3 V and 5 V supplies. ... 1
- Changed the ESD standards ... 6
- Changed the typical characteristics section ... 17
- Deleted the Product Preview Note From the Available Options Table ... 21

Changes from Revision A (October 2011) to Revision B **Page**

- Changed feature bullet From: ISO7641FC: 1.2 mA at 10 Mbps To: ISO7641FC: 1.3 mA at 10 Mbps ... 1
- Changed Safety and Regulatory Approvals bullet From: 6 KV_{PK} for 1 Minute per UL1577 and VDE (Pending) To: 6000 V_{PK} / 4243 V_{RMS} for 1 Minute per UL 1577 (pending) ... 1
- Changed Safety and Regulatory Approvals bullet From: To: 6000 V_{PK} / 4243 V_{RMS} for 1 Minute per UL 1577 (approved) . 1
- Changed Safety and Regulatory Approvals bullet From: CSA Component Acceptance Notice 5A, IEC 60601-1 Medical Standard (pending) To: CSA Component Acceptance Notice 5A, IEC 60601-1 Medical Standard (approved) ... 1
- Changed all the ELECTRICAL CHARACTERISTICS tables ... 7
- Changed the SWITCHING CHARACTERISTICS table ISO7640F and ISO7641F C-Grade values ... 9
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- Changed all the SWITCHING CHARACTERISTICS tables ... 14
- Changed the IEC 60664-1 Ratings Table ... 23

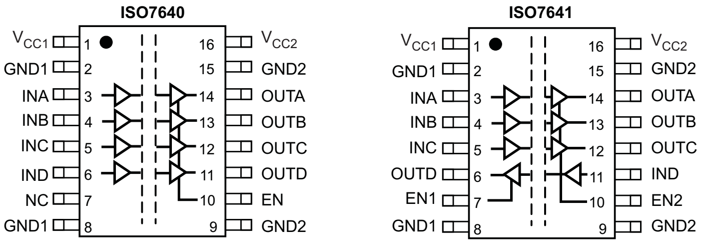
Changes from Original (September 2011) to Revision A **Page**

- Changed Figure 11 - From: 0 V or V_{CC} To: IN = V_{CC} ... 20
- Added Note (1) "Per JEDEC package dimensions" to the IEC INSULATION AND SAFETY-RELATED SPECIFICATIONS FOR DW-16 PACKAGE table ... 20

- Changed L(I01) Min Value From: 8 mm To: 8.3 mm 20
- Changed L(I02) Min Value From: 7.8 mm To: 8.1 mm 20
- Added pinout for ISO7641 and ISO7631 28

5 Pin Configuration and Functions

DW Package
16-Pin SOIC
Top View



Pin Functions

PIN			I/O	DESCRIPTION
NAME	ISO7640	ISO7641		
EN	10	-	I	Enables (when High or Open) or Disables (when Low) OUTA, OUTB, OUTC and OUTD of ISO7640
EN1	-	7	I	Enables (whenHigh or Open) or Disables (when Low) OUTD of ISO7641
EN2	-	10	I	Enables (when High or Open) or Disables (when Low) OUTA, OUTB, and OUTC of ISO7641
GND1	2	2	–	Ground connection for V_{CC1}
	8	8		
GND2	9	9	–	Ground connection for V_{CC2}
	15	15		
INA	3	3	I	Input, channel A
INB	4	4	I	Input, channel B
INC	5	5	I	Input, channel C
IND	6	11	I	Input, channel D
NC	7	-	-	No Connect pins are floating with no internal connection
OUTA	14	14	O	Output, channel A
OUTB	13	13	O	Output, channel B
OUTC	12	12	O	Output, channel C
OUTD	11	6	O	Output, channel D
V_{CC1}	1	1	–	Power supply, V_{CC1}
V_{CC2}	16	16	–	Power supply, V_{CC2}

6 Specifications

6.1 Absolute Maximum Ratings[1]

		MIN	MAX	UNIT
Supply voltage[2]	V_{CC1}, V_{CC2}	–0.5	6	V
Voltage	INx, OUTx, ENx	–0.5	V_{CC} + 0.5[3]	V
Output Current, I_O		–15	15	mA
Maximum junction temperature, T_J			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values except differential I/O bus voltages are with respect to the local ground terminal (GND1 or GND2) and are peak voltage values.
(3) Maximum voltage must not exceed 6 V.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1]	±4000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[2]	±1500	
		Machine model, per JEDEC JESD22-A115-A	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CC1}, V_{CC2}	Supply voltage		2.7		5.5	V
I_{OH}	High-level output current		–4			mA
I_{OL}	Low-level output current				4	mA
V_{IH}	High-level input voltage		2		5.5	V
V_{IL}	Low-level input voltage		0		0.8	V
t_{ui}	Input pulse duration	≥3-V Operation	6.67			ns
		<3-V Operation	10			
1 / t_{ui}	Signaling rate	≥3-V Operation	0		150	Mbps
		<3-V Operation	0		100	
T_J	Junction temperature		–40		136	°C
T_A	Ambient temperature		–40	25	125	°C

6.4 Thermal Information

THERMAL METRIC[1]			ISO76xx DW (SOIC) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance		72	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance		38	
$R_{\theta JB}$	Junction-to-board thermal resistance		39	
ψ_{JT}	Junction-to-top characterization parameter		9.4	
P_D	Maximum Device Power Dissipation	V_{CC1} = V_{CC2} = 5.5V, T_J = 150°C, C_L = 15 pF Input a 75-MHz 50% duty cycle square wave	399	mW

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics: V_{CC1} and V_{CC2} at 5 V ±10%

V_{CC1} and V_{CC2} at 5 V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –4 mA; see Figure 9	V_{CCO} [(1)] –0.8	4.8		V
		I_{OH} = –20 μA; see Figure 9	V_{CCO} [(1)] –0.1	5		
V_{OL}	Low-level output voltage	I_{OL} = 4 mA; see Figure 9		0.2	0.4	V
		I_{OL} = 20 μA; see Figure 9		0	0.1	
$V_{I(HYS)}$	Input threshold voltage hysteresis			450		mV
I_{IH}	High-level input current	V_{IH} = V_{CC} at INx or ENx			10	μA
I_{IL}	Low-level input current	V_{IL} = 0 V at INx or ENx	–10			
CMTI	Common-mode transient immunity	V_I = V_{CC} or 0 V; see Figure 12	25	75		kV/μs

(1) V_{CCO} is the supply voltage, V_{CC1} or V_{CC2}, for the output channel that is being measured.

6.6 Electrical Characteristics: V_{CC1} at 5 V ±10% and V_{CC2} at 3.3 V ±10%

V_{CC1} at 5 V ±10% and V_{CC2} at 3.3 V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –4 mA; see Figure 9	OUTx on V_{CC1} (5V) side	V_{CC1} – 0.8	4.8		V
			OUTx on V_{CC2} (3.3V) side	V_{CC2} – 0.4	3		
		I_{OH} = –20 μA; see Figure 9	OUTx on V_{CC1} (5V) side	V_{CC1} – 0.1	5		
			OUTx on V_{CC2} (3.3V) side	V_{CC2} – 0.1	3.3		
V_{OL}	Low-level output voltage	I_{OL} = 4 mA; see Figure 9			0.2	0.4	V
		I_{OL} = 20 μA; see Figure 9			0	0.1	
$V_{I(HYS)}$	Input threshold voltage hysteresis				430		mV
I_{IH}	High-level input current	V_{IH} = V_{CC} at INx or ENx				10	μA
I_{IL}	Low-level input current	V_{IL} = 0 V at INx or ENx		–10			
CMTI	Common-mode transient immunity	V_I = V_{CC} or 0 V; see Figure 12		25	50		kV/μs

6.7 Electrical Characteristics: V_{CC1} at 3.3 V ±10% and V_{CC2} at 5 V ±10%

V_{CC1} at 3.3 V ±10% and V_{CC2} at 5 V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –4 mA; see Figure 9	OUTx on V_{CC1} (3.3 V) side	V_{CC1}–0.4	3		V
			OUTx on V_{CC2} (5 V) side	V_{CC2}–0.8	4.8		
		I_{OH} = –20 μA; see Figure 9	OUTx on V_{CC1} (3.3 V) side	V_{CC1}–0.1	3.3		
			OUTx on V_{CC2} (5 V) side	V_{CC2}–0.1	5		
V_{OL}	Low-level output voltage	I_{OL} = 4 mA; see Figure 9			0.2	0.4	V
		I_{OL} = 20 μA; see Figure 9			0	0.1	
$V_{I(HYS)}$	Input threshold voltage hysteresis				430		mV
I_{IH}	High-level input current	V_{IH} = V_{CC} at INx or ENx				10	μA
I_{IL}	Low-level input current	V_{IL} = 0 V at INx or ENx		–10			
CMTI	Common-mode transient immunity	V_I = V_{CC} or 0 V; see Figure 12		25	50		kV/μs

6.8 Electrical Characteristics: V_{CC1} and V_{CC2} at 3.3 V ±10%

V_{CC1} and V_{CC2} at 3.3 V ± 10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –4 mA; see Figure 9	V_{CCO} (1) – 0.4	3		V
		I_{OH} = –20 μA; see Figure 9	V_{CCO} (1) – 0.1	3.3		
V_{OL}	Low-level output voltage	I_{OL} = 4 mA; see Figure 9		0.2	0.4	V
		I_{OL} = 20 μA; see Figure 9		0	0.1	
$V_{I(HYS)}$	Input threshold voltage hysteresis			425		mV
I_{IH}	High-level input current	V_{IH} = V_{CC} at INx or ENx			10	μA
I_{IL}	Low-level input current	V_{IL} = 0 V at INx or ENx	–10			
CMTI	Common-mode transient immunity	V_I = V_{CC} or 0 V; see Figure 12	25	50		kV/μs

(1) V_{CCO} is the supply voltage, V_{CC1} or V_{CC2}, for the output channel that is being measured.

6.9 Electrical Characteristics: V_{CC1} and V_{CC2} at 2.7 V

V_{CC1} and V_{CC2} at 2.7 V(1) (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –4 mA; see Figure 9	V_{CCO} (2) – 0.5	2.4		V
		I_{OH} = –20 μA; see Figure 9	V_{CCO} (2) – 0.1	2.7		
V_{OL}	Low-level output voltage	I_{OL} = 4 mA; see Figure 9		0.2	0.4	V
		I_{OL} = 20 μA; see Figure 9		0	0.1	
$V_{I(HYS)}$	Input threshold voltage hysteresis			350		mV
I_{IH}	High-level input current	V_{IH} = V_{CC} at INx or ENx			10	μA
I_{IL}	Low-level input current	V_{IL} = 0 V at INx or ENx	–10			
CMTI	Common-mode transient immunity	V_I = V_{CC} or 0 V; see Figure 12	25	50		kV/μs

(1) For 2.7-V operation, max data rate is 100 Mbps.
(2) V_{CCO} is the supply voltage, V_{CC1} or V_{CC2}, for the output channel that is being measured.

6.10 Supply Current: V_{CC1} and V_{CC2} at 5 V ±10%

V_{CC1} and V_{CC2} at 5 V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
ISO7640FM						
I_{CC1}	Disable	EN = 0 V		0.6	1.2	mA
I_{CC2}				4.5	6.6	
I_{CC1}	DC to 1 Mbps	DC Signal: $V_I = V_{CC}$ or 0 V, AC Signal: All channels switching with square wave clock input; C_L = 15 pF		0.7	1.3	
I_{CC2}				4.6	6.7	
I_{CC1}	10 Mbps			1.1	2	
I_{CC2}				6.6	10.5	
I_{CC1}	25 Mbps			1.9	3	
I_{CC2}				9.7	14.7	
I_{CC1}	150 Mbps			8.2	14.5	
I_{CC2}				35	58	
ISO7641FM						
I_{CC1}	Disable	EN1 = EN2 = 0 V		2.6	4.2	mA
I_{CC2}				4.2	6.8	
I_{CC1}	DC to 1 Mbps	DC Signal: $V_I = V_{CC}$ or 0 V, AC Signal: All channels switching with square wave clock input; C_L = 15 pF		2.7	4.3	
I_{CC2}				4.3	6.9	
I_{CC1}	10 Mbps			3.6	4.9	
I_{CC2}				6	8.2	
I_{CC1}	25 Mbps			5.1	6.6	
I_{CC2}				8.8	11.4	
I_{CC1}	150 Mbps			17	22	
I_{CC2}				31	42	

6.11 Supply Current: V_{CC1} at 5 V ±10% and V_{CC2} at 3.3 V ±10%

V_{CC1} at 5 V ±10% and V_{CC2} at 3.3 V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ISO7640FM						
I_{CC1}	Disable	EN = 0 V		0.6	1.2	mA
I_{CC2}				3.6	5.1	
I_{CC1}	DC to 1 Mbps	DC Signal: V_I = V_{CC} or 0 V, AC Signal: All channels switching with square wave clock input; C_L = 15 pF		0.7	1.3	
I_{CC2}				3.7	5.2	
I_{CC1}	10 Mbps			1.1	2	
I_{CC2}				5	7.1	
I_{CC1}	25 Mbps			1.9	3	
I_{CC2}				6.9	11	
I_{CC1}	150 Mbps			8.2	14.5	
I_{CC2}				24	40	
ISO7641FM						
I_{CC1}	Disable	EN1 = EN2 = 0 V		2.6	4.2	mA
I_{CC2}				3.2	4.9	
I_{CC1}	DC to 1 Mbps	DC Signal: V_I = V_{CC} or 0 V, AC Signal: All channels switching with square wave clock input; C_L = 15 pF		2.7	4.3	
I_{CC2}				3.3	5	
I_{CC1}	10 Mbps			3.6	4.9	
I_{CC2}				4.4	5.8	
I_{CC1}	25 Mbps			5.1	6.6	
I_{CC2}				6.1	7.6	
I_{CC1}	150 Mbps			17	22	
I_{CC2}				20.6	26.5	

6.12 Supply Current: V_{CC1} at 3.3 V ±10% and V_{CC2} at 5 V ±10%

V_{CC1} at 3.3 V ±10% and V_{CC2} at 5 V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
ISO7640FM						
I_{CC1}	Disable	EN = 0 V		0.35	0.7	mA
I_{CC2}				4.5	6.6	
I_{CC1}	DC to 1 Mbps	DC Signal: $V_I = V_{CC}$ or 0 V, AC Signal: All channels switching with square wave clock input; C_L = 15 pF		0.4	0.8	
I_{CC2}				4.6	6.7	
I_{CC1}	10 Mbps			0.7	1.2	
I_{CC2}				6.6	10.5	
I_{CC1}	25 Mbps			1.1	2	
I_{CC2}				9.7	14.7	
I_{CC1}	150 Mbps			5	8.5	
I_{CC2}				35	58	
ISO7641FM						
I_{CC1}	Disable	EN1 = EN2 = 0 V		1.9	2.9	mA
I_{CC2}				4.2	6.8	
I_{CC1}	DC to 1 Mbps	DC Signal: $V_I = V_{CC}$ or 0 V, AC Signal: All channels switching with square wave clock input; C_L = 15 pF		2	3	
I_{CC2}				4.3	6.9	
I_{CC1}	10 Mbps			2.5	3.5	
I_{CC2}				6	8.2	
I_{CC1}	25 Mbps			3.4	4.5	
I_{CC2}				8.8	11.4	
I_{CC1}	150 Mbps			10.5	14.5	
I_{CC2}				31	42	

6.13 Supply Current: V_{CC1} and V_{CC2} at 3.3 V ±10%

V_{CC1} and V_{CC2} at 3.3 V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ISO7640FM						
I_{CC1}	Disable	EN = 0 V		0.35	0.7	mA
I_{CC2}				3.6	5.1	
I_{CC1}	DC to 1 Mbps	DC Signal: $V_I = V_{CC}$ or 0 V, AC Signal: All channels switching with square wave clock input; C_L = 15 pF		0.4	0.8	
I_{CC2}				3.7	5.2	
I_{CC1}	10 Mbps			0.7	1.2	
I_{CC2}				5	7.1	
I_{CC1}	25 Mbps			1.1	2	
I_{CC2}				6.9	11	
I_{CC1}	150 Mbps			5	8.5	
I_{CC2}				24	40	
ISO7641FM						
I_{CC1}	Disable	EN1 = EN2 = 0 V		1.9	2.9	mA
I_{CC2}				3.2	4.9	
I_{CC1}	DC to 1 Mbps	DC Signal: $V_I = V_{CC}$ or 0 V, AC Signal: All channels switching with square wave clock input; C_L = 15 pF		2	3	
I_{CC2}				3.3	5	
I_{CC1}	10 Mbps			2.5	3.5	
I_{CC2}				4.4	5.8	
I_{CC1}	25 Mbps			3.4	4.5	
I_{CC2}				6.1	7.6	
I_{CC1}	150 Mbps			10.5	14.5	
I_{CC2}				20.6	26.5	

6.14 Supply Current: V_{CC1} and V_{CC2} at 2.7 V

V_{CC1} and V_{CC2} at 2.7 V (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ISO7640FM						
I_{CC1}	Disable	EN = 0 V		0.2	0.6	mA
I_{CC2}				3.3	5	
I_{CC1}	DC to 1 Mbps	DC Signal: $V_I = V_{CC}$ or 0 V, AC Signal: All channels switching with square wave clock input; C_L = 15 pF		0.2	0.7	
I_{CC2}				3.4	5.1	
I_{CC1}	10 Mbps			0.4	1.1	
I_{CC2}				4.4	6.8	
I_{CC1}	25 Mbps			0.8	1.8	
I_{CC2}				6	9.5	
I_{CC1}	100 Mbps			2.7	5	
I_{CC2}				14.2	21	
ISO7641FM						
I_{CC1}	Disable	EN1 = EN2 = 0 V		1.6	2.4	mA
I_{CC2}				2.8	4.1	
I_{CC1}	DC to 1 Mbps	DC Signal: $V_I = V_{CC}$ or 0 V, AC Signal: All channels switching with square wave clock input; C_L = 15 pF		1.7	2.5	
I_{CC2}				2.9	4.2	
I_{CC1}	10 Mbps			2.1	3	
I_{CC2}				3.8	5	
I_{CC1}	25 Mbps			2.8	3.8	
I_{CC2}				5.2	6.7	
I_{CC1}	100 Mbps			6.4	7.5	
I_{CC2}				11.8	15.5	

6.15 Switching Characteristics: V_{CC1} and V_{CC2} at 5 V ±10%

V_{CC1} and V_{CC2} at 5 V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See Figure 9	3.5	7	10.5	ns
PWD (1)	Pulse width distortion $\|t_{PHL} – t_{PLH}\|$				2	
$t_{sk(o)}$ (2)	Channel-to-channel output skew time	Same-direction Channels			2	
		Opposite-direction Channels			3	
$t_{sk(pp)}$ (3)	Part-to-part skew time				4.5	
t_r	Output signal rise time	See Figure 9		1.6		ns
t_f	Output signal fall time			1		
t_{PHZ}	Disable Propagation Delay, high-to-high impedance output	See Figure 10		5	16	ns
t_{PLZ}	Disable Propagation Delay, low-to-high impedance output			5	16	
t_{PZH}	Enable Propagation Delay, high impedance-to-high output			4	16	
t_{PZL}	Enable Propagation Delay, high impedance-to-low output			4	16	
t_{fs}	Fail-safe output delay time from input data or power loss	See Figure 11		9.5		μs

(1) Also known as Pulse Skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

6.16 Switching Characteristics: V_{CC1} at 5 V ±10% and V_{CC2} at 3.3 V ±10%

V_{CC1} at 5 V ±10% and V_{CC2} at 3.3 V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See Figure 9	4	8	13	ns
PWD (1)	Pulse width distortion $\|t_{PHL} – t_{PLH}\|$				2	
$t_{sk(o)}$ (2)	Channel-to-channel output skew time	Same-direction Channels			2.5	
		Opposite-direction Channels			3.5	
$t_{sk(pp)}$ (3)	Part-to-part skew time				6	
t_r	Output signal rise time	See Figure 9		2		ns
t_f	Output signal fall time			1.2		
t_{PHZ}	Disable Propagation Delay, high-to-high impedance output	See Figure 10		6.5	17	ns
t_{PLZ}	Disable Propagation Delay, low-to-high impedance output			6.5	17	
t_{PZH}	Enable Propagation Delay, high impedance-to-high output			5.5	17	
t_{PZL}	Enable Propagation Delay, high impedance-to-low output			5.5	17	
t_{fs}	Fail-safe output delay time from input data or power loss	See Figure 11		9.5		μs

(1) Also known as Pulse Skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

6.17 Switching Characteristics: V_{CC1} at 3.3 V ±10% and V_{CC2} at 5 V ±10%

V_{CC1} at 3.3 V ±10% and V_{CC2} at 5 V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See Figure 9	4	7.5	12.5	ns
PWD[1]	Pulse width distortion $\|t_{PHL} – t_{PLH}\|$				2	
$t_{sk(o)}$[2]	Channel-to-channel output skew time	Same-direction Channels			2.5	
		Opposite-direction Channels			3.5	
$t_{sk(pp)}$[3]	Part-to-part skew time				6	
t_r	Output signal rise time	See Figure 9		1.7		ns
t_f	Output signal fall time			1.1		
t_{PHZ}	Disable Propagation Delay, high-to-high impedance output	See Figure 10		5.5	17	ns
t_{PLZ}	Disable Propagation Delay, low-to-high impedance output			5.5	17	
t_{PZH}	Enable Propagation Delay, high impedance-to-high output			4.5	17	
t_{PZL}	Enable Propagation Delay, high impedance-to-low output			4.5	17	
t_{fs}	Fail-safe output delay time from input data or power loss	See Figure 11		9.5		μs

(1) Also known as Pulse Skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

6.18 Switching Characteristics: V_{CC1} and V_{CC2} at 3.3 V ±10%

V_{CC1} and V_{CC2} at 3.3 V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See Figure 9	4	8.5	14	ns
PWD[1]	Pulse width distortion $\|t_{PHL} – t_{PLH}\|$				2	
$t_{sk(o)}$[2]	Channel-to-channel output skew time	Same-direction Channels			3	
		Opposite-direction Channels			4	
$t_{sk(pp)}$[3]	Part-to-part skew time				6.5	
t_r	Output signal rise time	See Figure 9		2		ns
t_f	Output signal fall time			1.3		
t_{PHZ}	Disable Propagation Delay, high-to-high impedance output	See Figure 10		6.5	17	ns
t_{PLZ}	Disable Propagation Delay, low-to-high impedance output			6.5	17	
t_{PZH}	Enable Propagation Delay, high impedance-to-high output			5.5	17	
t_{PZL}	Enable Propagation Delay, high impedance-to-low output			5.5	17	
t_{fs}	Fail-safe output delay time from input data or power loss	See Figure 11		9.2		μs

(1) Also known as Pulse Skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

6.19 Switching Characteristics: V_{CC1} and V_{CC2} at 2.7 V

V_{CC1} and V_{CC2} at 2.7 V (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See Figure 9	5	8	16	ns
PWD(1)	Pulse width distortion $\|t_{PHL} – t_{PLH}\|$	See Figure 9			2.5	ns
$t_{sk(o)}$ (2)	Channel-to-channel output skew time	Same-direction Channels			4	ns
		Opposite-direction Channels			5	ns
$t_{sk(pp)}$ (3)	Part-to-part skew time				8	ns
t_r	Output signal rise time	See Figure 9		2.3		ns
t_f	Output signal fall time	See Figure 9		1.8		ns
t_{PHZ}	Disable Propagation Delay, high-to-high impedance output	See Figure 10		8	18	ns
t_{PLZ}	Disable Propagation Delay, low-to-high impedance output	See Figure 10		8	18	ns
t_{PZH}	Enable Propagation Delay, high impedance-to-high output	See Figure 10		7	18	ns
t_{PZL}	Enable Propagation Delay, high impedance-to-low output	See Figure 10		7	18	ns
t_{fs}	Fail-safe output delay time from input data or power loss	See Figure 11		8.5		μs

(1) Also known as Pulse Skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

6.20 Typical Characteristics

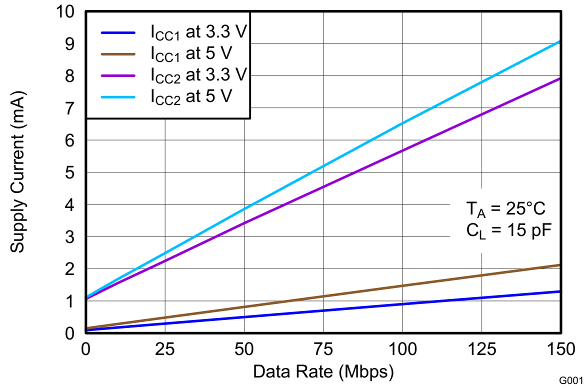


Figure 1. ISO7640FM Supply Current per Channel vs Data Rate

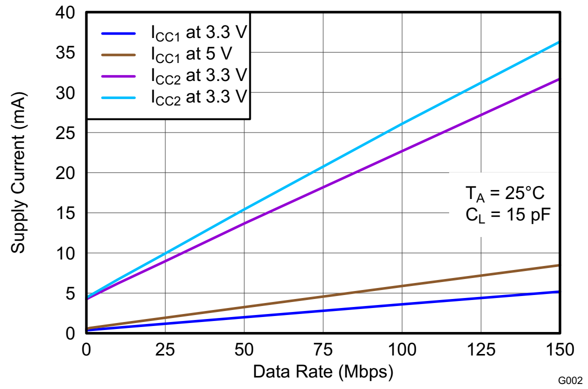


Figure 2. ISO7640FM Supply Current for All Channels vs Data Rate

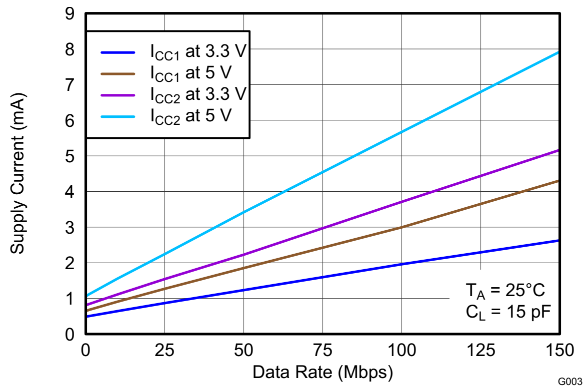


Figure 3. ISO7641FM Supply Current per Channel vs Data Rate

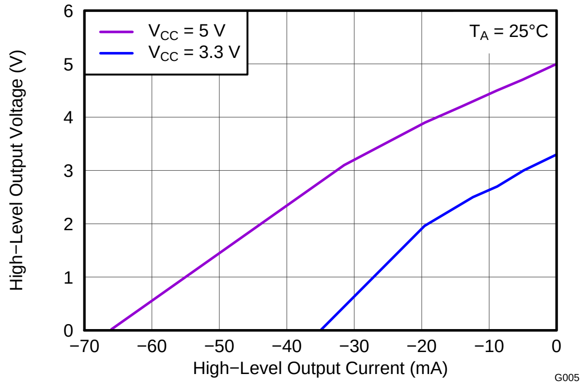


Figure 4. High-Level Output Voltage vs High-Level Output Current

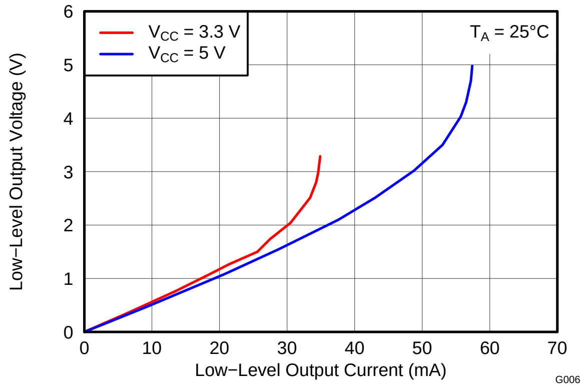


Figure 5. Low-Level Output Voltage vs Low-Level Output Current

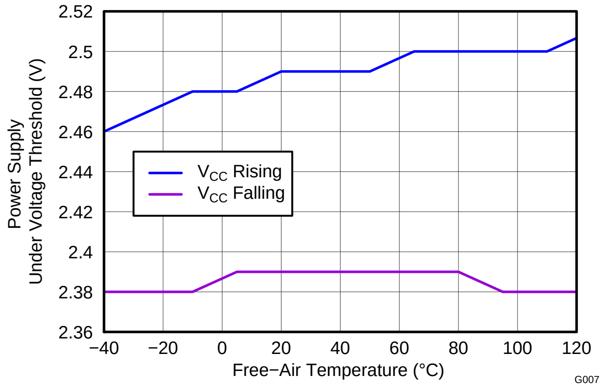


Figure 6. V_{CC} Undervoltage Threshold vs Free Air Temperature

Typical Characteristics (continued)

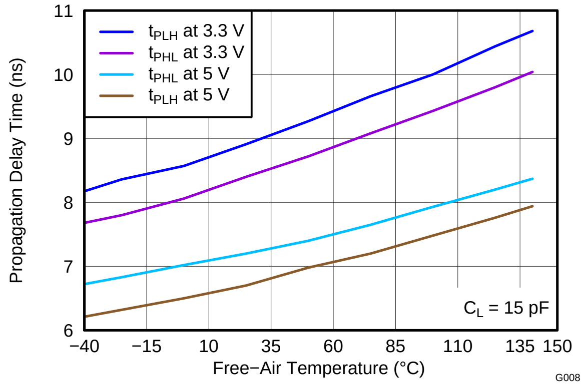


Figure 7. Propagation Delay Time vs Free Air Temperature

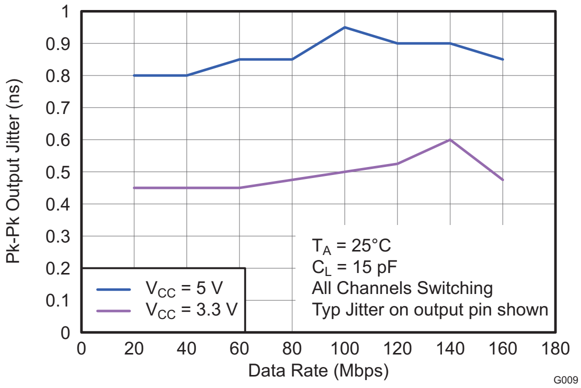
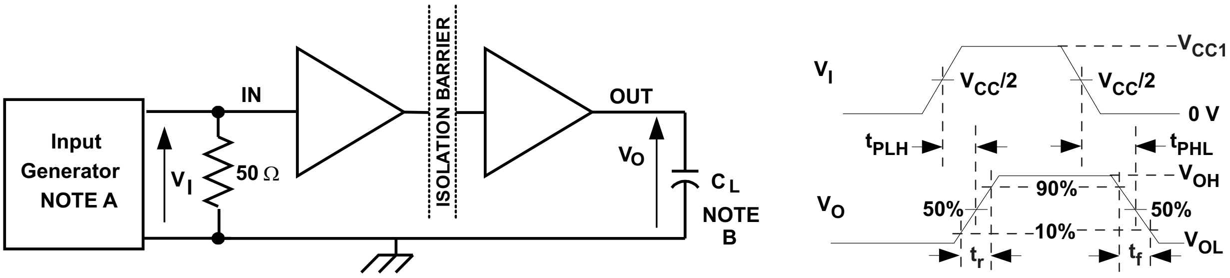


Figure 8. Output Jitter vs Data Rate

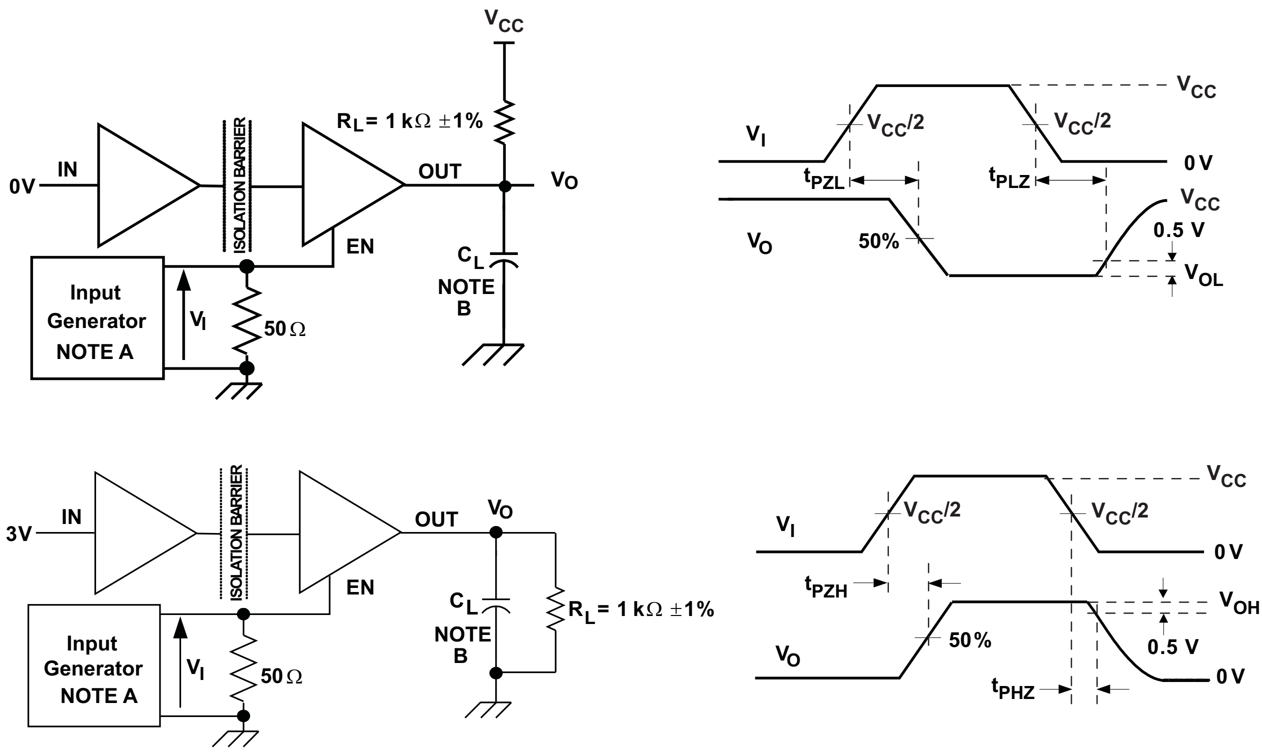
7 Parameter Measurement Information



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3ns, Z_O = 50 Ω. At the input, 50-Ω resistor is required to terminate Input Generator signal. It is not needed in actual application.

B. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 9. Switching Characteristics Test Circuit and Voltage Waveforms

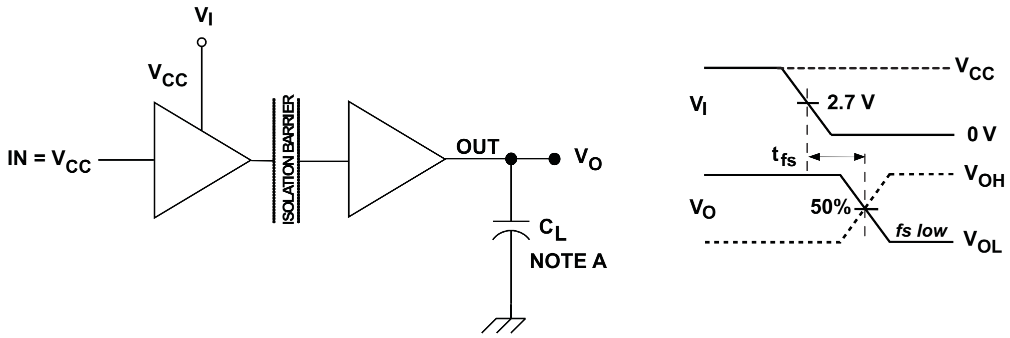


A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 10 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3 ns, Z_O = 50 Ω.

B. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

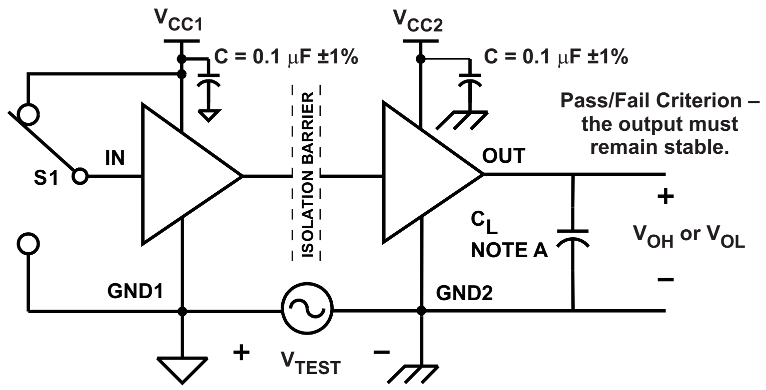
Figure 10. Enable/Disable Propagation Delay Time Test Circuit and Waveform

Parameter Measurement Information (continued)



A. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 11. Fail-Safe Delay Time Test Circuit and Voltage Waveforms



A. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 12. Common-Mode Transient Immunity Test Circuit

8 Detailed Description

8.1 Overview

The isolator in Figure 13 is based on a capacitive isolation barrier technique. The I/O channel of the device consists of two internal data channels, a high-frequency channel (HF) with a bandwidth from 100 kbps up to 150 Mbps, and a low-frequency channel (LF) covering the range from 100 kbps down to DC. In principle, a single- ended input signal entering the HF-channel is split into a differential signal via the inverter gate at the input. The following capacitor-resistor networks differentiate the signal into transients, which then are converted into differential pulses by two comparators. The comparator outputs drive a NOR-gate flip-flop whose output feeds an output multiplexer. A decision logic (DCL) at the driving output of the flip-flop measures the durations between signal transients. If the duration between two consecutive transients exceeds a certain time limit, (as in the case of a low-frequency signal), the DCL forces the output-multiplexer to switch from the high- to the low-frequency channel.

Because low-frequency input signals require the internal capacitors to assume prohibitively large values, these signals are pulse-width modulated (PWM) with the carrier frequency of an internal oscillator, thus creating a sufficiently high frequency signal, capable of passing the capacitive barrier. As the input is modulated, a low-pass filter (LPF) is needed to remove the high-frequency carrier from the actual data before passing it on to the output multiplexer.

8.2 Functional Block Diagram

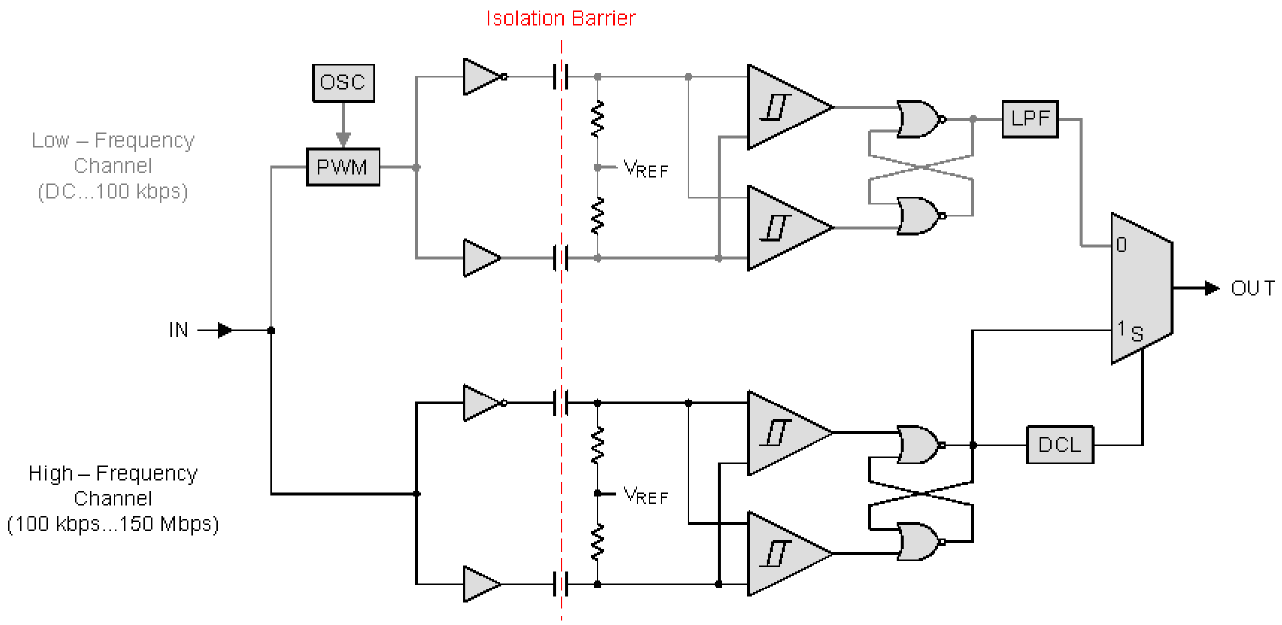


Figure 13. Conceptual Block Diagram of a Digital Capacitive Isolator

8.3 Feature Description

PRODUCT	RATED ISOLATION	PACKAGE	INPUT THRESHOLD	DATA RATE, INPUT FILTER	CHANNEL DIRECTION
ISO7640FM	6 KV_{PK} / 5 KV_{RMS} (1)	DW-16	1.5 V TTL	150 Mbps, No Noise Filter	4 Forward, 0 Reverse
ISO7641FM					3 Forward, 1 Reverse

(1) See the *Table 2* table for detailed isolation ratings.

8.3.1 IEC Insulation and Safety-Related Specifications for DW-16 Package

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
L(I01)	Minimum air gap (Clearance)	Shortest terminal to terminal distance through air	8.3			mm
L(I02)(1)	Minimum external tracking (Creepage)	Shortest terminal to terminal distance across the package surface	8.1			mm
CTI	Tracking resistance (Comparative Tracking Index)	DIN IEC 60112 / VDE 0303 Part 1	≥400			V
	Minimum Internal Gap (Internal Clearance)	Distance through the insulation	0.014			mm
R_{IO}(2)	Isolation resistance, Input to Output	V_{IO} = 500 V, T_A = 25°C		$>10^{12}$		Ω
		V_{IO} = 500 V, 100°C ≤ T_A ≤ T_A max		$>10^{11}$		
C_{IO}(2)	Barrier capacitance, Input to Output	V_I = 0.4 sin (2πft), f = 1MHz		2		pF
C_I(3)	Input capacitance	V_I = V_{CC}/2 + 0.4 sin (2πft), f = 1MHz, V_{CC} = 5 V		2		pF

(1) Per JEDEC package dimensions.
(2) All pins on each side of the barrier tied together creating a two-terminal device.
(3) Measured from input pin to ground.

NOTE

Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit-board (PCB) do not reduce this distance.

Creepage and clearance on a PCB become equal according to the measurement techniques shown in the Isolation Glossary. Techniques such as inserting grooves and/or ribs on a PCB are used to help increase these specifications.

8.3.2 DIN V VDE V 0884-10 (VDE V 0884-10) Insulation Characteristics

over recommended operating conditions (unless otherwise noted)(4)

PARAMETER		TEST CONDITIONS	SPECIFICATION	UNIT
V_{IORM}	Maximum working insulation voltage		1414	V_{PEAK}
V_{PR}	Input-to-output test voltage	After Input/Output safety test subgroup 2/3, V_{PR} = V_{IORM} x 1.2, t = 10 s, Partial discharge < 5 pC	1697	V_{PEAK}
		Method a, After environmental tests subgroup 1, V_{PR} = V_{IORM} x 1.6, t = 10 s, Partial Discharge < 5 pC	2262	
		Method b1, 100% Production test V_{PR} = V_{IORM} x 1.875, t = 1 s Partial discharge < 5 pC	2652	
V_{IOTM}	Maximum transient overvoltage	V_{TEST} = V_{IOTM} t = 60 sec (Qualification) t = 1 sec (100% Production)	6000	V_{PEAK}
R_S	Insulation resistance	V_{IO} = 500 V at T_S	$>10^9$	Ω
	Pollution degree		2	

(4) Climatic Classification 40/125/21

Table 1. IEC 60664-1 Ratings Table

PARAMETER	TEST CONDITIONS	SPECIFICATION
Basic Isolation Group	Material Group	II
Installation classification	Rated mains voltage ≤ 300 V_{RMS}	I–IV
	Rated mains voltage ≤ 600 V_{RMS}	I–III
	Rated mains voltage ≤ 1000 V_{RMS}	I–II

Table 2. Regulatory Information

VDE	TUV	CSA	UL	CQC
Certified according to DIN V VDE V 0884-10 (VDE V 0084-10):2006-12	Certified according to EN/UL/CSA 60950-1 and EN/UL/CSA 61010-1	Approved under CSA Component Acceptance Notice 5A, IEC 61010-1, IEC 60950-1, IEC 60601-1	Recognized under UL 1577 Component Recognition Program	Certified according to GB4943.1-2011
Basic Insulation, Maximum Transient Overvoltage, 6000 V_{PK} , Maximum Working Voltage, 1414 V_{PK}	5000 V_{RMS} Isolation Rating, Reinforced Insulation, 400 V_{RMS} maximum working voltage, Basic Insulation, 600 V_{RMS} maximum working voltage	5000 V_{RMS} Isolation Rating, 380 V_{RMS} Reinforced and 760 V_{RMS} Basic working voltage per CSA 60950-1-07 and IEC 60950-1 (2nd Ed.), 300 V_{RMS} Reinforced and 600 V_{RMS} Basic working voltage per CSA 61010-1-04 and IEC 61010-1 (2nd Ed.), 2 Means of Patient Protection at 125 V_{RMS} per CSA 60601-1:08 and IEC 60601-1 (3rd Ed.)	Single Protection, 4243 V_{RMS} (1)	Reinforced Insulation, Altitude ≤ 5000 m, Tropical Climate, 250 V_{RMS} maximum working voltage
Certificate number: 40016131	Certificate number: U8V 13 09 77311 010	Master contract number: 220991	File Number: E181974	Certificate number: CQC14001109542

(1) Production tested ≥ 5092 VRMS for 1 second in accordance with UL 1577.

8.3.3 Safety Limiting Values

Safety limiting intends to prevent potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the IO can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier potentially leading to secondary system failures.

Table 3. Safety Limiting Values

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_S	Safety input, output, or supply current	DW-16	θ_{JA} = 72°C/W, V_I = 5.5 V, T_J = 150°C, T_A = 25°C			316	mA
			θ_{JA} = 72°C/W, V_I = 3.6 V, T_J = 150°C, T_A = 25°C			482	
			θ_{JA} = 72°C/W, V_I = 2.7 V, T_J = 150°C, T_A = 25°C			643	
T_S	Maximum case temperature					150	°C

The safety-limiting constraint is the absolute maximum junction temperature specified in the absolute maximum ratings table. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determines the junction temperature. The assumed junction-to-air thermal resistance in the *Thermal Information* table is that of a device installed on a High-K Test Board for Leaded Surface Mount Packages. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance.

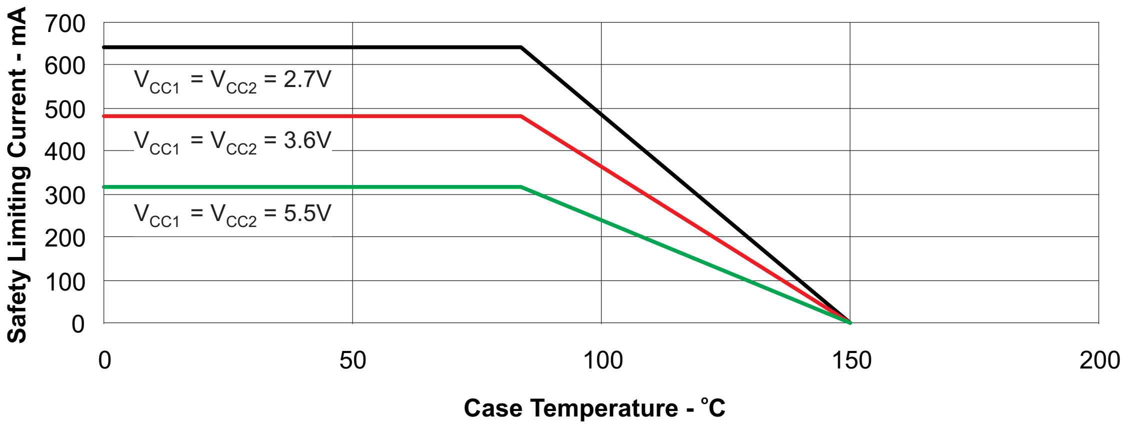


Figure 14. DW-16 θ_{JC} Thermal Derating Curve per DIN V VDE V 0884-10

8.4 Device Functional Modes

Table 4. Function Table(1)

V_{CCI}	V_{CCO}	INPUT (INx)	OUTPUT ENABLE (ENx)	OUTPUT (OUTx)
PU	PU	H	H or Open	H
		L	H or Open	L
		X	L	Z
		Open	H or Open	L
PD	PU	X	H or Open	L
PD	PU	X	L	Z
X	PD	X	X	Undetermined

(1) V_{CCI} = Input-side VCC; V_{CCO} = Output-side V_{CC}; PU = Powered Up ($V_{CC} \geq 2.7$ V); PD = Powered Down ($V_{CC} \leq 2.1$ V); X = Irrelevant; H = High Level; L = Low Level; Z = High Impedance

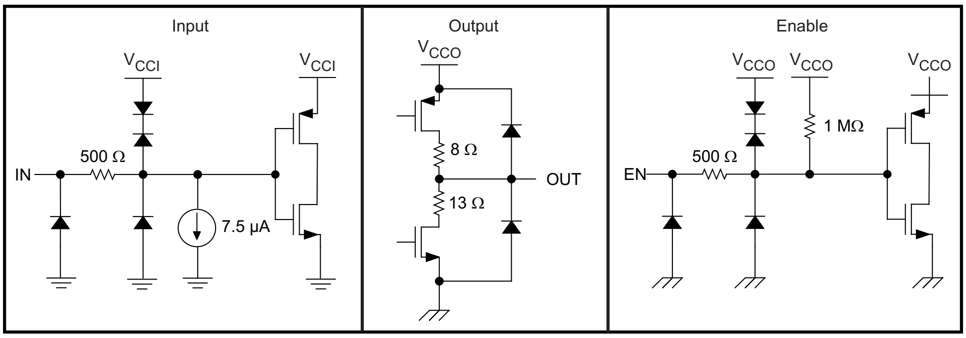


Figure 15. Device I/O Schematics

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

ISO764x use single-ended TTL-logic switching technology. Its supply voltage range is from 3 V to 5.5 V for both supplies, V_{CC1} and V_{CC2}. When designing with digital isolators, it is important to note that due to the single-ended design structure, digital isolators do not conform to any specific interface standard and are only intended for isolating single-ended CMOS or TTL digital signal lines. The isolator is typically placed between the data controller (that is, μC or UART), and a data converter or a line transceiver, regardless of the interface type or standard.

9.2 Typical Application

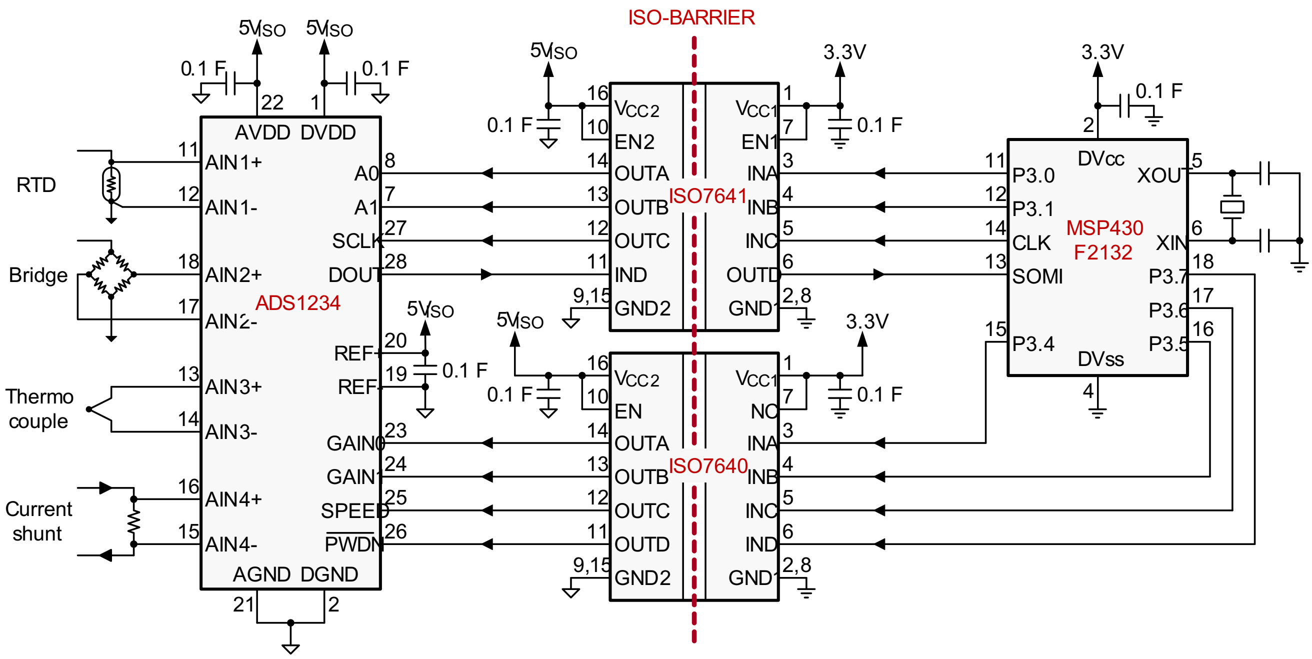


Figure 16. Isolated Data Acquisition System for Process Control

9.2.1 Design Requirements

Unlike optocouplers, which require external components to improve performance, provide bias, or limit current, the ISO764x device only requires two external bypass capacitors to operate.

Typical Application (continued)

9.2.2 Detailed Design Procedure

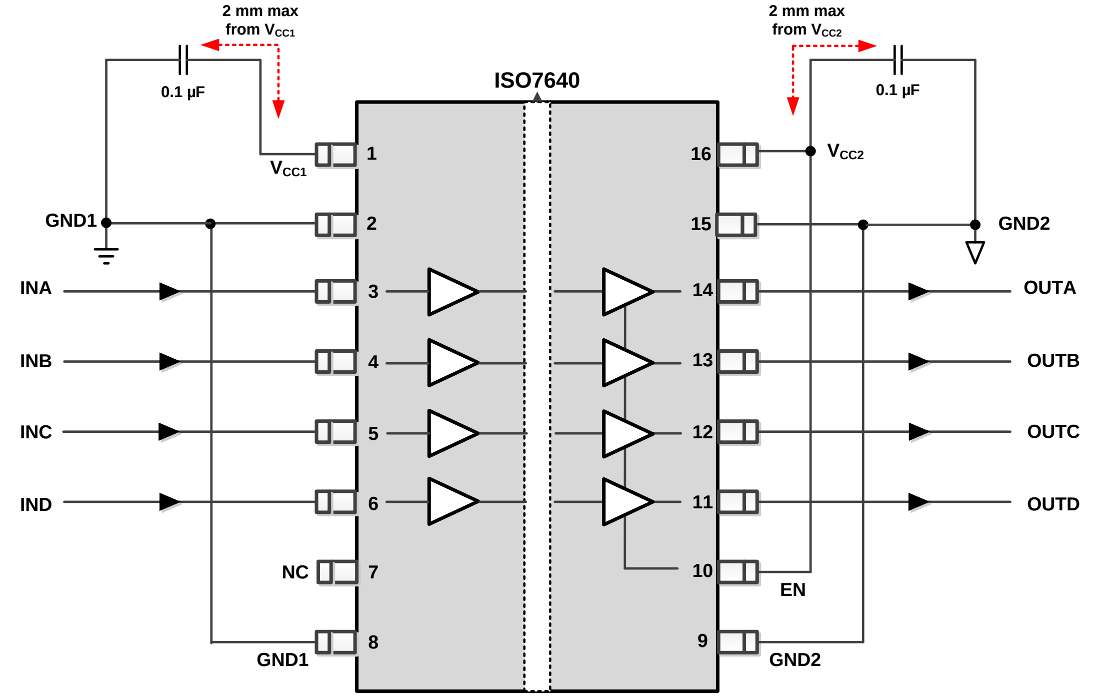


Figure 17. Typical ISO7640FM Circuit Hookup

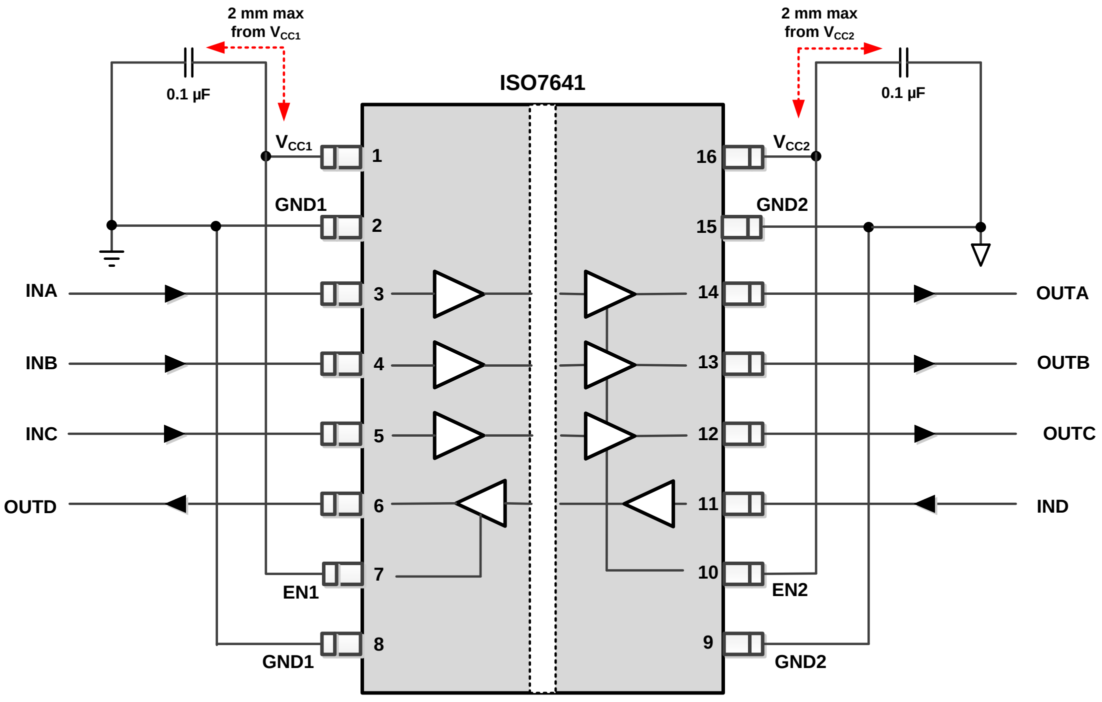


Figure 18. Typical ISO7641FM Circuit Hookup

Typical Application (continued)

9.2.2.1 Typical Supply Current Equations

(Calculated based on room temperature and typical Silicon process)

ISO7640FM:

At $V_{CC1} = V_{CC2} = 3.3$ V

$$I_{CC1} = 0.388 + 0.0312 \times f \quad (1)$$

$$I_{CC2} = 3.39 + 0.03561 \times f + 0.006588 \times f \times C_L \quad (2)$$

At $V_{CC1} = V_{CC2} = 5$ V

$$I_{CC1} = 0.584 + 0.05349 \times f \quad (3)$$

$$I_{CC2} = 4.184 + 0.05597 \times f + 0.009771 \times f \times C_L \quad (4)$$

ISO7641FM:

At $V_{CC1} = V_{CC2} = 3.3$ V

$$I_{CC1} = 1.848 + 0.03233 \times f + 0.001645 \times f \times C_L \quad (5)$$

$$I_{CC2} = 3.005 + 0.03459 \text{ x } f + 0.0049395 \times f \times C_L \quad (6)$$

At $V_{CC1} = V_{CC2} = 5$ V

$$I_{CC1} = 2.369 + 0.05385 \times f + 0.002448 \times f \times C_L \quad (7)$$

$$I_{CC2} = 3.857 + 0.05506 \times f + 0.007348 \times f \times C_L \quad (8)$$

I_{CC1} and I_{CC2} are typical supply currents measured in mA; f is data rate measured in Mbps; C_L is the capacitive load on each channel measured in pF.

9.2.3 Application Curves

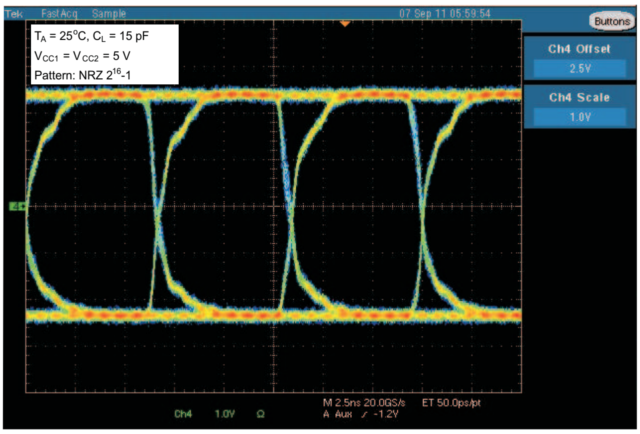


Figure 19. Typical Eye Diagram at 150 Mbps, 5-V Operation

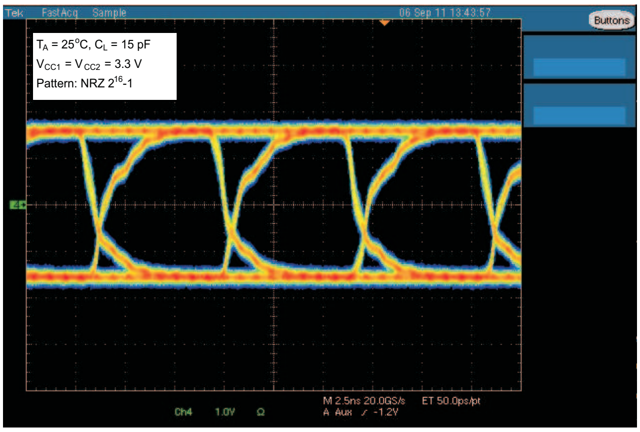


Figure 20. Typical Eye Diagram at 150 Mbps, 3.3-V Operation

10 Power Supply Recommendations

To ensure reliable operation at all data rates and supply voltages, a 0.1-μF bypass capacitor is recommended at input and output supply pins (V_{CC1} and V_{CC2}). The capacitors should be placed as close to the supply pins as possible. If only a single primary-side power supply is available in an application, isolated power can be generated for the secondary-side with the help of a transformer driver such as Texas Instruments' SN6501. For such applications, detailed power supply design and transformer selection recommendations are available in SN6501 data sheet (SLLSEA0).

11 Layout

11.1 Layout Guidelines

A minimum of four layers is required to accomplish a low EMI PCB design (see Figure 21). Layer stacking should be in the following order (top-to-bottom): high-speed signal layer, ground plane, power plane and low-frequency signal layer.

- Routing the high-speed traces on the top layer avoids the use of vias (and the introduction of their inductances) and allows for clean interconnects between the isolator and the transmitter and receiver circuits of the data link.
- Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100 pF/in^2.
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links usually have margin to tolerate discontinuities such as vias.

If an additional supply voltage plane or signal layer is needed, add a second power and ground plane system to the stack to keep it symmetrical. This makes the stack mechanically stable and prevents it from warping. Also the power and ground plane of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly.

NOTE

For detailed layout recommendations, see *Digital Isolator Design Guide*, SLLA284.

11.2 Layout Example

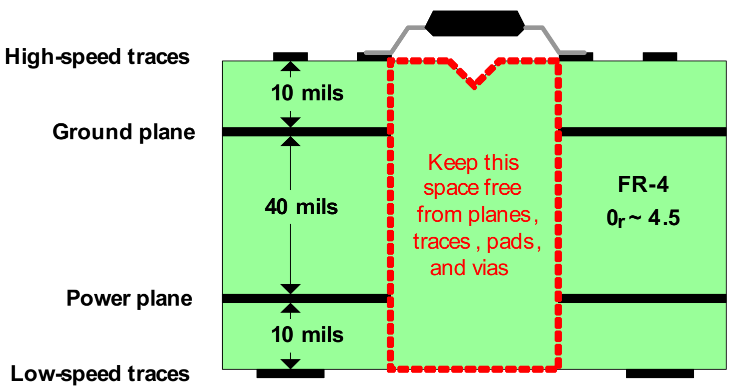


Figure 21. Recommended Layer Stack

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation, see the following:

- *Digital Isolator Design Guide*, SLLA284
- *Transformer Driver for Isolated Power Supplies*, SLLSEA0

12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 5. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
ISO7640FM	Click here	Click here	Click here	Click here	Click here
ISO7641FM	Click here	Click here	Click here	Click here	Click here

12.3 Trademarks

DeviceNet is a trademark of DeviceNet Open Vendors Association.
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

SLLA353 -- *Isolation Glossary.*

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ISO7640FMDW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	ISO7640FM	Samples
ISO7640FMDWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	ISO7640FM	Samples
ISO7641FMDW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	ISO7641FM	Samples
ISO7641FMDWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	ISO7641FM	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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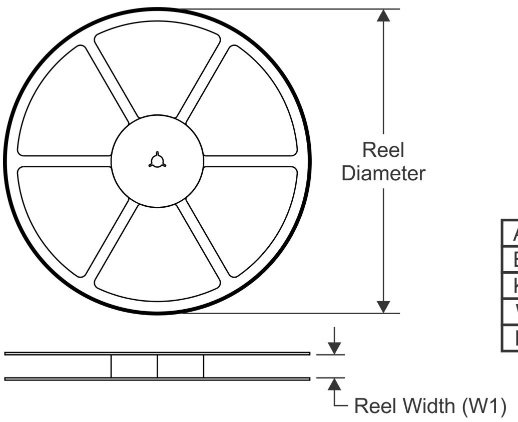
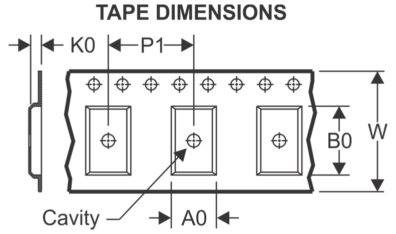
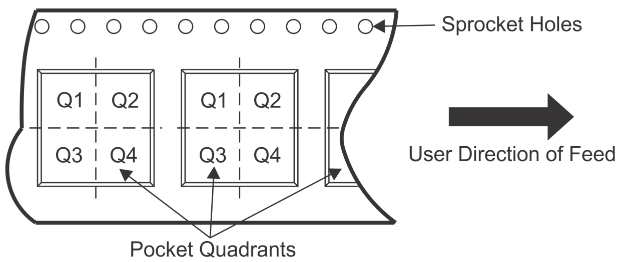
TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

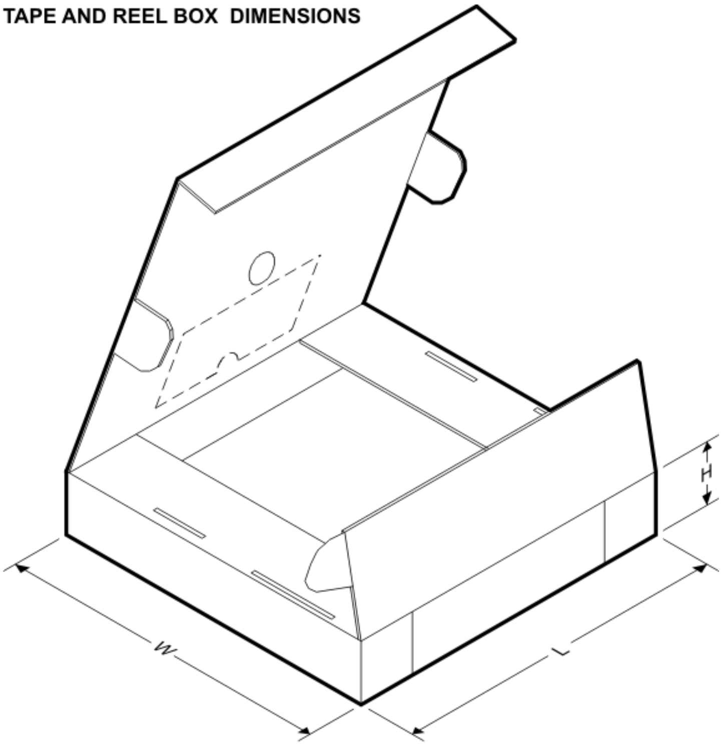
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISO7640FMDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7641FMDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

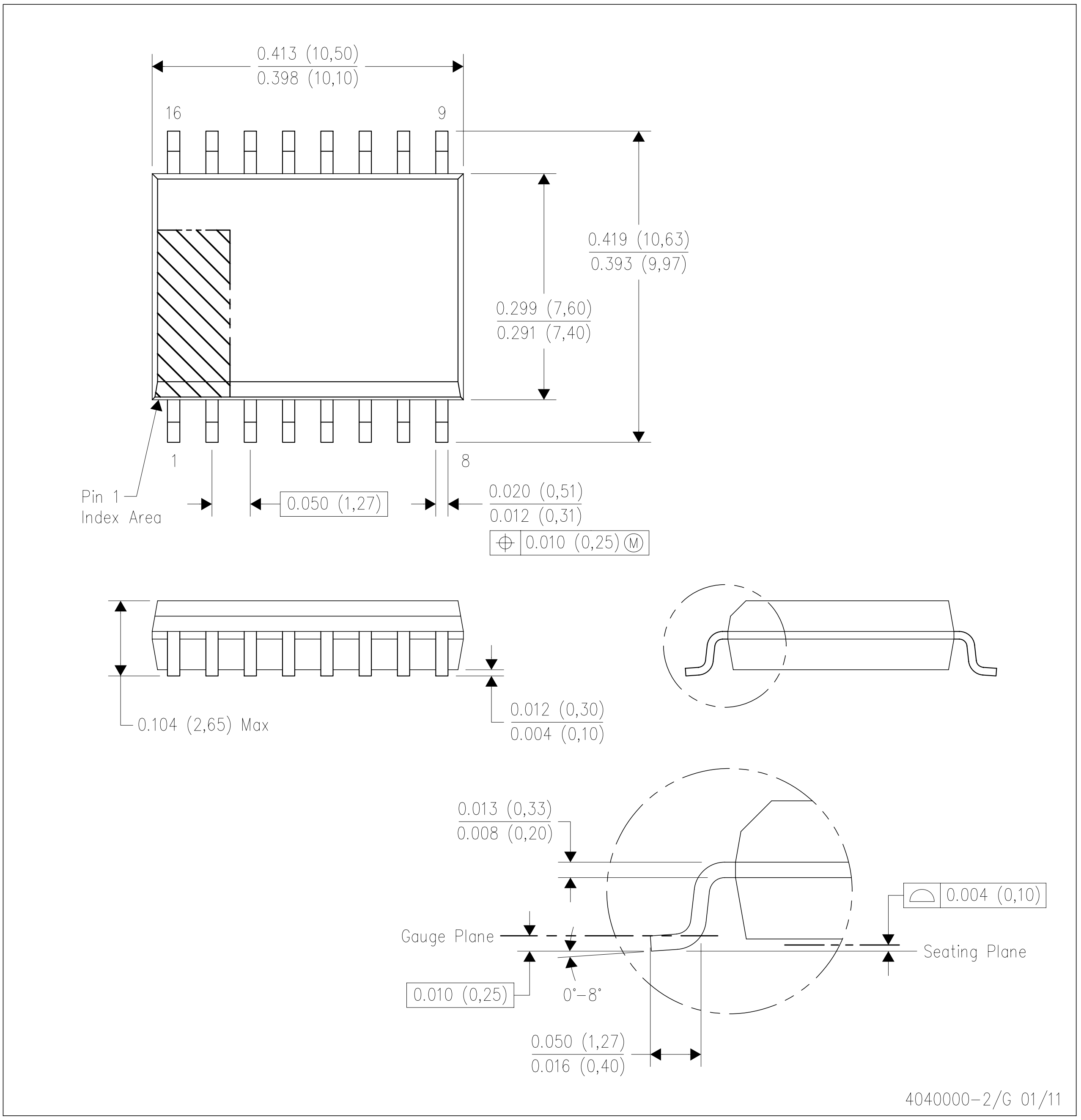


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISO7640FMDWR	SOIC	DW	16	2000	367.0	367.0	38.0
ISO7641FMDWR	SOIC	DW	16	2000	367.0	367.0	38.0

MECHANICAL DATA

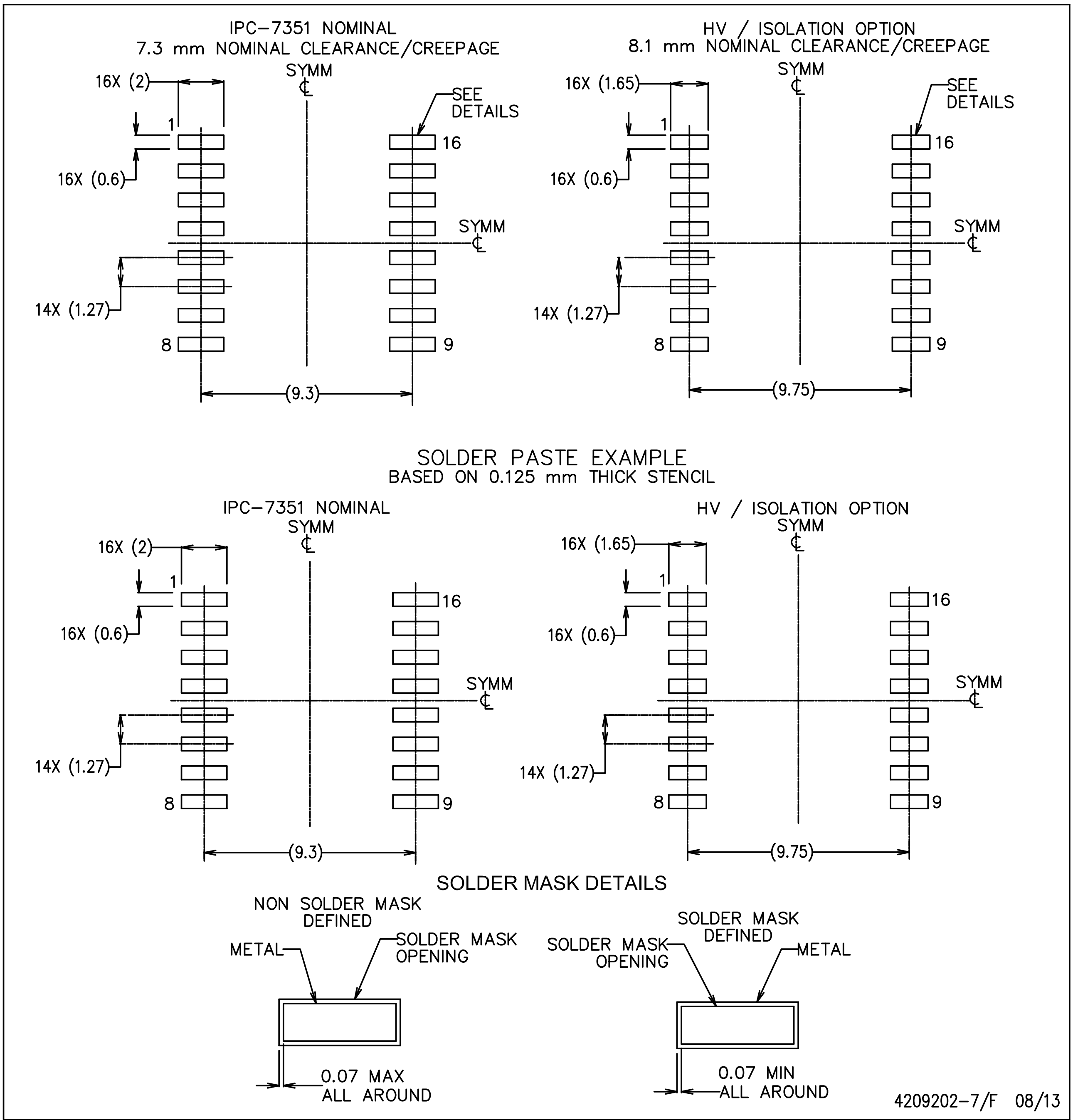
DW (R-PDSO-G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-013 variation AA.

LAND PATTERN DATA

DW (R-PDSO-G16) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Refer to IPC7351 for alternate board design.
- D. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
- E. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- F. Board assembly site may have different recommendations for stencil design.

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